2016 *mini*@sic Europractice MPW runs Schedule and Prices

Accessible for universities & research institutes
Version 160401 – v7

www.europractice-ic.com

mini@sic

Through the *mini***@sic** program the EUROPRACTICE IC Service is offering special MPW prototyping conditions to stimulate Academia and publicly funded Research Institutes to prototype small ASIC designs for education or publicly funded research. Through Multi Project Wafer Services, the high cost of a prototype run (masks and wafers) is shared amongst several customers. However for student education or PhD research programs the minimum prototyping charges are still too high. By introducing the *mini***@sic** concept on MPW runs EUROPRACTICE is offering considerably lower minimum prototyping charges for small ASIC designs. **Academia and Research Institutes will have the possibility to prototype small designs at low prices on selected MPW runs.**

ON Semiconductor (formerly AMIS)	J	F	M	A	M	J	J	A	S	O	N	D
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	18		29			13		16			2	
ON Semi 0.35µ C035U 4M (3M & 5M optional) only thick top metal		8		25			4		12		14	
ON Semi 0.7µ C07M-I2T100 100 V - 2M & 3M options	18		29			13		16			2	
ON Semi 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)	11			11			12			10		
ON Semi 0.35µ C035 - I3T50U 50 V 4M - 3M optional (5M on special request)			7			6			5			5
ON Semi 0.35µ C035 - I3T50U (E) 50 V 4M - 3M optional (5M on special request)			7			6			5			5
ON Semi 0.35µ C035 - I3T25U 3.3/25 V 4M (3M & 5M optional) only thick top metal		8		25			4		12		14	

ams	J	F	M	A	M	J	J	A	S	O	N	D
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO				18				1			21	
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO				18				1			21	
ams 0.35µ HV CMOS H35B4D3 120V 4M					2					31		
ams 0.35µ SiGe-BiCMOS S35 4M/4P						6						12
ams 0.18µ CMOS C18 6M/1P/MIM/1.8V/5V		22			23			22			28	
ams 0.18µ HV CMOS H18 50V/20V/5V/1.8V/ 6M/MIM		22			23			22			28	
Bottom Anti Reflective Coating (BARC) Diode for ams 0.35µ CMOS C35OPTO 4M/2P/5V IO				18				1				
Wafer Level Chip Scale Package for ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO								1			21	

IHP	J	F	M	A	M	J	J	A	S	O	N	D
IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V	25							1		31		
IHP SGB25VGD 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V + RF HV-LDMOS GD-Module 22V	25									31		
IHP SG25H1 0.25µ SiGe:C Ft/Fmax=190GHz/220GHz 5M/MIM	25				2			1				
IHP SG25H3P 0.25µ Complementary SiGe:C Ft/Fmax (npn)110/180GHz / (pnp)90/120GHz 5M/MIM										31		
IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM	25				2					31		
IHP SG25H4 0.25µ SiGe:C Ft/Fmax= 200/220GHz 5M/MIM	25				2			1		31		
SG25H_EPIC (based on SG25H4)										31		
IHP SG13S SiGe:C Bipolar/Analog/CMOS Ft/Fmax= 250/300GHz 7M/MIM			29					29				5
IHP SG13C SiGe:C CMOS 7M/MIM			29					29				5
IHP SG13G2 SiGe:C Bipolar/Analog Ft/Fmax= 300/500GHz 7M/MIM			29					29				5
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)					30							

Bumping available for all IHP technologies with extra charge, limited to 200 bumps

X-FAB	J	F	M	A	M	J	J	A	S	O	N	D
XH018 0.18µ HV NVM CMOS E-FLASH *		22				13				24		
XT018 0.18µ HV SOI CMOS **		1							12			

* Process modules included : LPMOS, ISOMOS, NVM, HVMOS, DMOS, MIM, MRPOLY, SCHOTTKY, OPT3, LVT, FLASH, MET3, METMID, MET4, PHOTODIO.
** Process modules included : MIM, LP5MOS, 1XN, 1XP, MET3, MET4, METMID, HVN, HVP, DTI, NBUR, HWC, HRPOLY, PSUB, DNC, DPC.

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS MS/RF (MIM: 2.0 fFum2 / UTM: 20kÅ)			23						7			
TSMC 0.18 CMOS High Voltage BCD Gen 2		24			4				7			
TSMC 90nm CMOS Low Power MS/RF (12-inch)		24		27		29		31		26		
TSMC 65nm CMOS Low Power MS/RF (12-inch)		2	23		25			31		19		
TSMC 40nm CMOS Low Power MS/RF (12-inch)	27		17			15		17			23	
TSMC 28nm CMOS HPL (HKMG)			30		25					26		

Runs in RED are preliminary

options TSMC mini@sic runs	IO	MIM /um2	special remarks
TSMC 0.18µ CMOS MS/RF	3.3 V	2 fF	6 metals with UTM (20kA) topmetal
TSMC 0.18 CMOS High Voltage BCD Gen 2 0.18 UM CMOS High Voltage Mixed Signal based General Purpose BCD Dual Gate FSG AL 1P6M [SALICIDE, NBL/PBL EPI, 1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5VV]		2 fF	6 metals with UTM (30kA) topmetal
TSMC 90nm CMOS LP MS RF	2.5V	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1N1U Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 65nm CMOS LP MS RF	2.5V (1.8UD, 3.3OD)	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1Z1U_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 40nm CMOS LP MS RF – **No Triple Gate oxide**	2.5V (1.8UD, 3.3OD)	-	Core : 1.1 V, Metal scheme : 1P8M_5X2Z_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 28nm CMOS HPL – High Performance Low Leakage	1.8 V	-	Core : 1.0 V, Metal scheme : 1P8M_5X1Z1U UTRDL (28kA thick AP layer) Default: BEOL option 1, 10 mils backlapping

UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L65N Logic/Mixed-Mode/RF - LL		1		25			25			24		
UMC L65N Logic/Mixed-Mode/RF - SP				25						24		
UMC L130 Mixed-Mode/RF		15				27				31		
UMC L180 Mixed-Mode/RF		29			23				5		28	

options UMC mini@sic runs	Core	IO	MIM	topmetal	special remarks
UMC L65N Logic/Mixed-Mode-MODE65N/RF - LL - 1P8M1T0F1U - 1.2V/2.5V	1.2	2.5V/2.5V_OD3.3V	2fF	32.5kA	Metal-stack "26"
UMC L65N Logic/Mixed-Mode-MODE65N/RF – SP – 1.0V/2.5V	1.0	2.5V/2.5V_OD3.3V	2fF	32.5kA	tbd
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	1.2V	3.3V	1fF	20kA	Possible combinations: HS, HS-LL (No SP possible)
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	1.8V	3.3V	1fF	20kA	

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 55 nm LPe		1		4		6				4		5
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	11		14		9		18				14	
GLOBALFOUNDRIES 28 nm SLP		22			2						21	
GLOBALFOUNDRIES 22 nm FDX									5			

Runs in RED are preliminary

2016 *mini*@sic Europractice MPW runs – Pricelist

Accessible for universities, research institutes and companies
Prices and conditions may change at any time without prior notice
Prices valid for runs starting 1 January 2016.

NON-EUROPEAN price applies to all non-European (not belonging to the countries of EUROPEAN price) universities and research institutes who submit designs for **educational or publicly funded research use only**

EUROPEAN price : only applies to EUROPRACTICE registered (who paid their annual full membership fee) Academic and Research Members from all 28 EU countries and Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine who submit designs for **educational or publicly funded research use only.**
For the following technologies, there are special discounted prices thanks to a special grant through the EU-Project EUROPRACTICE 2013 in the 7th Framework : ams 0.18 HV CMOS H18, IHP SG25Hx and SG13x, TSMC 90, 65, 40 & 28nm, UMC 90 & 65nm, XFAB XH018 & XT018, GLOBALFOUNDRIES 55, 40, 28 & 22nm.

Prices are given for the delivery of unpackaged, untested prototypes. Encapsulation and testing will be charged separately.

Number of prototypes
OnSemi > 20 samples
ams : 40 samples
UMC : 0.18um, 0.13um : 25 samples
UMC : 65nm : 45 samples
IHP : 40 samples SG25 & SG13, 20 samples PIC, EPIC & MEMS
XFAB : 15 samples
TSMC : 40 samples for 0.18u, 100 samples for 90 … 28nm
GLOBALFOUNDRIES : 50 samples
If you need more prototype samples, please ask for a quotation

Plots
You can order plots/PDF of your designs
- first plot/PDF costs 50 euro
- next plots cost 20 euro each

Packaging : see separate prices and available packages

ALL PRICES IN EURO

ON Semiconductor (formerly AMIS)	NON-EUROPEAN Price/mm²	EUROPEAN Price/mm²
ON Semi 0.7µ C07M-D 2M/1P	300 [2]	270 [2]
ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	350 [2]	315 [2]
ON Semi 0.35µ C035U 4M (default) including analog options	720 [2]	670 [2]
ON Semi 0.35µ C035U 3M (optional) including analog options	700 [2]	650 [2]
ON Semi 0.35µ C035U 5M (optional) including analog options	800 [2]	750 [2]
ON Semi 0.7µ C07M-I2T100 100 V - 2M	525 [2]	485 [2]
ON Semi 0.7µ C07M-I2T100 100 V - 3M	560 [2]	525 [2]
ON Semi 0.35µ C035 - I3T80U 80 V 3M	850 [2]	800 [2]
ON Semi 0.35µ C035 - I3T80U 80 V 4M	925 [2]	875 [2]
ON Semi 0.35µ C035 - I3T80U 80 V 5M	1050 [2]	995 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 3M	850 [2]	800 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 4M	925 [2]	875 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 5M	1050 [2]	995 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 3M (optional)	750 [2]	700 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 4M (default)	770 [2]	720 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 5M (optional)	800 [2]	750 [2]

ams	NON-EUROPEAN Price/mm²	EUROPEAN Price/mm²
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	640 [2]	580 [2]
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	800 [3]	700 [3]
ams 0.35µ HV CMOS H35B4D3 120V 4M	880 [2]	800 [2]
ams 0.35µ SiGe-BiCMOS S35 4M/4P	880 [2]	800 [2]
ams 0.18µ CMOS C18 6M/1P/MIM/1.8V/5V	1100 [3]	1050 [3]
ams 0.18µ HV CMOS H18 50V/20V/5V/1.8V/ 6M/MIM	1200 [3]	1000 & 1100 [5]
Bottom Anti Reflective Coating (BARC) Diode for ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	One-off extra fee of 6500	One-off extra fee of 4500
Wafer Level Chip Scale Package for ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	One-off extra fee of 6000	One-off extra fee of 4000

IHP	NON-EUROPEAN Price/mm²	EUROPEAN Price/mm²
IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V	2125 [4]	1940 [4]
IHP SGB25VGD 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V + RF HV-LDMOS GD-Module 22V	2680 [4]	2445 [4]
IHP SG25H1 0.25µ SiGe:C Ft/Fmax=190GHz/220GHz 5M/MIM	5525 [4]	4875 [4, 6]
IHP SG25H3P 0.25µ Complementary SiGe:C Ft/Fmax (npn)110/180GHz / (pnp)90/120GHz 5M/MIM	4930 [4]	4350 [4, 6]
IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM	3230 [4]	2950 [4, 6]
IHP SG25H4 0.25µ SiGe:C Ft/Fmax= 200/220GHz 5M/MIM	4250 [4]	3750 [4, 6]
SG25H_EPIC (based on SG25H4)	5950 [4]	4550 [4, 6]
IHP SG13G2 SiGe:C Bipolar/Analog Ft/Fmax= 300/500GHz 7M/MIM	6375 [4]	5625 [4, 6]
IHP SG13S SiGe:C Bipolar/Analog/CMOS Ft/Fmax= 250/300GHz 7M/MIM	5780 [4]	5100 [4, 6]
IHP SG13C SiGe:C CMOS 7M/MIM	3825 [4]	3375 [4]
IHP SG25 PIC (Photonics devices, Ge Photo-diode, BEOL)	1700 [4]	1300 [4]

X-FAB	NON-EUROPEAN Price/block	EUROPEAN Price/block
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, MET4, METMID)	3765 [7]	3575 [7]
X-FAB XT018 0.18µ HV SOI CMOS (MET3, MET4, METMID)	3815 [7]	3625 [7]

TSMC	NON-EUROPEAN Price/block	EUROPEAN Price/block
TSMC 0.18 CMOS General Logic or MS/RF	4090 [12]	3890 [12]
TSMC 0.18 CMOS High Voltage BCD Gen 2	5770 [22]	5490 [22]
TSMC 90nm CMOS LP MS RF	12660 [13]	12030 [13]
TSMC 65nm CMOS LP MS RF	17070 [13]	16220 [13]
TSMC 40nm CMOS LP MS RF	22950 [11]	21810 [11]
TSMC 28nm CMOS HPL	24000 [21]	22800 [21]

UMC	NON-EUROPEAN Price/block	EUROPEAN Price/block
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	3320 [7]	3160 [7]
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	5600 [7]	5320 [7]
UMC L65N LOGIC/MIXED LL & L65N LOGIC/MIXED SP	11180 [8]	10630 [8]

GLOBALFOUNDRIES	NON-EUROPEAN Price : see notes	EUROPEAN Price : see notes
GLOBALFOUNDRIES 55 nm LPe	3850 [16, 15]	3550 [14, 15]
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	4750 [18, 15]	4450 [17, 15]
GLOBALFOUNDRIES 28 nm SLP	9800 [20, 15]	9000 [19, 15]
GLOBALFOUNDRIES 22 nm FDX	17000 [24, 15]	16000 [23, 15]

Notes

1) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 6 mm^2
2) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 4 mm^2
3) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 5 mm^2
4) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 0.8 mm^2
5) Minimum charged area = 5 mm^2.
   For area ≤ 5 mm^2, Price = 5000 euro
   For area > 5 mm^2, Price = 5000 + (area-5) * 1100
6) Minimum charged area = 0.8 mm^2
   For area ≤ 0.8 mm^2, Price = price/mm^2 – 30%
   For area > 0.8 mm^2, Price = price/mm^2 – 30% + (area-0.8)*price/mm^2
7) Price = per block of 1525x1525 microns needed to fit the design in. Adding two blocks together to one block is possible.
8) Price = per block of 1875x1875 microns needed to fit the design in. Adding two blocks together to one block is possible.
9) Minimum charged area = 4 mm^2.
   For area ≤ 4 mm^2, Price = 3200 euro
   For area > 4 mm^2, Price = 3200 + (area-4) * 880
10) Price = per submitted design to be bumped (no size limit, limited to 200 bumps)
11) Price = per block of 1920x1920 microns needed to fit the design in (designed dimensions – PRE-SHRINK) – see below
12) Price = per block of 1660x1660 microns needed to fit the design in
13) Price = per block of 2000x2000 microns needed to fit the design in
14) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 13400 euro. For area > 3 mm^2, Price = 13400 + (area-3) * 3550
15) Any die sizes between (1.5mmx1.5mm) to (12.5mmx12.5mm) possible. The mentioned die size is referred to the Pre-Shrink die size
16) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 19320 euro. For area > 4 mm^2, Price = 19320 + (area-4) * 3850
17) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 17460 euro. For area > 3 mm^2, Price = 17460 + (area-3) * 4450
18) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 25200 euro. For area > 4 mm^2, Price = 25200 + (area-4) * 4750
19) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 27000 euro. For area > 3 mm^2, Price = 27000 + (area-3) * 9000
20) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 48550 euro. For area > 4 mm^2, Price = 48550 + (area-4) * 9800
21) Price = per block of 1570x1570 microns needed to fit the design in (designed dimensions – PRE-SHRINK) – see below
22) Price = per block of 2500x2500 microns needed to fit the design in
23) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 48000 euro. For area > 3 mm^2, Price = 48000 + (area-3) * 16000
24) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 83000 euro. For area > 4 mm^2, Price = 83000 + (area-4) * 17000

UMC 0.18 and 0.13µ mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1525 x 1525 µm
- 2 sub-blocks : design may not be larger than 3240 x 1525 µm
- 3 sub-blocks : design may not be larger than 4960 x 1525 µm
- 4 sub-blocks : design may not be larger than 3240 x 3240 µm
- 6 sub-blocks : design may not be larger than 4960 x 3240 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

UMC 90nm & 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1875 x 1875 µm
- 2 sub-blocks : design may not be larger than 3950 x 1875 µm

TSMC 90nm & 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2000 x 2000 µm
- 2 sub-blocks : design may not be larger than 4000 x 2000 µm

TSMC 40nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1920 x 1920 µm
- 2 sub-blocks : design may not be larger than 3840 x 1920 µm
- These are designed dimensions. Fabricated designs (40nm) are shrinked during maskmaking in both X and Y directions by 0.9

TSMC 28nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1570 x 1570 µm
- 2 sub-blocks : design may not be larger than 3140 x 1570 µm
- These are designed dimensions. Fabricated designs (28nm) are shrinked during maskmaking in both X and Y directions by 0.9

TSMC 0.18µ CMOS mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1660 x 1660 µm
- 2 sub-blocks : design may not be larger than 3320 x 1660 µm
- 3 sub-blocks : design may not be larger than 4980 x 1660 µm
- 4 sub-blocks : design may not be larger than 3320 x 3320 µm
- 6 sub-blocks : design may not be larger than 4980 x 3320 µm

TSMC 0.18µ HV BCD mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2500 x 2500 µm
- 2 sub-blocks : design may not be larger than 5000 x 2500 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

Contacts
imec, Belgium (P. Malisse, tel: +32 16 281272, e-mail: mpc@imec.be)
Fraunhofer IIS, Germany (W. McKinley, tel : +49 9131 776 4413, e-mail: europrac@iis.fraunhofer.de)