EUROPRACTICE IC SERVICE

European Commission | Horizon 2020 European Union funding for Research & Innovation

2017 *mini*@sic Europractice MPW runs Schedule and Prices

Accessible for universities & research institutes
Version 170524- v13

www.europractice-ic.com

mini@sic

Through the *mini***@sic** program the EUROPRACTICE IC Service is offering special MPW prototyping conditions to stimulate Academia and publicly funded Research Institutes to prototype small ASIC designs for education or publicly funded research. Through Multi Project Wafer Services, the high cost of a prototype run (masks and wafers) is shared amongst several customers. However for student education or PhD research programs the minimum prototyping charges are still too high. By introducing the *mini***@sic** concept on MPW runs EUROPRACTICE is offering considerably lower minimum prototyping charges for small ASIC designs. **Academia and Research Institutes will have the possibility to prototype small designs at low prices on selected MPW runs.**

ON Semiconductor (formerly AMIS)	J	F	M	A	M	J	J	A	S	O	N	D
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	16		27			5		14		30		
ON Semi 0.35µ C035U 4M (3M & 5M optional) only thick top metal	30			17			3		18			4
ON Semi 0.7µ C07M-I2T100 100 V - 2M & 3M options	16		27			5		14		30		
ON Semi 0.35µ C035 - I3T80U 80 V 4M (3M & 5M optional) only thick top metal	2			3			10			9		
ON Semi 0.35µ C035 - I3T50U 50 V 4M - 3M optional (5M on special request)			6		29				4			4
ON Semi 0.35µ C035 - I3T50U (E) 50 V 4M - 3M optional (5M on special request)			6		29				4			4
ON Semi 0.35µ C035 - I3T25U 3.3/25 V 4M (3M & 5M optional) only thick top metal	30			17			3		18			4

ams	J	F	M	A	M	J	J	A	S	O	N	D
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO				24				7			20	
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO				24				7			20	
ams 0.35µ HV CMOS H35B4D3 120V 4M					2					30		
ams 0.35µ SiGe-BiCMOS S35 4M/4P						6						11
ams 0.18µ CMOS aC18 6M/1P/MIM/1.8V/5V		20			22			21			27	
ams 0.18µ HV CMOS aH18 50V/20V/5V/1.8V/ 6M/MIM								21			27	
Bottom Anti Reflective Coating (BARC) Diode for ams 0.35µ CMOS C35OPTO 4M/2P/5V IO				24				7			20	
Wafer Level Chip Scale Package for ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO				24				7			20	

Note: Customers making use of WLSCP have to send in their design gds file two weeks before the indicated deadline

IHP	J	F	M	A	M	J	J	A	S	O	N	D
IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V				21				4				
IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM	30							4				
IHP SG25H4 0.25µ SiGe:C Ft/Fmax= 200/220GHz 5M/MIM	30			21				4				
SG25H_EPIC (based on SG25H4)										20		
IHP SG13S SiGe:C Bipolar/Analog/CMOS/RF-MEMS Ft/Fmax= 250/300GHz 7M/MIM			17					18			24	
IHP SG13C SiGe:C CMOS 7M/MIM			17					18			24	
IHP SG13G2 SiGe:C Bipolar/Analog/RF-MEMS Ft/Fmax= 300/500GHz 7M/MIM			17					18			24	
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)				7								

Bumping available for all IHP technologies with extra charge, limited to 200 bumps
Important Note: Dates are registration deadlines after which designs cannot enter this MPW run anymore. Final GDSII file must be submitted within 10 days after this date.

X-FAB	J	F	M	A	M	J	J	A	S	O	N	D
XH018 0.18µ HV NVM CMOS E-FLASH *				24						30		
XT018 0.18µ HV SOI CMOS **			13						18			

* Process modules included for metal 6 option : LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO.
** Process modules included for metal 6 option : LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, MET4, METMID, METTHK, HWC.

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS General Logic or MS/RF (MIM: 2.0 fFum2 / UTM: 20kÅ)	31				17				27			
TSMC 0.18 CMOS High Voltage BCD Gen 2					31				27			
TSMC 90nm CMOS LP MS RF		22				21				25		
TSMC 65nm CMOS LP MS RF		15			24			23			22	
TSMC 40nm CMOS LP MS RF		8				14				18		
TSMC 28nm CMOS HPL RF (reserve 4 months in advance)		22										
TSMC 28nm CMOS HPC RF (reserve 4 months in advance)				26						25		

options TSMC mini@sic runs	IO	MIM /um2	special remarks
TSMC 0.18µ CMOS MS/RF	3.3 V	2 fF	6 metals with UTM (20kA) topmetal
TSMC 0.18 CMOS High Voltage BCD Gen 2 0.18 UM CMOS High Voltage Mixed Signal based General Purpose BCD Dual Gate FSG AL 1P6M [SALICIDE, NBL/PBL EPI, 1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5VV]		2 fF between M5 & M6	6 metals with UTM (30kA) topmetal
TSMC 90nm CMOS LP MS RF	2.5V	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1N1U Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 65nm CMOS LP MS RF	2.5V (1.8UD, 3.3OD)	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1Z1U_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 40nm CMOS LP MS RF – **No Triple Gate oxide**	2.5V (1.8UD, 3.3OD)	-	Core : 1.1 V, Metal scheme : 1P8M_5X2Z_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 28nm CMOS HPL – High Performance Low Leakage, RF	1.8 V	-	Core : 1.0 V, Metal scheme : 1P8M_5X1Z1U UTRDL (28kA thick AP layer) Default: BEOL option 1, 10 mils backlapping
TSMC 28nm CMOS HPC – High Performance Compact Mobile Computing, RF	1.8 V	-	Core : 0.9 V, Metal scheme : 1P8M_5X1Z1U UTRDL (28kA thick AP layer) Default: BEOL option 1, 10 mils backlapping

UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L65N Logic/Mixed-Mode/RF - LL	30			24			24			23		
UMC L130 Mixed-Mode/RF		27				19				30		
UMC L180 Mixed-Mode/RF	23		20		30		17		25		27	
UMC 40nm Logic/Mixed-Mode/LP						5				16		

options UMC mini@sic runs	Core	IO	MIM	topmetal	special remarks
UMC L65N Logic/Mixed-Mode-MODE65N/RF - LL - 1P8M1T0F1U - 1.2V/2.5V	1.2	2.5V/2.5V_OD3.3V	2fF	32.5kA	Metal-stack "26"
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	1.2V	3.3V	1fF	20kA	Possible combinations: HS, HS-LL (No SP possible)
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	1.8V	3.3V	1fF	20kA	
UMC 40nm LP Logic/MS	This is work in progress. Target to get it fully settled mid January				

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 55 nm LPe			13						18			
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave				3						2		
GLOBALFOUNDRIES 28 nm SLP/SLP-RF					8						6	
GLOBALFOUNDRIES 22 nm FDSOI										2		

Important Note: Dates are registration deadlines after which designs cannot enter this MPW run anymore. Final GDSII file must be submitted within 6 weeks after this date.

2017 *mini*@sic Europractice MPW runs – Pricelist

Accessible for universities, research institutes and companies
Prices and conditions may change at any time without prior notice
Prices valid for runs starting 1 January 2017.

NON-EUROPEAN price applies to all non-European (not belonging to the countries of EUROPEAN price) universities and research institutes who submit designs for **educational or publicly funded research use only.**

EUROPEAN price : only applies to EUROPRACTICE registered (who paid their annual full membership fee) Academic and Research Members from all 28 EU countries and Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine who submit designs for **educational or publicly funded research use only.**
For the following technologies, there are special discounted prices thanks to a special grant through the EU-Project EUROPRACTICE 2016 in the H2020 Framework : ams 0.35µm and 0.18µm, IHP SG25Hx and SG13x, TSMC 0.18µm, 90, 65, 40 & 28nm, UMC 180, 130, 65 & 40nm, XFAB XH018 & XT018, GLOBALFOUNDRIES 55, 40, 28 & 22nm and On Semi 0.7 and 0.35µm.

Prices are given for the delivery of unpackaged, untested prototypes. Encapsulation and testing will be charged separately.

Number of prototypes
OnSemi > 20 samples
ams : 40 samples
UMC : 0.18um, 0.13um : 25 samples
UMC : 65nm, 40nm : 45 samples
IHP : 40 samples SG25 & SG13, 20 samples PIC, EPIC & MEMS
XFAB : 15 samples
TSMC : 40 samples for 0.18u, 100 samples for 90 … 28nm
GLOBALFOUNDRIES : 50 samples
If you need more prototype samples, please ask for a quotation

Plots
You can order plots/PDF of your designs
- first plot/PDF costs 50 euro
- next plots cost 20 euro each

Packaging : see separate prices and available packages

ALL PRICES IN EURO

ON Semiconductor (formerly AMIS)	NON-EUROPEAN Price/mm²	EUROPEAN Price/mm²
ON Semi 0.7µ C07M-D 2M/1P	300 [2]	270 [2]
ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	350 [2]	315 [2]
ON Semi 0.7µ C07M-I2T100 100 V - 2M	525 [2]	485 [2]
ON Semi 0.7µ C07M-I2T100 100 V - 3M	560 [2]	525 [2]
ON Semi 0.35µ C035U 4M (default) including analog options	720 [2]	670 [2]
ON Semi 0.35µ C035U 3M (optional) including analog options	700 [2]	650 [2]
ON Semi 0.35µ C035U 5M (optional) including analog options	800 [2]	750 [2]
ON Semi 0.35µ C035 - I3T80U 80 V 3M	850 [2]	800 [2]
ON Semi 0.35µ C035 - I3T80U 80 V 4M	925 [2]	875 [2]
ON Semi 0.35µ C035 - I3T80U 80 V 5M	1050 [2]	995 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 3M	850 [2]	800 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 4M	925 [2]	875 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 5M	1050 [2]	995 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 3M (optional)	750 [2]	700 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 4M (default)	770 [2]	720 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 5M (optional)	800 [2]	750 [2]

ams	NON-EUROPEAN Price/mm²	EUROPEAN Price/mm²
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	640 [2]	580 [2]
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	800 [2]	700 [2]
ams 0.35µ HV CMOS H35B4D3 120V 4M	880 [2]	800 [2]
ams 0.35µ SiGe-BiCMOS S35 4M/4P	880 [2]	800 [2]
ams 0.18µ CMOS aC18 6M/1P/MIM/1.8V/5V	1100 [2]	1050 [2]
ams 0.18µ HV CMOS aH18 50V/20V/5V/1.8V/ 6M/MIM	1150 [2]	1100 [2]
Bottom Anti Reflective Coating (BARC) Diode for ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	One-off extra fee of 6900	One-off extra fee of 4500
Wafer Level Chip Scale Package for ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	One-off extra fee of 6250	One-off extra fee of 4000

IHP	NON-EUROPEAN Price/mm²	EUROPEAN Price/mm²
IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V	2125 [4]	1940 [4]
IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM	3230 [4]	2950 [4]
IHP SG25H4 0.25µ SiGe:C Ft/Fmax= 200/220GHz 5M/MIM	3910 [4]	3220 [4]
SG25H_EPIC (based on SG25H4)	5610 [4]	3960 [4]
IHP SG13G2 SiGe:C Bipolar/Analog Ft/Fmax= 300/500GHz 7M/MIM	6205 [4]	5110 [4, 6]
IHP SG13S SiGe:C Bipolar/Analog/CMOS Ft/Fmax= 250/300GHz 7M/MIM	5355 [4]	4410 [4]
IHP SG13C SiGe:C CMOS 7M/MIM	3825 [4]	3375 [4]
IHP SG25 PIC (Photonics devices, Ge Photo-diode, BEOL)	1700 [4]	1200 [4]

X-FAB	NON-EUROPEAN Price/block	EUROPEAN Price/block
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, MET4, METMID, METTHK)	3950 [7]	3765 [7]
X-FAB XT018 0.18µ HV SOI CMOS (MET3, MET4, METMID, METTHK)	4040 [7]	3840 [7]

TSMC	NON-EUROPEAN Price/block	EUROPEAN Price/block
TSMC 0.18 CMOS General Logic or MS/RF	3840 [13]	3650 [13]
TSMC 0.18 CMOS High Voltage BCD Gen 2	5420 [23]	5150 [23]
TSMC 90nm CMOS LP MS RF	11880 [14]	11290 [14]
TSMC 65nm CMOS LP MS RF	15500 [14]	14730 [14]
TSMC 40nm CMOS LP MS RF	20840 [12]	19800 [12]
TSMC 28nm CMOS HPL RF	22470 [22]	21350 [22]
TSMC 28nm CMOS HPC RF	23130 [22]	21980 [22]

UMC	NON-EUROPEAN Price/block	EUROPEAN Price/block
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	3120 [8]	2970 [8]
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	5250 [8]	4990 [8]
UMC L65N Logic/Mixed-Mode LL & L65N Logic/Mixed-Mode SP	10470 [9]	9950 [9]
UMC 40nm LP Logic/Mixed Mode/RF	20180 [9]	19180 [9]

GLOBALFOUNDRIES	NON-EUROPEAN Price: see notes	EUROPEAN Price: see notes
GLOBALFOUNDRIES 55 nm LPe	18500 & 4000 [17, 16, 26]	13900 & 3800 [15, 16]
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	23750 & 5000 [19, 16, 26]	17850 & 4700 [18, 16]
GLOBALFOUNDRIES 28 nm SLP	46800 & 10200 [21, 16, 26]	29100 & 9700 [20, 16]
GLOBALFOUNDRIES 22 nm FDSOI	65000 & 14700 [25, 16, 26]	42000 & 14000 [24, 16]

Notes

1) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 3 mm^2
2) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 4 mm^2
3) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 5 mm^2
4) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 0.8 mm^2
5) Minimum charged area = 5 mm^2.
   For area ≤ 5 mm^2, Price = 5000 euro
   For area > 5 mm^2, Price = 5000 + (area-5) * 1100
6) Minimum charged area = 0.8 mm^2
   For area ≤ 0.8 mm^2, Price = 3270 euro
   For area > 0.8 mm^2, Price = 3270 + (area-0.8)*5110
7) Price = per block of 1520x1520 microns needed to fit the design in. Adding two blocks together to one block is possible.
8) Price = per block of 1525x1525 microns needed to fit the design in. Adding two blocks together to one block is possible.
9) Price = per block of 1875x1875 microns needed to fit the design in. Adding two blocks together to one block is possible.
10) Minimum charged area = 4 mm^2.
    For area ≤ 4 mm^2, Price = 3200 euro
    For area > 4 mm^2, Price = 3200 + (area-4) * 880
11) Price = per submitted design to be bumped (no size limit, limited to 200 bumps)
12) Price = per block of 1920x1920 microns (designed area – pre-shrink) needed to fit the design in, (on silicon area – after shrink = 1730x1730 microns) – see below
13) Price = per block of 1660x1660 microns needed to fit the design in
14) Price = per block of 2000x2000 microns needed to fit the design in
15) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 13900 euro. For area > 3 mm^2, Price = 13900 + (area-3) * 3800
16) Any edge length between 1.0 mm to 12.5 mm is possible. The mentioned die size is referred to the Pre-Shrink die size
17) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 18500 euro. For area > 4 mm^2, Price = 18500 + (area-4) * 4000
18) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 17850 euro. For area > 3 mm^2, Price = 17850 + (area-3) * 4700
19) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 23750 euro. For area > 4 mm^2, Price = 23750 + (area-4) * 5000
20) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 29100 euro. For area > 3 mm^2, Price = 29100 + (area-3) * 9700
21) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 46800 euro. For area > 4 mm^2, Price = 46800 + (area-4) * 10200
22) Price = per block of 1570x1570 microns (designed area – pre-shrink) needed to fit the design in, (on silicon area – after shrink = 1413x1413 microns) – see below
23) Price = per block of 2500x2500 microns needed to fit the design in
24) Minimum charged area = 3 mm^2. For area ≤ 3 mm^2, Price = 42000 euro. For area > 3 mm^2, Price = 42000 + (area-3) * 14000
25) Minimum charged area = 4 mm^2. For area ≤ 4 mm^2, Price = 65000 euro. For area > 4 mm^2, Price = 65000 + (area-4) * 14700
26) We reserve the right to cancel mini@sic runs if the run is not economically feasible.

UMC 0.18 and 0.13µ mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1525 x 1525 µm
- 2 sub-blocks : design may not be larger than 3240 x 1525 µm
- 3 sub-blocks : design may not be larger than 4960 x 1525 µm
- 4 sub-blocks : design may not be larger than 3240 x 3240 µm
- 6 sub-blocks : design may not be larger than 4960 x 3240 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

UMC 90nm & 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1875 x 1875 µm
- 2 sub-blocks : design may not be larger than 3950 x 1875 µm

TSMC 90nm & 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2000 x 2000 µm
- 2 sub-blocks : design may not be larger than 4000 x 2000 µm

TSMC 40nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1920 x 1920 µm (pre-shrink)
- 2 sub-blocks : design may not be larger than 3840 x 1920 µm
- These are designed dimensions. Fabricated designs (40nm) are shrinked during maskmaking in both X and Y directions by 0.9

TSMC 28nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1570 x 1570 µm (pre-shrink)
- 2 sub-blocks : design may not be larger than 3140 x 1570 µm
- These are designed dimensions. Fabricated designs (28nm) are shrinked during maskmaking in both X and Y directions by 0.9

TSMC 0.18µ CMOS mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1660 x 1660 µm
- 2 sub-blocks : design may not be larger than 3320 x 1660 µm
- 3 sub-blocks : design may not be larger than 4980 x 1660 µm
- 4 sub-blocks : design may not be larger than 3320 x 3320 µm
- 6 sub-blocks : design may not be larger than 4980 x 3320 µm

TSMC 0.18µ HV BCD mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2500 x 2500 µm
- 2 sub-blocks : design may not be larger than 5000 x 2500 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

Contacts
imec, Belgium (P. Malisse, tel: +32 16 281272, e-mail: mpc@imec.be)
Fraunhofer IIS, Germany (W. McKinley, tel : +49 9131 776 4413, e-mail: europrac@iis.fraunhofer.de)