EUROPRACTICE IC SERVICE

European Commission | Horizon 2020 European Union funding for Research & Innovation

2018 *mini*@sic Europractice MPW runs Schedule and Prices

Accessible for universities & research institutes
Version 180112- v3.0

www.europractice-ic.com

mini@sic

Through the *mini***@sic** program the EUROPRACTICE IC Service is offering special MPW prototyping conditions to stimulate Academia and publicly funded Research Institutes to prototype small ASIC designs for education or publicly funded research. Through Multi Project Wafer Services, the high cost of a prototype run (masks and wafers) is shared amongst several customers. However for student education or PhD research programs the minimum prototyping charges are still too high. By introducing the *mini***@sic** concept on MPW runs EUROPRACTICE is offering considerably lower minimum prototyping charges for small ASIC designs. **Academia and Research Institutes will have the possibility to prototype small designs at low prices on selected MPW runs.**

ON Semiconductor	J	F	M	A	M	J	J	A	S	O	N	D
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	15		26			4		13		29		
ON Semi 0.7µ C07M-I2T100 100 V - 2M & 3M options	15		26			4		13		29		
ON Semi 0.35µ C035U 4M (3M & 5M optional) only thick top metal	29			16			2		17			3
ON Semi 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)	2			2			9			9		
ON Semi 0.35µ C035 - I3T50U 50 V 4M - 3M optional (5M on special request)			5		28				3			3
ON Semi 0.35µ C035 - I3T50U (E) 50 V 4M - 3M optional (5M on special request)			5		28				3			3
ON Semi 0.35µ C035 - I3T25U 3.3/25 V 4M (3M & 5M optional) only thick top metal	29			16			2		17			3

	J	F	M	A	M	J	J	A	S	O	N	D
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO					14						19	
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO					14							
ams 0.35µ HV CMOS H35B4D3 120V 4M					2					29		
ams 0.35µ SiGe-BiCMOS S35 4M/4P				9								10
ams 0.30µ A30B4S3 4M/4P Low VT										29		
ams 0.18µ CMOS aC18 6M/1P/MIM/1.8V/5V					14						19	
ams 0.18µ HV CMOS aH18 50V/20V/5V/1.8V/ 6M/MIM					14						19	
Bottom Anti Reflective Coating (BARC) Diode for ams 0.35µ CMOS C35OPTO 4M/2P/5V IO					14						19	
Wafer Level Chip Scale Package for ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO					14						19	

Note: Customers making use of WLSCP have to send in their design gds file two weeks before the indicated deadline
Please be aware of extended lead times for the AMS runs. For more information, please contact the support team at amssup@imec.be

aC18 and aH18 MPW service is limited to ongoing projects and no production on these processes will be supported.

IHP	J	F	M	A	M	J	J	A	S	O	N	D
IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V	19						27					
IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM	19						27			19		
IHP SG25H4 0.25µ SiGe:C Ft/Fmax= 200/220GHz 5M/MIM + optional TSV	19						27					
SG25H4_EPIC high performance BiCMOS technology + photonic design layers				6						19		
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)					25							
IHP SG13S SiGe:C Bipolar/Analog/CMOS/RF-MEMS Ft/Fmax= 250/300GHz 7M/MIM + optional RF-MEMS or TSV			2					17			23	
IHP SG13C SiGe:C CMOS 7M/MIM			2					17			23	
IHP SG13G2 SiGe:C Bipolar/Analog/RF-MEMS Ft/Fmax= 300/500GHz 7M/MIM + optional RF MEMS			2					17			23	
IHP BEOL SG13 (M1 and Metal Layers Above) + optional RF-MEMS or LBE or TSV		16										

Bumping available for all IHP technologies with extra charge, limited to 200 bumps
Important Note: Dates are registration deadlines after which designs cannot enter this MPW run anymore. Final GDSII file must be submitted within 10 days after this date.

X-FAB	J	F	M	A	M	J	J	A	S	O	N	D
XH018 0.18µ HV NVM CMOS E-FLASH *				23						29		
XT018 0.18µ HV SOI CMOS **			12						17			

* Process modules included for 6 metal option : LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO.
** Process modules included for 6 metal option: LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, MET4, METMID, METTHK, HWC

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS General Purpose Logic or MS/RF (MIM: 2.0 fFum2 / UTM: 20kÅ)	15				30				19			
TSMC 0.18 CMOS High Voltage BCD GenII				4						17		
TSMC 65nm CMOS Low Power MS RF (reserve 4 months in advance)		14			16			15			14	
TSMC 40nm CMOS Low Power MS RF			6						5			
TSMC 28nm CMOS HPC RF (reserve 4 months in advance)				25						31		
TSMC 28nm CMOS HPC RF – Micro-block (reserve 4 months in advance)				25						31		

Important Note: read below for 28 nm Micro-block conditions
Note: Dates in red are preliminary and can change after TSMC released the schedule for H2 2018.
*** Contact** eptsmc@imec.be **if any of the following options are used: MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS**

options TSMC mini@sic runs	IO	MIM /um2	special remarks
TSMC 0.18µ CMOS MS/RF	3.3 V	2 fF	Metalscheme: 1P6M_4X1U with UTM (20kA) topmetal
TSMC 0.18 CMOS High Voltage BCD Gen 2 0.18 UM CMOS High Voltage Mixed Signal based General Purpose BCD Dual Gate FSG AL 1P6M [SALICIDE, NBL/PBL EPI, 1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5VV]		2 fF between M5 & M6	Metalscheme: 1P6M_4X1U with UTM (30kA) topmetal
TSMC 65nm CMOS LP MS RF	2.5V (1.8UD, 3.3OD)	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1Z1U_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 40nm CMOS LP MS RF – **No Triple Gate oxide**	2.5V (1.8UD, 3.3OD)	-	Core : 1.1 V, Metal scheme : 1P8M_5X2Z_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 28nm CMOS HPC – High Performance Compact Mobile Computing, RF – also applies for Micro-block	1.8 V	-	Core : 0.9 V, Metal scheme : 1P8M_5X1Z1U UTRDL (28kA thick AP layer) Default: BEOL option 1, 11 mils backlapping

UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L65N Logic/Mixed-Mode/RF - LL			12						3			
UMC L130 Mixed-Mode/RF		12				18				29		
UMC L180 Mixed-Mode/RF		5		23			16			29		

options UMC mini@sic runs	Core	IO	MIM	topmetal	special remarks
UMC L65N Logic/Mixed-Mode-MODE65N/RF - LL - 1P8M1T0F1U - 1.2V/2.5V	1.2	2.5V/2.5V_OD3.3V	2fF	32.5kA	Metal-stack "26"
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	1.2V	3.3V	1fF	20kA	Possible combinations: HS, HS-LL (No SP possible)
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	1.8V	3.3V	1fF	20kA	

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 130nm BCDlite							2				5	
GLOBALFOUNDRIES 55 nm LPe					14							
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave						4						
GLOBALFOUNDRIES 28 nm SLP/SLP-RF					2							
GLOBALFOUNDRIES 22 nm FDSOI			12						17			

Important Note: Dates are registration deadlines after which designs cannot enter this MPW run anymore. Final GDSII file must be submitted within 6 weeks after this date. We reserve the right to cancel mini@sic runs if the run is not economically feasible.
Dates in red are preliminary

2018 *mini*@sic Europractice MPW runs – Pricelist

Accessible for universities, research institutes and companies
Prices and conditions may change at any time without prior notice
Prices valid for runs starting 1 January 2018.

NON-EUROPEAN price applies to all non-European (not belonging to the countries of EUROPEAN price) universities and research institutes who submit designs for **educational or publicly funded research use only.**

EUROPEAN price: only applies to EUROPRACTICE registered (who paid their annual full membership fee) Academic and Research Members from all 28 EU countries and Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine who submit designs for **educational or publicly funded research use only.**

Prices are given for the delivery of unpackaged, untested prototypes. Encapsulation and testing will be charged separately.

Number of prototypes
OnSemi > 20 samples
ams : 40 samples
UMC : 0.18um, 0.13um : 25 samples
UMC : 65nm: 45 samples
IHP : 40 samples SG25 & SG13, 25 samples using RFMEMS switch module, TSV module, PIC, EPIC
XFAB : 15 samples
TSMC : 40 samples for 0.18u, 100 samples for 65, 28nm
GLOBALFOUNDRIES : 50 samples
If you need more prototype samples, please ask for a quotation

Plots
You can order plots/PDF of your designs
- first plot/PDF costs 50 euro
- next plots cost 20 euro each

Packaging : see separate prices and available packages

ALL PRICES IN EURO

ON Semiconductor (formerly AMIS)	STANDARD Price/mm²	DISCOUNTED Price/mm²
ON Semi 0.7µ C07M-D 2M/1P	300 [1]	270 [1]
ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	350 [1]	315 [1]
ON Semi 0.7µ C07M-I2T100 100 V - 2M	525 [1]	485 [1]
ON Semi 0.7µ C07M-I2T100 100 V - 3M	560 [1]	525 [1]
ON Semi 0.35µ C035U 4M (default) including analog options	720 [1]	670 [1]
ON Semi 0.35µ C035U 3M (optional) including analog options	700 [1]	650 [1]
ON Semi 0.35µ C035U 5M (optional) including analog options	800 [1]	750 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 3M	850 [1]	800 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 4M	925 [1]	875 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 5M	1050 [1]	995 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 3M	850 [1]	800 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 4M	925 [1]	875 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 5M	1050 [1]	995 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 3M (optional)	750 [1]	700 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 4M (default)	770 [1]	720 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 5M (optional)	800 [1]	750 [1]

ams	STANDARD Price/mm²	DISCOUNTED Price/mm²
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	640 [1]	580 [1]
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	800 [1]	700 [1]
ams 0.35µ HV CMOS H35B4D3 120V 4M	880 [1]	800 [1]
ams 0.35µ SiGe-BiCMOS S35 4M/4P	880 [1]	800 [1]
ams 0.30µ A30B4S3 4M/4P Low VT	880 [1]	800 [1]
ams 0.18µ CMOS aC18 6M/1P/MIM/1.8V/5V	1100 [1, 2]	1050 [1, 2]
ams 0.18µ HV CMOS aH18 50V/20V/5V/1.8V/ 6M/MIM	1150 [1, 2]	1100 [1, 2]
Bottom Anti Reflective Coating (BARC) Diode for ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	One-off extra fee of 6900	One-off extra fee of 6100
Wafer Level Chip Scale Package for ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	One-off extra fee of 6450	One-off extra fee of 6150

IHP	STANDARD Price/mm²	DISCOUNTED Price/mm²
IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V	2125 [3]	2000 [3, 4]
IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM	3230 [3]	3040 [3, 4]
IHP SG25H4 0.25µ SiGe:C Ft/Fmax= 200/220GHz 5M/MIM	3910 [3]	3680 [3, 4]
SG25H_EPIC high performance BiCMOS technology + photonic design layers	5610 [3]	4620 [3, 4]
IHP SG13G2 SiGe:C Bipolar/Analog Ft/Fmax= 300/500GHz 7M/MIM + optional RF-MEMS	6205 [3]	5110 [3, 4]
IHP SG13S SiGe:C Bipolar/Analog/CMOS Ft/Fmax= 250/300GHz 7M/MIM + optional RF-MEMS or TSV	5355 [3]	4410 [3, 4]
IHP SG13C SiGe:C CMOS 7M/MIM	3825 [3]	2660 [3, 4]
IHP SG25 PIC (Photonics devices, Ge Photo-diode, BEOL)	3230 [3]	2660 [3, 4]
IHP BEOL SG23 (M1 and Metal Layers Above) + optional RF-MEMS or LBE or TSV	850 [3]	800 [3, 4]
IHP SPECIAL SERVICES		
Bumping (available for all IHP techologies)	One-off fee 6500 [8]	One-off fee 4700 [8, 4]
Localized Back side etching (available for all IHP technologies) not offered for EPIC/PIC runs and RF-MEMS	One-off fee 4250 [8]	One-off fee 4250 [8, 4]
TSV to ground (SG25H4/SG13S)	One-off fee 4250 [8]	One-off fee 2500 [8, 4]
RF-MEMS switch for SG13G2 and SG13S (IP)	One-off fee 8500 [8]	One-off fee 2500 [8, 4]

X-FAB	STANDARD Price/block	DISCOUNTED Price/block
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, MET4, METMID, METTHK)	4010 [5]	3700 [5]
X-FAB XT018 0.18µ HV SOI CMOS (MET3, MET4, METMID, METTHK)	4100 [5]	3775 [5]

TSMC	STANDARD Price/block	DISCOUNTED Price/block
TSMC 0.18 CMOS General Logic or MS/RF	3640 [10]	3170 [10]
TSMC 0.18 CMOS High Voltage BCD Gen 2	5140 [17]	4520 [17]
TSMC 65nm CMOS LP MS RF	13310 [11]	12530 [11]
TSMC 40nm CMOS LP MS RF	17890 [9]	16830 [9]
TSMC 28nm CMOS HPC RF	21000 [16]	18490 [16]
TSMC 28nm CMOS HPC RF – Micro-block	12325 [18]	10095 [18]

UMC	STANDARD Price/block	DISCOUNTED Price/block
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	3070 [6]	2570 [6]
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	5020 [6]	4460 [6]
UMC L65N Logic/Mixed-Mode LL	10000 [7]	9400 [7]

GLOBALFOUNDRIES	STANDARD Price: see notes	DISCOUNTED Price: see notes
GLOBALFOUNDRIES 130 nm BCDlite	7125 & 1500 [13, 12]	4400 & 1400 [15, 12]
GLOBALFOUNDRIES 55 nm LPe	21125 & 4000 [13, 12]	18275 & 3800 [14, 12]
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	26938 & 5000 [13, 12]	23163 & 4700 [14, 12]
GLOBALFOUNDRIES 28 nm SLP	53550 & 10200 [13, 12]	46325 & 9700 [14, 12]
GLOBALFOUNDRIES 22 nm FDSOI	72000 & 14000 [13, 12]	60000 & 13200 [14, 12]

Notes

1) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 4 mm^2
2) aC18 and aH18 MPW service is limited to ongoing projects and no production on these processes will be supported.
3) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 0.8 mm^2
4) These discount prices are only available for the **28 EU countries**
5) Price = per block of 1520x1520 microns needed to fit the design in. Adding two blocks together to one block is possible.
6) Price = per block of 1525x1525 microns needed to fit the design in. Adding two blocks together to one block is possible.
7) Price = per block of 1875x1875 microns needed to fit the design in. Adding two blocks together to one block is possible.
8) Price = per submitted design. For bumping (no size limit, limited to 200 bumps)
9) Price = per block of 1920x1920 microns (designed area – pre-shrink) needed to fit the design in, (on silicon area – after shrink = 1730x1730 microns) – see below
10) Price = per block of 1660x1660 microns needed to fit the design in
11) Price = per block of 2000x2000 microns needed to fit the design in
12) Any edge length between 1.0 mm to 12.5 mm is possible. The mentioned die size is referred to the Pre-shrink die size
13) Minimum Block (4.75 mm^2) Price/Price for area > 4.75 mm^2 = Minimum Block Price + (area in mm^2 – 4.75 mm^2) * Price/mm^2
14) Minimum Block (4.25 mm^2) Price/Price for area > 4.25 mm^2 = Minimum Block Price + (area in mm^2 – 4.25 mm^2) * Price/mm^2
15) Minimum Block (3 mm^2) Price/Price for area > 3 mm^2 = Minimum Block Price + (area in mm^2 – 3 mm^2) * Price/mm^2
16) Price = per block of 1570x1570 microns (designed area – pre-shrink) needed to fit the design in, (on silicon area – after shrink = 1413x1413 microns) – see below
17) Price = per block of 2500x2500 microns needed to fit the design in.
18) *Micro-block rules, applicable for TSMC 28nm*:
The Micro-block size is 1110 x 1110 microns (designed area – pre-shrink). On silicon area is 1000 x 1000 microns.
In case the design is larger than the Micro-block size, only option is a miniasic block.
Multiple Micro-blocks are possible on one run.
Micro-block and miniasic reservations/registrations should be done no later than 4 months before the deadline.
Withdrawal of the Micro-block or miniasic block later than one week before the deadline will be subject to a penalty of 50% of the amount due. (*)
In case of Micro-block, there is no commitment that the run will be launched in case of insufficient participations. (**)
In case of miniasic, there is always commitment that the run will be launched.
Combining miniasic and Micro-block on one run is allowed.
(*) *The amount can be recovered at the next participation. In case of 2 subsequent late withdrawals the fee cannot be recovered anymore.*
(**) A graphical picture of the run status will be available per request. An online tool is in preparation and soon online.

UMC 0.18 and 0.13µ mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1525 x 1525 µm
- 2 sub-blocks : design may not be larger than 3240 x 1525 µm
- 3 sub-blocks : design may not be larger than 4960 x 1525 µm
- 4 sub-blocks : design may not be larger than 3240 x 3240 µm
- 6 sub-blocks : design may not be larger than 4960 x 3240 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

UMC 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1875 x 1875 µm
- 2 sub-blocks : design may not be larger than 3950 x 1875 µm

TSMC 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2000 x 2000 µm
- 2 sub-blocks : design may not be larger than 4000 x 2000 µm

TSMC 40nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1920 x 1920 µm (pre-shrink)
- 2 sub-blocks : design may not be larger than 3840 x 1920 µm
- These are designed dimensions. Fabricated designs (40nm) are shrinked during maskmaking in both X and Y directions by 0.9

TSMC 28nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1570 x 1570 µm (pre-shrink)
- 2 sub-blocks : design may not be larger than 3140 x 1570 µm
- These are designed dimensions. Fabricated designs (28nm) are shrinked during maskmaking in both X and Y directions by 0.9
- Micro-blocks

TSMC 0.18µ CMOS mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1660 x 1660 µm
- 2 sub-blocks : design may not be larger than 3320 x 1660 µm
- 3 sub-blocks : design may not be larger than 4980 x 1660 µm
- 4 sub-blocks : design may not be larger than 3320 x 3320 µm
- 6 sub-blocks : design may not be larger than 4980 x 3320 µm

TSMC 0.18µ HV BCD mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2500 x 2500 µm
- 2 sub-blocks : design may not be larger than 5000 x 2500 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

Contacts
imec, Belgium (P. Malisse, tel: +32 16 281272, e-mail: mpc@imec.be)
Fraunhofer IIS, Germany (Thomas Drischel, tel : +49 9131 776 4463, e-mail: europrac@iis.fraunhofer.de)