2019 General Europractice MPW runs Schedule and Prices

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Version 181115– v1.0

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Dear customer,

Please note that indicated dates are **gds-in deadlines for TSMC, UMC, X-Fab, ON Semiconductor, ams technologies, STMicrolectronics**. If you want to participate onto one of below listed MPW runs, please make sure to do your design registration in time to ensure a seat is reserved for you. How many weeks in advance is mentioned in the notes per foundry. For questions, you can send a mail to:

For TSMC technologies : eptsmc@imec.be
For UMC technologies : epumc@imec.be
For X-fab technologies : epxfab@imec.be
For ON Semiconductor technologies : greta.milczanowska@imec.be
For ams technologies :
If your service center is fraunhofer : virtual-asic@iis.fraunhofer.de
If your service center is CMP : cmp@mycmp.fr
For IHP technologies : virtual-asic@iis.fraunhofer.de
For GLOBALFOUNDRIES technologies : virtual-asic@iis.fraunhofer.de
For STMicrolectronics : cmp@mycmp.fr

ON Semiconductor	J	F	M	A	M	J	J	A	S	O	N	D
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	14		25			3		12		28		
ON Semi 0.7µ C07M-I2T100 100 V - 2M & 3M options	14		25			3		12		28		
ON Semi 0.5µ CMOS EEPROM C5F & C5N – 200 mm			4*									
ON Semi 0.35µ C035U - 4M (3M & 5M optional) only thick top metal	28			15			1		16			2
ON Semi 0.35µ C035 - I3T25U 3.3/25 V 4M (3M & 5M optional) only thick top metal	28			15			1		16			2
ON Semi 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)	2			1			8			7		
ON Semi 0.35µ C035 - I3T50U (E) 50 V 4M - 3M optional (5M on special request)			4		27				2			2
ONC18MS (0.18 µm - 1.8/3.3 V - 15V DMOS - 5LM - MiMC - ESD - HiR - EPI)		4		8		10		12		7		9
ONC18MS-LL (=ONC18MS + High Vt)		4		8		10		12		7		9
ONC18HPA (= ONC18MS + DNW + Zener + Stacked MiMC + Native Dev + Schottky)		4		8		10		12		7		9
ONC18-I4T 45/70V HV CMOS (=ONC18MS + 30V + 45V + 70V DMOS)		4		8		10		12		7		9

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 3 weeks in advance.
* ON Semi is experiencing a line load issue for the foreseeable future that pushes out delivery up to 26 weeks

ams	J	F	M	A	M	J	J	A	S	O	N	D
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO		18			13			5			18	
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO					13						18	
ams 0.35µ HV CMOS H35B4D3 120V 4M			5						30			
ams 0.35µ SiGe-BiCMOS S35 4M/4P			18							14		

Important notes:
- Dates are GDS submission deadlines. The design registration has to be done at least 2 weeks in advance.

Do not start new projects with ams technologies. The ams MPW runs are **only available for existing projects**.
Please be aware of extended lead times for the ams runs. For more information, please contact the support team at virtual-asic@iis.fraunhofer.de or cmp@mycmp.fr

IHP	J	F	M	A	M	J	J	A	S	O	N	D
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics				12						18		
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)					24							
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV		22				14		30				
IHP SG13C SiGe:C CMOS 7M/MIM		22				14		30				
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV		22				14		30				
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV			8									

Important notes:
- Dates are registration deadlines. Final GDSII file must be submitted within 10 days after this date.
- Bumping available for all IHP technologies with extra charge, limited to 200 bumps.
- IHP SG25H4 MPW runs available on request for existing projects only. (Contact: virtual-asic@iis.fraunhofer.de for additional information)

X-FAB	J	F	M	A	M	J	J	A	S	O	N	D
XH018 0.18µ HV NVM CMOS E-FLASH	18			23		29				24		
XT018 0.18µ HV SOI CMOS	4		15			7		23			1	
XS018 0.18µ OPTO		27							11			
XP018 0.18µ NVM CMOS		7				20				10		
XH035 0.35µ HV CMOS	11				3			9			8	
XR013					20						18	

options regular runs	Process modules included for 4 metal option	Process modules included for 6 metal option
XH018 0.18µ HV NVM CMOS E-FLASH	LPMOS, MET3, METMID, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO	LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO
XT018 0.18µ HV SOI CMOS	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, METTHK, HWC	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, MET4, METMID, METTHK, HWC
XS018 0.18µ OPTO	MOS3LP, MOSLP, METTHIN, MET3, MET4, MRPOLY, ISOMOS, LVTN3D, BCH, MIM23, PPDB, 4TPIX, SFLATPV	MOS3LP, MOSLP, MET3, MET4, MET5, METMID, MRPOLY, ISOMOS, LVTN3D, BCH, MIM23, PPDB, 4TPIX, SFLATPV
XP018 0.18µ NVM CMOS	LP5MOS, MET3, METMID, MRPOLY, HRPOLY, ISOMOS, LVT, MIM, NVM	LP5MOS, MET3, MET4, METMID, METTHK, MRPOLY, HRPOLY, ISOMOS, LVT, MIM, NVM
XH035 0.35µ HV CMOS	MOS, MOS5A, ISOMOS, HVMOSMID, HRPOLY, MIM, METAL4	Not available
XR013	TBD	TBD

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 2 weeks in advance.

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	30	20	6,27	17,24	8	5,12,26	31	28		2,23	27	
TSMC 0.18 CMOS High Voltage BCD Gen II	9	20,27	27	17	1	5,12	3	7	4	2,30		4
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (8-inch)			13			5		28				4
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (12-inch)	9	13		10	15		10	14		9	13	
TSMC 90nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power	2			17			10			2		
TSMC 65nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (reserve 4 months in advance)	30	20	27	24	22	26	24	28	25	23	27	
TSMC 40nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (no triple gate oxide)	2	6	6	10	1	5	3	7	4	9	6	4
TSMC 28nm CMOS Logic HPL/HPC/HPC+, RF HPL/HPC/HPC+ (reserve 4 months in advance)		6,27		3	1,29		3,31	28		2,30		4

Important notes:
- Dates are GDS submission deadlines. The design registration has to be done at least 4 weeks in advance unless otherwise specified in above table.
- Contact eptsmc@imec.be if any of the following options are used: MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS

* Dates in red are preliminary and can change after TSMC released the schedule for H2 2019.

STMicroelectronics	J	F	M	A	M	J	J	A	S	O	N	D
ST 28nm CMOS28FDSOI	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 55nm BiCMOS055	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 65nm CMOS065	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 130nm BiCMOS9MW	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 130nm H9SOI-FEM	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 130nm HCMOS9GP	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 130nm HCMOS9A	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 0.16µm BCD8sP	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ST 0.16µm BCD8s-SOI	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 4 weeks in advance.

UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L180 Logic GII, Mixed-Mode/RF		4		29			29			7		
UMC L180 EFLASH Logic GII (1)		25					8				11	
UMC CIS180 Image Sensor – CONV/ULTRA diode (1)				8					30			
UMC L130 Logic/Mixed-Mode/RF		18				24					4	
UMC L110AE Logic/Mixed-Mode/RF			11	22			8		9	28		
UMC L65N Logic/Mixed-Mode/RF - LL	2*		4	1*			1*+22		30*		18	
UMC L65N Logic/Mixed-Mode/RF - SP	2*		4	1*			1*+22				18	
UMC 40N Logic/Mixed-Mode – LP		25		29			1		2		18	
UMC 28N Logic/Mixed-Mode – HPC (1)		11			13			12			11	

options regular runs	Core	IO	MIM	topmetal	special remarks
UMC L180 Logic GII	1.8V	3.3V	1fF	8kA - Max. 1P6M	Redistribution and bumping on request
UMC L180 Mixed-Mode/RF	1.8V	3.3V	1fF	8kA/20kA Max. 1P6M	Redistribution and bumping on request.
UMC L180 EFLASH logic GII	1.8V	3.3V	/	8kA - Max. 2P6M	Please get in touch with imec for the EEFLASH macro information.
UMC CIS18 – CONV	1.8V	3.3V	1fF	5kA – Max.1P4M	Colorfilters and microlenses included
UMC CIS18 – ULTRA	1.8V	3.3V	1fF	5kA – Max.2P4M	Colorfilters and microlenses included. Ultra diode is pinned. PIP capacitor possible.
UMC L130 Logic	1.2V	3.3V	1fF/1.5fF/2fF	8kA Max. 1P8M2T	Two types (out of 3) of devices can be combined: HS,LL, SP. Redistr. to Al.
UMC L130 Mixed-Mode/RF	1.2V	3.3V	1fF/1.5fF/2fF	8kA/20kA Max. 1P8M2T	Two types (out of 3) of devices can be combined: HS,LL, SP. Redistr. to Al.
UMC L110AE Logic/Mixed-Mode/RF	1.2V	1.8V/2.5V/3.3V/5V	1fF/1.5fF/2fF	8kA/12kA/20kA/40kA Max. 1P8M	Metalization is Aluminium. 5V device possible! HS,LL,SP can be combined.
UMC L65N Logic/Mixed-Mode/RF - SP	1.0V, 1.1V	1.8V/2.5V/ 2.5V_OD3.3V/3.3V	2fF	8kA/32.5kA Max. 1P10M	Metallization recommendation on request. Redistribution to Aluminium. * = 32kA topmetal, LVT, MIM in development. 2.5V_OD3.3V not available. ** = 3.3V not available. Please check with us before tapeout.
UMC L65N Logic/Mixed-Mode/RF - LL	1.2V	1.8V/2.5V/ 2.5V_OD3.3V/3.3V	2fF	8kA/32.5kA Max. 1P10M	Metallization recommendation on request. Redistribution to Aluminium. * = 32kA topmetal in development. Please check with us before tapeout.
UMC 40N Logic/Mixed-Mode - LP	0.9V	1.8V/2.5V	2fF	8kA/12kA/32.5kA	Metallization recommendation on request. Redistribution to Aluminium.
UMC 28N Logic/Mixed-Mode - HPC	1.0 & 1.1V	1.8V/2.5V	2fF	8kA/12kA/32.5kA	Metallization recommendation on request. Redistribution to Aluminium.

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 3 weeks in advance.

(1) Contact Europractice when planning to participate to those runs.

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 130nm BCDlite	7		11		13		8		9		11	
GLOBALFOUNDRIES 130 nm LP	7		11		13		8		9		11	
GLOBALFOUNDRIES 55 nm LPe		11		15		11		12		14		16
GLOBALFOUNDRIES 55 nm LPx-NVM/LPx-RF		11		15		11		12		14		16
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	2			1			3			1		
GLOBALFOUNDRIES 28 nm SLP/SLP-RF		4			6			5			4	
GLOBALFOUNDRIES 22 nm FDSOI	2		4	29			1		2		4	

Important note: Dates are registration deadlines. Final GDSII file must be submitted within 6 weeks after this date.
* Dates in red are preliminary.

imec	J	F	M	A	M	J	J	A	S	O	N	D
imec Si-Photonics Passives+			27					28				
imec Si-Photonics iSiPP50G		6			22					16		
imec SiN-Photonics BioPIX 300*				1								
imec SiN-Photonics BioPIX 150*§							8					

* imec SiN-Photonics BioPIX: early access runs operated by the H2020-project PIX4Life
*§ imec SiN-Photonics BioPIX 150 MPW run is tentative

CEA-LETI	J	F	M	A	M	J	J	A	S	O	N	D
LETI SiPhotonics Passives	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
LETI SiPhotonics Passives with Heater	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Teledyne Dalsa	J	F	M	A	M	J	J	A	S	O	N	D
Teledyne Dalsa MIDIS	30											

MEMSCAP	J	F	M	A	M	J	J	A	S	O	N	D
PolyMUMPs			26			25			17			16
SOIMUMPs		19			21			21			26	
PiezoMUMPs	15				7			27				

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