EUROPRACTICE IC SERVICE

European Commission | Horizon 2020 European Union funding for Research & Innovation

2019 *mini*@sic Europractice MPW runs Schedule and Prices

Accessible for universities & research institutes
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mini@sic

Through the *mini***@sic** program the EUROPRACTICE IC Service is offering special MPW prototyping conditions to stimulate Academia and publicly funded Research Institutes to prototype small ASIC designs for education or publicly funded research. Through Multi Project Wafer Services, the high cost of a prototype run (masks and wafers) is shared amongst several customers. However for student education or PhD research programs the minimum prototyping charges are still too high. By introducing the *mini***@sic** concept on MPW runs EUROPRACTICE is offering considerably lower minimum prototyping charges for small ASIC designs. **Academia and Research Institutes will have the possibility to prototype small designs at low prices on selected MPW runs.**

ON Semiconductor	J	F	M	A	M	J	J	A	S	O	N	D
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	14		25			3		12		28		
ON Semi 0.7µ C07M-I2T100 100 V - 2M & 3M options	14		25			3		12		28		
ON Semi 0.35µ C035U 4M (3M & 5M optional) only thick top metal	28			15			1		16			2
ON Semi 0.35µ C035 - I3T25U 3.3/25 V 4M (3M & 5M optional) only thick top metal	28			15		2			16			2
ON Semi 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)	2			1			8			7		
ON Semi 0.35µ C035 - I3T50U (E) 50 V 4M - 3M optional (5M on special request)			4		27				2			2

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 3 weeks in advance.

ams	J	F	M	A	M	J	J	A	S	O	N	D
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO		18			13			5			18	
ams 0.35µ HV CMOS H35B4D3 120V 4M			5						30			
ams 0.35µ SiGe-BiCMOS S35 4M/4P			18							14		

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Do not start new projects with ams technologies. The ams MPW runs are **only available for existing projects**.
Please be aware of extended lead times for the ams runs. For more information, please contact the support team at virtual-asic@iis.fraunhofer.de or cmp@mycmp.fr

IHP	J	F	M	A	M	J	J	A	S	O	N	D
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics				12						18		
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)					24							
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV		22			14			30				
IHP SG13C SiGe:C CMOS 7M/MIM		22				14		30				
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV		22				14		30				
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV			8									

Important Note:

- Dates are registration deadlines. DRC clean GDSII file must be submitted within 10 days after this date.
- Bumping available for all IHP technologies with extra charge, limited to 200 bumps.
- IHP SG25H4 MPW runs available on request for existing projects only. (Contact: virtual-asic@iis.fraunhofer.de for additional information).

X-FAB	J	F	M	A	M	J	J	A	S	O	N	D
XH018 0.18µ HV NVM CMOS E-FLASH				23						24		
XT018 0.18µ HV SOI CMOS			15								1	

options regular runs	Process modules included for 6 metal option
XH018 0.18µ HV NVM CMOS E-FLASH	LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO
XT018 0.18µ HV SOI CMOS	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, MET4, METMID, METTHK, HWC

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 2 weeks in advance.

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	23				29				25			
TSMC 0.18 CMOS High Voltage BCD GenII				9						23		
TSMC 65nm CMOS Low Power MS RF (reserve 4 months in advance)		13			15			21			20	
TSMC 40nm CMOS Low Power MS RF				24						2		
TSMC 28nm CMOS HPC RF (reserve 4 months in advance)			27							23		
TSMC 28nm CMOS HPC RF – Micro-block (reserve 4 months in advance)			27							23		

Important notes:
- Dates are GDS submission deadlines. The design registration has to be done at least 4 weeks in advance unless otherwise specified in above table.
- Contact eptsmc@imec.be if any of the following options are used: MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS
- Read below for 28 nm Micro-block conditions

options TSMC mini@sic runs	IO	MIM /um2	special remarks
TSMC 0.18µ CMOS MS/RF	3.3 V	2 fF	Metalscheme: 1P6M_4X1U with UTM (20kA) topmetal
TSMC 0.18 CMOS High Voltage BCD Gen 2 0.18 UM CMOS High Voltage Mixed Signal based General Purpose BCD Dual Gate FSG AL 1P6M [SALICIDE, NBL/PBL EPI, 1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5VV]		2 fF between M5 & M6	Metalscheme: 1P6M_4X1U with UTM (30kA) topmetal
TSMC 65nm CMOS LP MS RF	2.5V (1.8UD, 3.3OD)	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1Z1U_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 40nm CMOS LP MS RF – **No Triple Gate oxide**	2.5V (1.8UD, 3.3OD)	-	Core : 1.1 V, Metal scheme : 1P8M_5X2Z_RDL Default : wirebond with 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 28nm CMOS HPC – High Performance Compact Mobile Computing, RF – also applies for Micro-block	1.8 V	-	Core : 0.9 V, Metal scheme : 1P8M_5X1Z1U UTRDL (28kA thick AP layer) Default: BEOL option 1, 11 mils backlapping

UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L65N Logic/Mixed-Mode/RF - LL		25					15				11	
UMC L130 Mixed-Mode/RF		11				17				28		
UMC L180 Mixed-Mode/RF	28			22			22		30			

options UMC mini@sic runs	Core	IO	MIM	topmetal	special remarks
UMC L65N Logic/Mixed-Mode-MODE65N/RF - LL - 1P8M1T0F1U - 1.2V/2.5V	1.2	2.5V/2.5V_OD3.3V	2fF	32.5kA	Metal-stack "26"
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	1.2V	3.3V	1fF	20kA	Possible combinations: HS, HS-LL (No SP possible)
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	1.8V	3.3V	1fF	20kA	

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 3 weeks in advance.

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 130nm BCDlite			11						9			
GLOBALFOUNDRIES 55 nm LPe		11						12				
GLOBALFOUNDRIES 22 nm FDSOI			4						2			

Important Note:
- Dates are registration deadlines after which designs cannot enter this MPW run anymore. Final GDSII file must be submitted within 6 weeks after this date.
- We reserve the right to cancel mini@sic runs if the run is not economically feasible.

* Dates in red are preliminary.

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