Sales Brochure

Cambridge Consultants ASIC Products

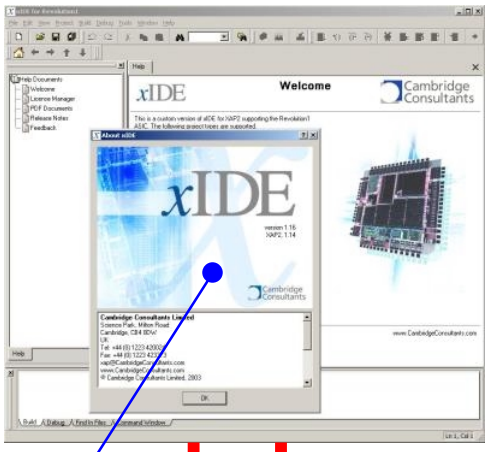
ASIC processors XAP APE

Development tools SIF *x*EMU *x*IDE

These IP blocks and Development Tools have helped Cambridge Consultants and their customers get many mixed analogue-digital SoC ASICs

Right First Time!

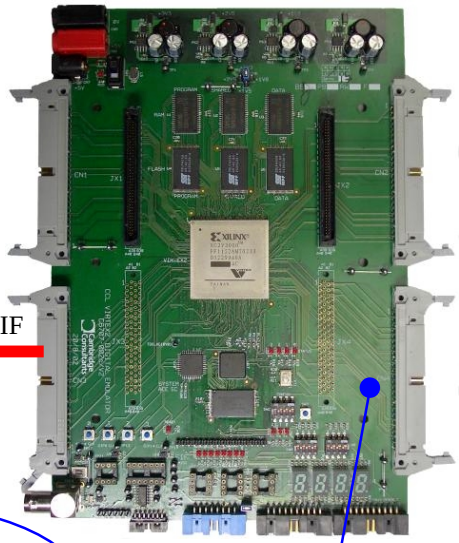
They can help you too…



USB LPT

*x*IDE kernel + custom plugin create a friendly Integrated Development Environment for software on the Final Product or Emulator

SIF



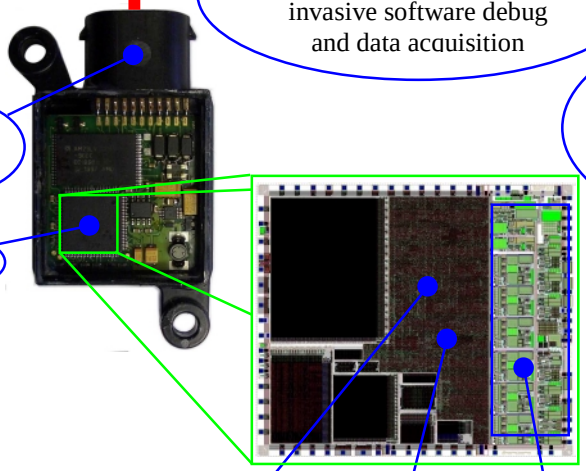
SIF

SIF pods enable high-speed, real-time non-invasive software debug and data acquisition

*x*EMU ASIC Emulator implements all the digital parts of the ASIC (gates, memories) and interfaces to a custom daughter card for all the analogue parts

Final Product

ASIC



XAP C Processor

APE DSP Processor

Analogue IP

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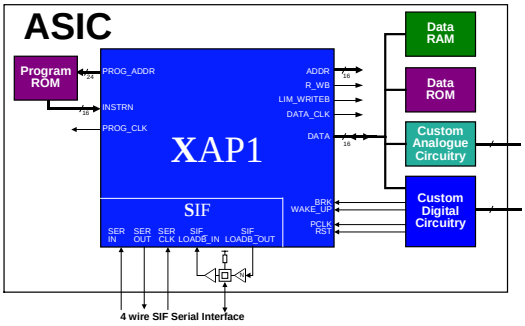
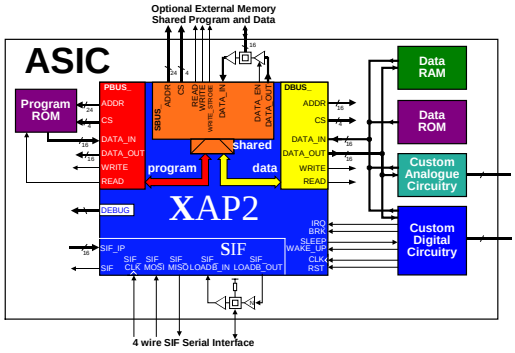
ASIC Processors

XAP family of C processors





Name	Architecture	Release	Gates	Prog. size	Data size	Toolkit
XAP 1	16 bit	1994	3000	64k × 18	64k × 16	*x*IDE for XAP 1
XAP 2	16 bit	1999	12000	16M × 16	64k × 16	*x*IDE for XAP 2
XAP 3	32 bit	2004		64 MB		*x*IDE for XAP 3

All the XAP family processors are optimised for ASIC use. They are low power, low gate count processors that offer high code density, minimising the cost of on-chip and off-chip memories (RAM, ROM, Flash). They come with full software development toolkits based upon *x*IDE. The C compiler, Assembler, Linker, Software Simulator and documentation, are available for a 1 month free trial download from www.cambridgeconsultants.com/asic.

APE DSP Processor

APE2 Customisable DSP Processor

Ideal for the low power, low gate count implementation of DSP algorithms. Has been proved in software radio applications. It is frequently used as a co-processor for the XAP family.

Development Tools

***x*EMU ASIC Emulator**

Contains; large Xilinx FPGA that can emulate up to 300k gates of random logic, 3 4Mbit RAM, 3 4Mbit Flash, JTAG port for configuration, SIF connection for debug and Control, multiple IO ports and daughter card connections. The *x*EMU allows ASIC designs to be precisely emulated at all levels, providing a very high level of confidence in the design before chips are manufactured. It also allows you to see the complete product working with real sensors or radio in a real life test environment.

SIF Serial Interface

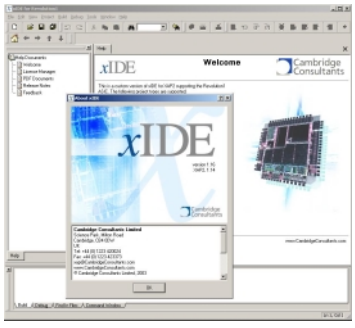
A patented 4 wire Serial interface developed by CCL . It allows non-invasive control and debug. Provides complete access to memory and registers without interfering with the chip operation or timing. It is available with USB or LPT PC interfaces. The Windows drivers enable multiple applications to simultaneously access all memory mapped devices in the ASIC using a single SIF Pod.

***x*IDE Integrated Development Environment**

*x*IDE is an Integrated Development Environment designed with the standard look and feel of IDE packages on the PC. Cambridge Consultants can develop custom plugins for different processors, ASICs and complete products. Plug-in support exists already for the XAP family of C processors and several ASICs created by CCL.

Analogue IP

Cambridge Consultants has an extensive range of analogue building blocks including RF and ADC components that greatly accelerate the design of mixed mode ASICs



References

Cambridge Silicon Radio (www.csr.com) use the XAP2 in all their Bluetooth chips. They also use software toolkits based on *x*IDE for their Bluetooth products.