IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

Title: Study of the non-classical gate layouts for MOSFETs.

Adviser Professor(s): Prof. Salvador Pinillos Gimenez, PhD.

Students involved (names and aimed degrees):

1- (PHD) Rodrigo Alves de Lima Moreto: Analog IC Design by Means Genetic Algorithm (Experimental);
2- (PHD) Denis Rodrigo de Oliveira: FISH MOSFET: : Electrical Characterization and Modeling (Experimental);
3- (PHD) Luis Eduardo Seixas Junior: DIAMOND MOSFET in Radiation Environment (Experimental);
4- (Master) Gabriel Augusto da Silva: POWER PLANAR MOSFET With Non-Conventional MOSFETs (Diamond, Octo, Wave and Fish) (Experimental);
5- (PhD) Vinicius Vono Peruzzi – Study of the devices matching between non-conventional gate geometry MOSFETs.
6- (Scientic Initiation) Luis Fernando Silva – Study of the harmonic distortion of Ellipsoidal MOSFETs.

Institution (University/Faculty): FEI University Center (Centro Universitário da FEI).

Type of Circuit Design: ( ) Digital; ( ) mixed signal; (x) analog; ( ) RF
Date of the circuit tape-out of the run: 2015/05/27, 05/27/2015.
Date of receiving the chips at your institution: 08/27/2015.
Date of the report and/or of later up-date: 02/22/2016.

Short Description of the circuit: (function, proposed innovation, number of transistors, passive components, screen shot of the chip layout, etc):

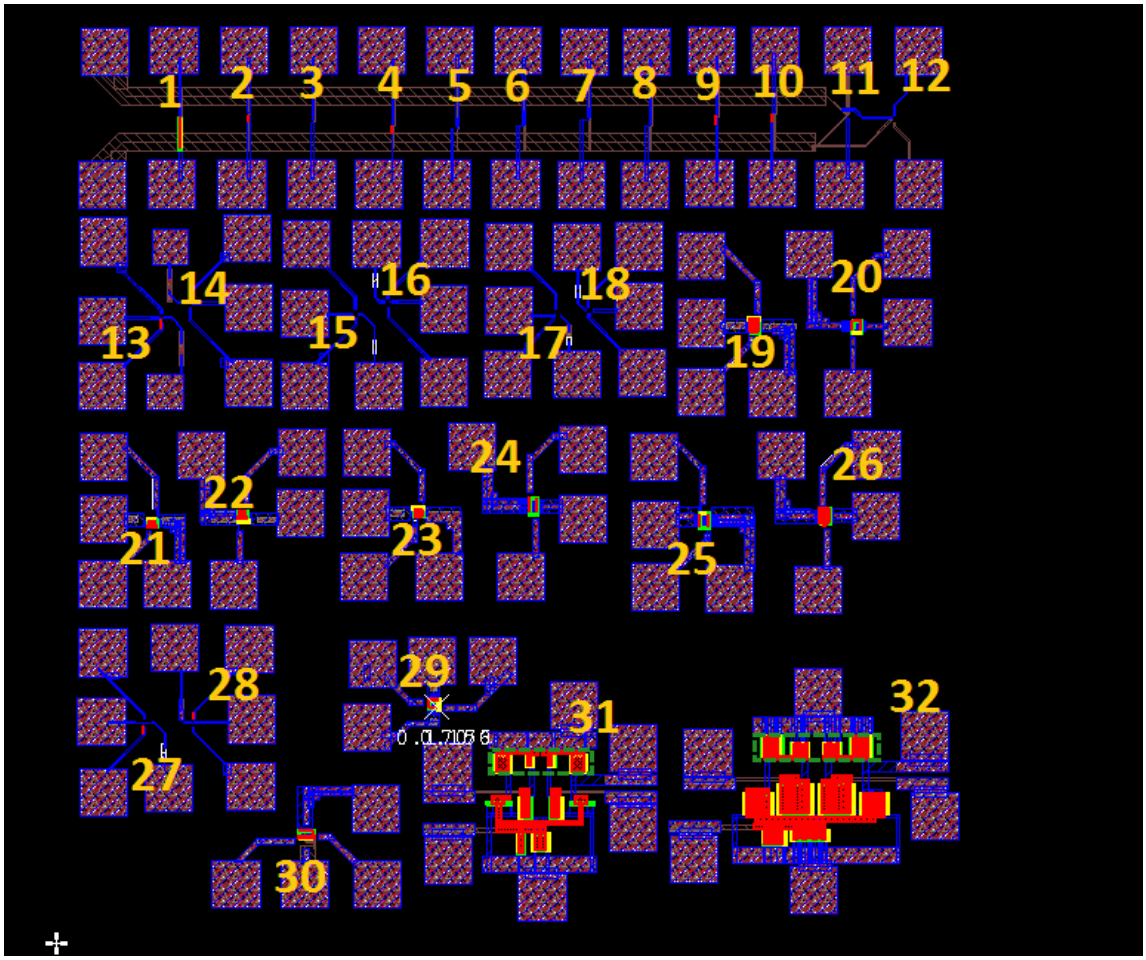
We manufactured several MOSFETs with non-typical gate geometries according to Table 1.

Table 1. Types of MOSFETs non-classical manufactured, their dimensions (W and L are respectively the channel width and length) and pads organization.

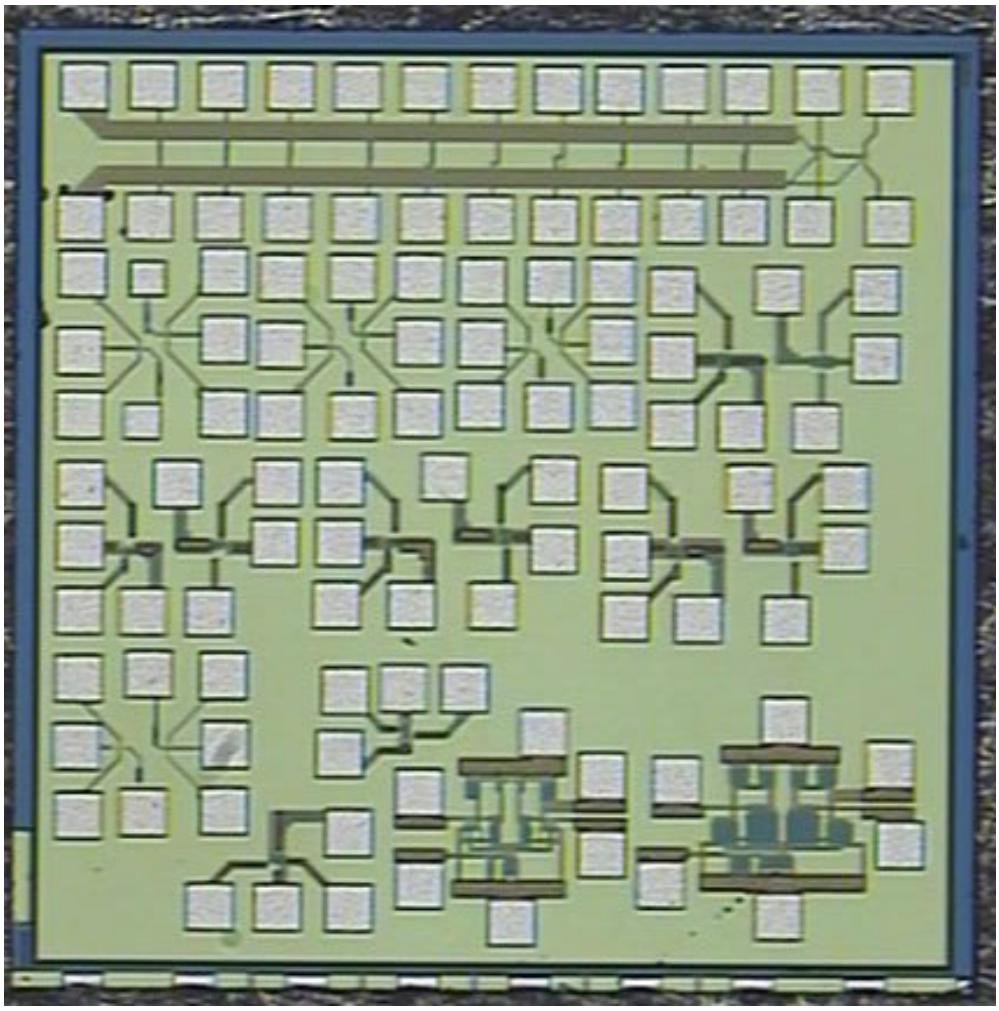
#		W	L	PADs Configuration
1	Unitary Conventional	0.42	0.18	A
2	Unitary Diamond (α=90°)	1.44	0.58	A
3	Unitary OCTO (α=90°, c=25%)	1.44	0.52	A
4	Unitary OCTO (α=90°, c=50%)	1.44	0.41	A
5	Unitary Fish (α=90°)	1.24	0.32	A
6	Unitary Fish (α=135°)	1.18	0.24	A
7	Unitary Fish (α=45°)	1.86	0.55	A
8	Unitary Wave	3.0	0.22	A
9	Unitary Diamond (α=135°)	1.6	0.43	A
10	Unitary Diamond (α=45°)	1.6	1.36	A
11	Unitary Ellipsoidal Annular	3.86	0.26	A
12	Unitary Circular Annular	3.0	0.26	A
13	Rectangular Inverter	5.0	0.18	F
14	Fish Inverter	3.5	0.18	G

15	Rectangular Inverter	5.0	0.4	F
16	Diamond Inverter	4.7	0.4	G
17	Rectangular Inverter	5.0	0.4	F
18	Diamond Inverter	4.7	0.4	G
19	Multifinger Power MOSFET (n-type)	297	0.18	B
20	Ellipsoidal Annular Power MOSFET (n-type)	315	0.26	C
21	Diamante Power MOSFET (α=90°, n-type,)	100	0.58	B
22	Octo Power MOSFET (α=90°, c=25%)	108	0.52	C
23	Octo Power MOSFET (α=90°, c=50%)	116	0.41	B
24	Fish Power MOSFET (α=45°)	172	0.55	C
25	Fish Power MOSFET (α=135°)	286	0.24	B
26	Fish Power MOSFET (α=90°)	294	0.32	C
27	Fish Inverter	4.2	0.18	F
28	Fish Inverter	2.5	0.18	G
29	Circular Annular Power MOSFET	243	0.26	D
30	Wave Power MOSFET	260	0.22	E
31	OTA (Operational Transconductance Amplifier) - Multifinger			
32	OTA(Operational Transconductance Amplifier) - Diamond			

Figure 1 illustrates the manufactured IC layout (Fig. 1a) and its corresponding picture (Fig. 1b).



(a)



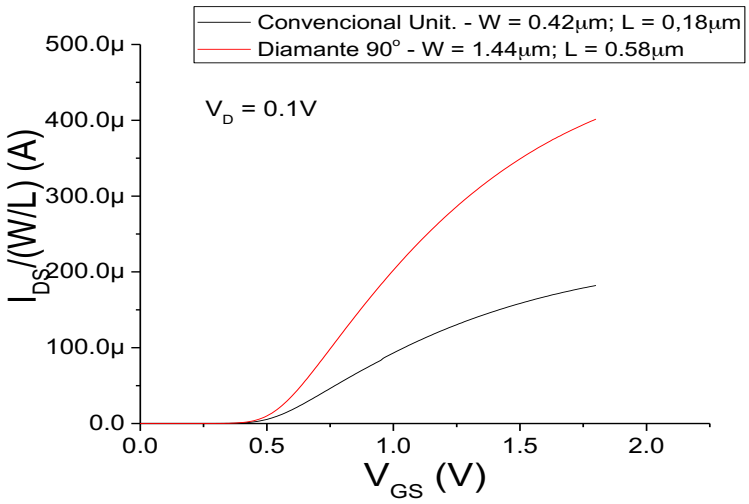
(b)

Figure 1. Layout (a) and picture (b) of the manufactured IC by TSMC, via IMEC.

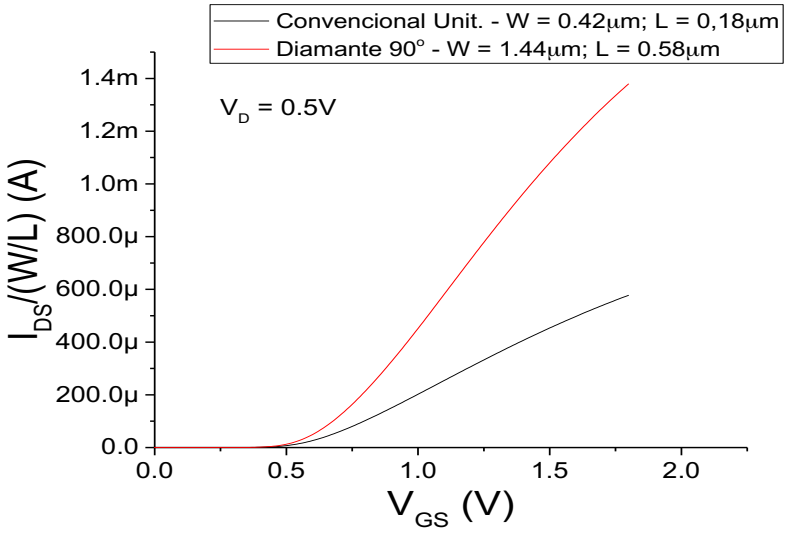
These innovative non-standard MOSFETs (Diamond, Octo, Ellipsoidal, Wave and Fish) will be compared to the classical rectangular ones in order to quantify their better performance, regarding the same gate areas and bias conditions.

Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc:

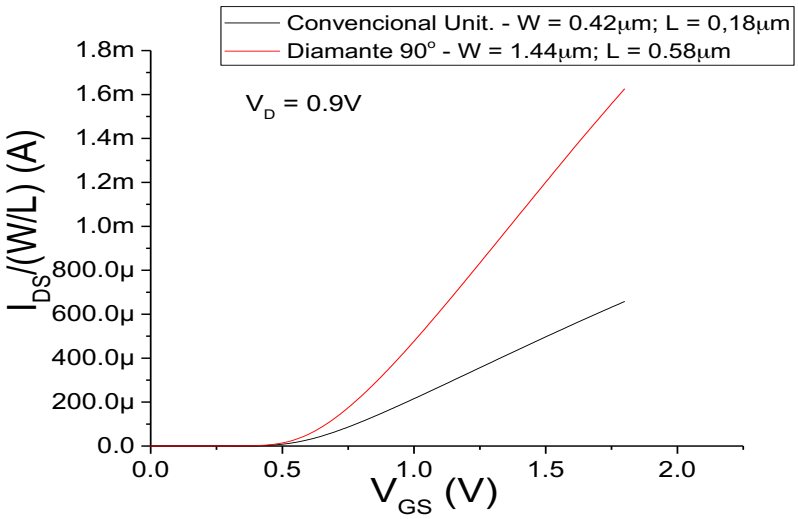
Figure 2 illustrates the comparative experimental curves of the drain current normalized by the aspect ratios [$I_{DS}/(W/L)$] as a function of the V_{GS}, regarding three different drain bias (V_{DS}), of a Diamond (hexagonal gate geometry) MOSFET (DM) and its respective classical rectangular MOSFET (RM), regarding that they present the same gate area (A_G). The MOSFETs threshold voltages (V_{TH}) is approximately 0.55V.


Convencional Unit. - W = 0.42μm; L = 0,18μm
Diamante 90° - W = 1.44μm; L = 0.58μm
V_D = 0.1V
I_DS/(W/L) (A)
500.0μ
400.0μ
300.0μ
200.0μ
100.0μ
0.0
0.0
0.5
1.0
1.5
2.0
V_GS (V)

(a)


Convencional Unit. - W = 0.42μm; L = 0,18μm
Diamante 90° - W = 1.44μm; L = 0.58μm
V_D = 0.5V
I_DS/(W/L) (A)
1.4m
1.2m
1.0m
800.0μ
600.0μ
400.0μ
200.0μ
0.0
0.0
0.5
1.0
1.5
2.0
V_GS (V)

(b)



(c)

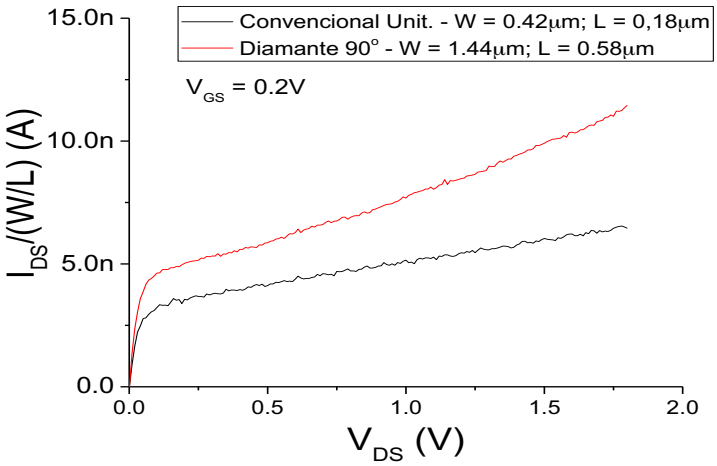
Figure 2. $I_{DS}/(W/L)$ as a function of the V_{GS}, regarding V_{DS} equal to 0.1 V (a), 0.5 V (b), and 0.9 V (c), respectively.

Table 2 presents the MOSFETs $I_{DS}/(W/L)$, and the percentage gains of the DM $I_{DS}/(W/L)$ in relation to the RM counterpart (G_{DM}) in Triode region, considering a V_{GS} equal to 1.5V

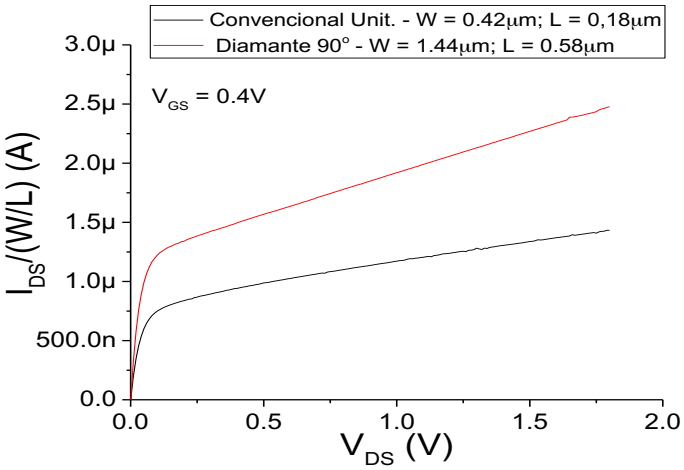
Table 2. $I_{DS}/(W/L)$ of the devices, and the percentage gains of the DM $I_{DS}/(W/L)$ in relation to the RM counterpart (G_{DM}) in Triode region, considering a V_{GS} equal to 1.5V.

	V_{DS} (V)		
	0.1	0.5	0.9
DM (α=90°) $I_{DS}/(W/L)$	349.08μA	1.08mA	1.2mA
RM $I_{DS}/(W/L)$	158.39μA	0.45mA	0.49mA
G_{DM} (%)	120.4	140.0	144.9

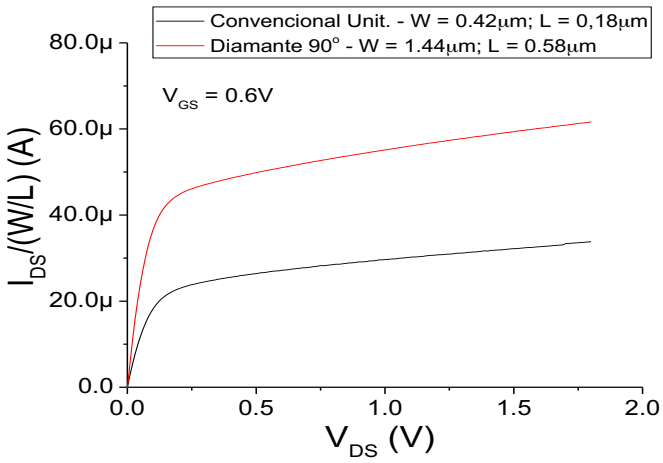
Besides, Figure 3 presents the comparative experimental curves of $I_{DS}/(W/L)$ as a function of the V_{DS} for five different drain bias (V_{GS}), of a DM and its respective RM counterpart, regarding that they present the same gate area (A_G).


Convencional Unit. - W = 0.42μm; L = 0,18μm
Diamante 90° - W = 1.44μm; L = 0.58μm
V_GS = 0.2V
I_DS/(W/L) (A)
15.0n
10.0n
5.0n
0.0
0.0
0.5
1.0
1.5
2.0
V_DS (V)

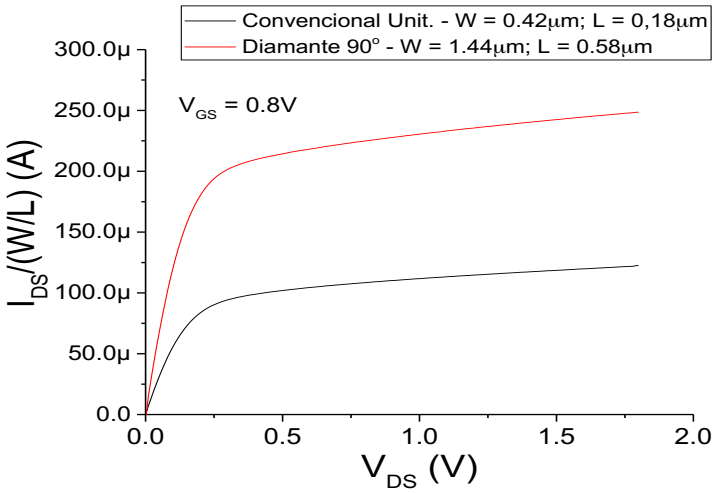
(a)


Convencional Unit. - W = 0.42μm; L = 0,18μm
Diamante 90° - W = 1.44μm; L = 0.58μm
V_GS = 0.4V
I_DS/(W/L) (A)
3.0μ
2.5μ
2.0μ
1.5μ
1.0μ
500.0n
0.0
0.0
0.5
1.0
1.5
2.0
V_DS (V)

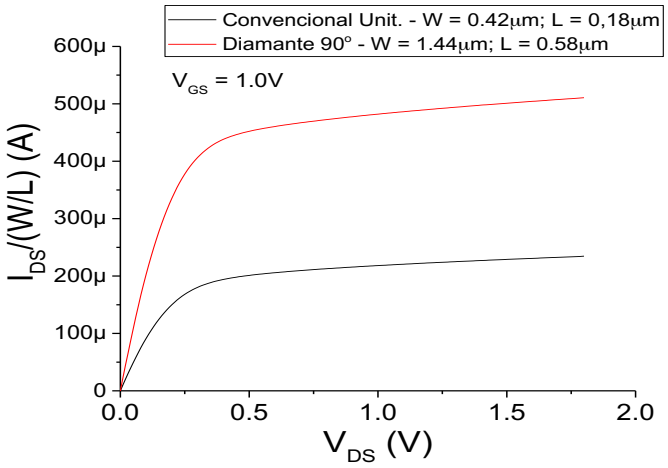
(b)


Convencional Unit. - W = 0.42μm; L = 0,18μm
Diamante 90° - W = 1.44μm; L = 0.58μm
V_GS = 0.6V
I_DS/(W/L) (A)
80.0μ
60.0μ
40.0μ
20.0μ
0.0
0.0
0.5
1.0
1.5
2.0
V_DS (V)

(c)



(d)



(e)

Figure 3. $I_{DS}/(W/L)$ as a function of the V_{DS}, regarding V_{GS} equal to 0.2 V (a), 0.4 V (b), 0.6 V (c), 0.8 V (b), and 01.0 V (c)respectively.

Table 3 presents the saturation $I_{DS}/(W/L)$ of MOSFETs and the percentage gains of the DM $I_{DS}/(W/L)$ in relation to the RM counterpart (G_{DM}), considering a V_{DS} equal to 1.5V.

Table 3. $I_{DS}/(W/L)$ of the devices, and the percentage gains of the DM $I_{DS}/(W/L)$ in relation to the RM counterpart (G_{DM}) for different V_{GS}, in Saturation region, considering a V_{GS} equal to 1.5V.

V_{GS}(V)					
	0.2	0.4	0.6	0.8	1.0
DM (α=90º) $I_{DS}/(W/L)$	9.9nA	2.27µA	59,36µA	242.43µA	501.03µA
RM $I_{DS}/(W/L)$	6.03nA	1.34µA	32.19µA	118.53µA	228.87µA
G_{DM} (%)	64.18	69.4	84.4	104.5	118.91

Based on Tables 1 and 2, we can conclude that the $I_{DS}/(W/L)$ of the DM operating in the Triode and Saturation regions are always higher (Triode region: from 120% to 145%; Saturation region: from 64% to 112%) than those found in the RM counterparts. This can be justified due to the LCE and PAMDLE effects, which are capable of boosting the electrical performance of the MOSFETs. Consequently, this innovative layout style can be used to boost the electrical performance of the analog and digital CMOS ICs applications. Besides, this layout technique can be used in any planar CMOS ICs manufacturing processes and it does not cause any extra financial impact, it is only layout change of the transistor gate geometry.

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit:

We didn't have any difficulty to implement these layouts, thanks the fantastic support of Prof. Jacobus W. Swart and Mr. Tobias Vanderhenst from IMEC. I would really like thank so much them for all support and attention.

Resulting publications (submitted, accepted or published) and degrees earned by students.

Unfortunately, we only received the chips on August 17, 2015, because the chips were sent to me wrongly. In reality, they must be sent to FAPESP. Consequently, I could not use these chips for the scientific initiation, master and PhD students. However, today I have one PhD student and another scientific initiation student performing measurements with these chips. I hope that as soon as possible we will publish these results.