ON-Semiconductor - Tools Technology

The design kits from ON Semiconductor provide customers with a comprehensive suite of libraries enabling efficient design of leading-edge mixed-signal and smart power ASICs. In a nutshell:

- Support of Cadence, Mentor and Synopsys design flows. Tanner tools supported on selected flows through EUROPRACTICE (1)
- Support for Spectre, Eldo and HSPICE analog simulation models (2)
- Full front-end (schematic entry and simulation) and back-end (physical layout) information for the libraries
- ESD robust I/O's (silicon proven)
- Extended temperature range modelling (3)
- Automotive qualified technologies
- Stitching is supported and specific design rules are provided on request

The design kits are developed for RHEL Linux workstations

(1) See Supported Design Tools

(2) Spectre, Eldo and HSPICE models are provided for the ONC18, I4T, I3T25, I3T50 and I3T80. Spectre models are provided for all 0.7µm and 0.5µm technologies as well as for the C035x technologies

(3) The BCD technologies (I2T100, I3T50, I3T80 and I4T) are all qualified for a junction temperature of 200 degrees Celsius. Models supporting this temperature range are also provided. For other technologies, contact your EUROPRACTICE representative

Supported Design Tools

DESIGN KITS	C035	C05	I2T100	I3T25	I3T50	I3T80	ONC18/I4T (*)
Cadence5							
Cadence6 (Open Access)							
Mentor Pyxis							

DESIGN KITS THROUGH PARTNERS	C035	C05	I2T100	I3T25	I3T50	I3T80	ONC18/I4T (*)
Tanner							

SELECTED ASPECTS OF THE DESIGN FLOW	C035	C05	I2T100	I3T25	I3T50	I3T80	ONC18/I4T (*)
Analog Simulation							
Spectre							
Eldo							
HSpice							
mcspice							
verilogA							
Verification: DRC, LVS, ...							
Calibre							
Assura/Diva							
Synopsys digital design flow	(1)	(1)	(1)				

(*) MPW Schedule to be confirmed soon

ON Semiconductor®

Reference Design flow

		Cadence Design kit	Mentor Design kit	Other
ANALOG	Schematic View and Sizing	Virtuoso	Pyxis Schematic Editor	
	Analog simulation	ADE L-XL-GXL Spectre - AP - UltraSim	Pyxis Simulation IC Analyst Eldo - Eldo Premier - Adit	HSPICE
	Analog layout Routing	Virtuoso-XL VSR (CCAR, VCR)	Pyxis DLA iroute - Pyxis Custom Router	
DIGITAL	Digital symbols RTL synthesis Scan insertion Static and Timing Analysis Power Analysis Digital Simulation Formal Verification P&R	Virtuoso Cadence RTL Cadence Incisive Cadence Conformal Encounter	Pyxis schematic and language editor interface Mentor Leonardo Mentor DFT advisor Mentor Questa Mentor Formal Pro Olympus-SOC	Synopsys Design Compiler Explorer Synopsys DFT compiler Synopsys Primetime Synopsys Primepower Synopsys Formality Synopsys IC compiler
	Test ATE	Cadence Encounter Test	Tessent	Synopsys Tetramax
TOP-LEVEL	Symbol Editor	Virtuoso	Pyxis schematic and language editor interface	
	Top-level Simulation Top-level Router	Cadence AMS	Mentor Questa - ADMS Pyxis Custom Router	
VERIFICATION	DRC LVS Robustness Analog parasitic extraction Digital parasitic extraction		Calibre Calibre Calibre PERC Calibre xRC - PEX	Synopsys StarRC