
Activity
Report
2012
EUROPRACTICE
IC SERVICE

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EUROPRACTICE IC service

The right cocktail of ASIC Services

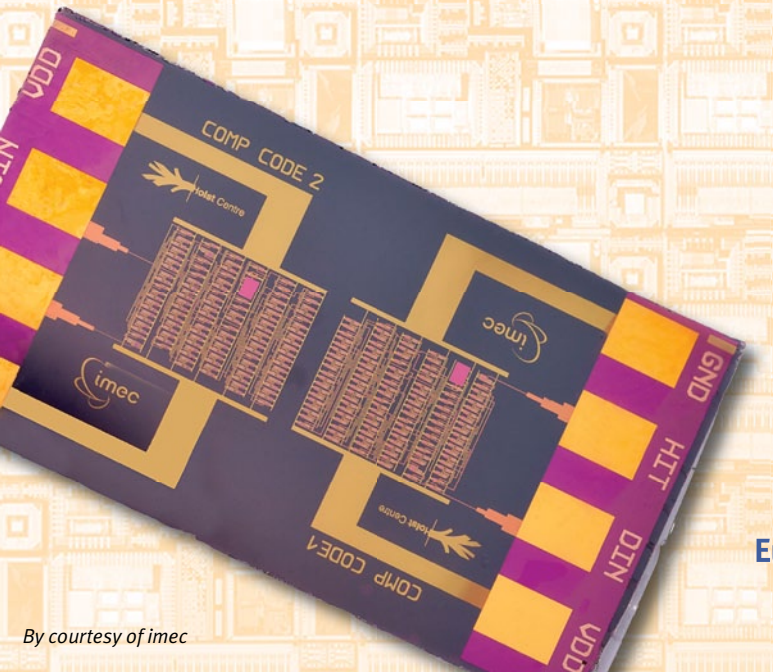
EUROPRACTICE IC Service offers you a proven route to ASICs that features:

- Low-cost ASIC prototyping
- Flexible access to silicon capacity for small and medium volume production quantities
- Partnerships with leading world-class foundries, assembly and testhouses
- Wide choice of IC technologies
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- RTL-to-Layout service for deep-submicron technologies
- Front-end ASIC design through Alliance Partners

Industry is rapidly discovering the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who don't need always the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise that includes IC manufacturing, packaging and test. This you can get all from EUROPRACTICE IC service, a service that is already established for 15 years in the market.

The EUROPRACTICE IC Services are offered by the following centers:

- imec, Leuven (Belgium)
- Fraunhofer-Institut fuer Integrierte Schaltungen (Fraunhofer IIS), Erlangen (Germany)



By courtesy of imec

SEVENTH FRAMEWORK PROGRAMME

The European Commission is funding the Europractice IC Service under the IST programme in the 7th framework.

This funding is exclusively used to support European universities and research laboratories.

Foreword

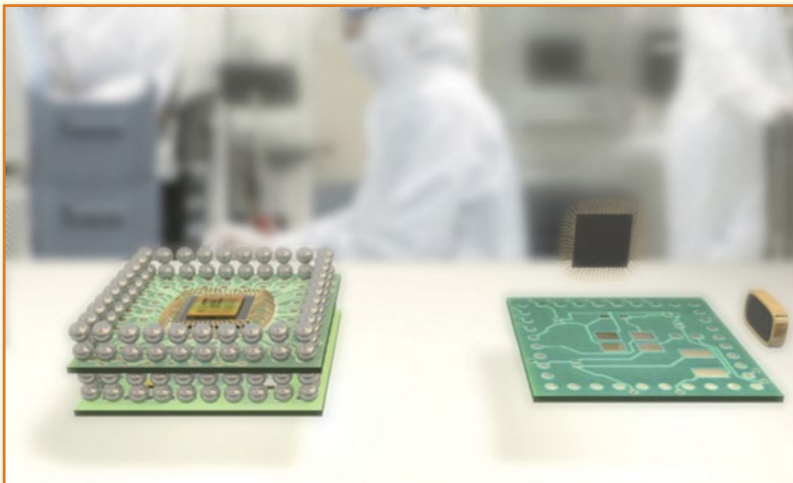
Dear EUROPRACTICE customers,

Again a year has passed, meaning we are offering now the EUROPRACTICE service for 17 years (since 1995) or 23 years including the initial 6 years of stimulating microelectronic design at the European universities and research institutes through EUROCHIP. For most of the professors currently teaching IC and MEMS design affordable access to CAD tools and IC/MEMS prototyping through EUROPRACTICE comes for granted as they have not been involved in the set up in the early years. It certainly does not come for granted. Without the continuous financial support of the European Commission, access would not exist in the form (portfolio of different tools and technologies and prices) we offer it today. In addition the service would not exist without the continuous technical support since all those years of the EUROPRACTICE partners imec, STFC and Fraunhofer. Every year or every two years, the partners have to submit a proposal and negotiate a contract with the European Commission. This most of the time runs very fluently without interruption for the 650 European Europractice members. Europe can be proud of the success of EUROPRACTICE, a pan-European service of CAD access to tools and technologies, allowing collaboration between universities, research institutes and companies using the same tools and technologies, allowing innovation in Europe. It is unique in the world.

In 2012 we signed a new 1.5 year contract with the European Commission to continue to offer our services to the 650 European Academia at favorable prices and allowing again to offer *mini***@sic** MPW runs at discounted prices. In January 2013 we submitted a new proposal to continue the EUROPRACTICE service after 1 July 2013.

Despite the fact that the *mini***@sic** designs decreased considerably in 2012 due to the temporary gap of discounted prices, the total number of designs prototyped is still high (454 designs worldwide). For the first time since our start, the majority of designs is now fabricated in 0.18/0.15 micron technologies.

In 2011 we started to offer integrated MEMS technology based on SiGeMEMS layers on top of standard 0.18µ CMOS integrated circuits. Although this is a promising technology for heterogeneous system integration, the take-up by the Academia was very small (mainly due to the relatively high cost). As a result the offering was not financially viable and EUROPRACTICE has to discontinue this offering in 2013.
Despite this, we continue to look for new MEMS-like and speciality technology offerings.



By courtesy of imec

Finally, I thank you for your continuous support, look forward to future cooperation and hope to meet you at our booths on exhibitions like DATE, DAC, GSA, ...

Sincerely yours,

Dr. C. Das
Chairman EUROPRACTICE IC Service
imec (Belgium)

Table of contents

EUROPRACTICE :

Your Total and Turn-Key ASIC Solution

EUROPRACTICE provides semiconductor and system companies with a total and turn-key ASIC solution including :

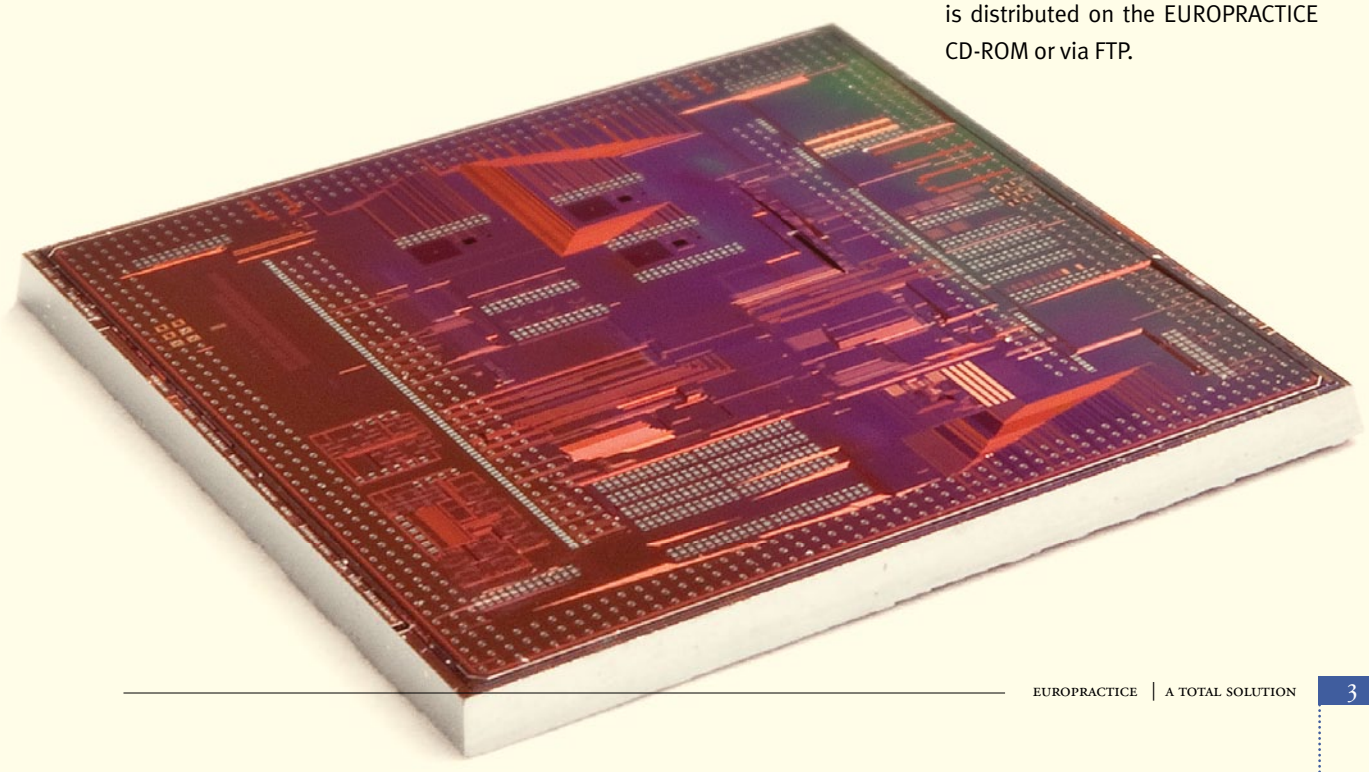
- easy access to foundry design rules, cell libraries and design kits
- deep submicron RTL-to-layout service
- low cost prototype fabrication service
- volume fabrication service including wafer fabrication, packaging and test
- ASIC qualification
- logistics
- technical customer support

New fables startup companies as well as small companies or companies having small ASIC volume products in niche markets experience huge problems to get access to foundries since their volume is too small.

EUROPRACTICE has wafer foundry agreements with different leading suppliers, allowing to offer the most advanced as well as specific technologies to those customers. Our foundry partners acknowledge the EUROPRACTICE Service as the optimal solution to provide wafer capacity to smaller customers. Suppliers see EUROPRACTICE as one big customer representing about 650 universities, research centers and 300 companies world-wide. Through agreements with foundry partners, EUROPRACTICE is able to offer ASIC solutions ranging from a few wafers to thousands of wafers per year.

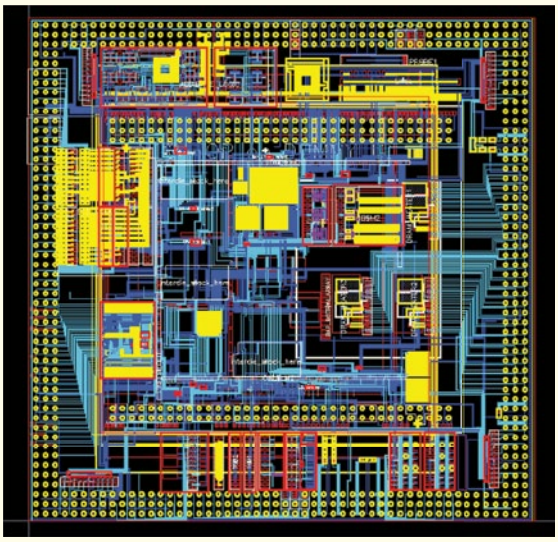
Easy access

Through its agreement with foundries and library partners, EUROPRACTICE is allowed to distribute foundry technology information and cell libraries upon simple signature of a standard Non-Disclosure Agreements or a Design Kit License Agreement. Those agreements can be downloaded from the EUROPRACTICE website. In this way you have access in a few days without having to go through a painful customer qualification procedure at the foundry. Foundry information includes design rules, spice parameters, design & layout manuals and DRC/ERC/LVS decks. Cell library information includes library manuals and design kits for most of the popular CAD tools (Cadence, Synopsys, Mentor Graphics, Tanner, etc.). This foundry and library information is distributed on the EUROPRACTICE CD-ROM or via FTP.



By courtesy of imec

ASIC Design



By courtesy of imec

When customers have received design rules, cell libraries, etc., they can start the ASIC design. ASIC design can be split up into front-end design and back-end design. Front-end design covers ASIC specification feasibility study and design including tasks such as schematic entry, VHDL description, scan insertion, simulation and synthesis. The front-end design can be carried out by the customer himself or can be subcontracted to a design house. During this design phase, Europractice offers technical support on technology, test, type of package, etc. Important know-how and feedback from the test house will be used to improve the DFT (Design For Testability). "State-of-the-art" CAD tools are used during the ASIC design phase.

When the netlist is ready the backend design activity starts including layout generation using state-of-the art layout tools. Deep submicron digital place & route tasks are in most cases not performed by the customers. For those customers that have not their own layout tools, EUROPRACTICE is offering such deep submicron layout service (see deep submicron layout service on page 7). After initial layout, timing verification is carried out by the customer using parasitic layout information and layout is iterated until timing is met. Verification of the design needs to be done in all technology corners.

When layout is finished, a final DRC (Design Rule Check) and LVS (Layout versus Schematic) is performed on the GDS-II database in order to deliver a correct GDS-II to the foundry for manufacturing.

By courtesy of imec

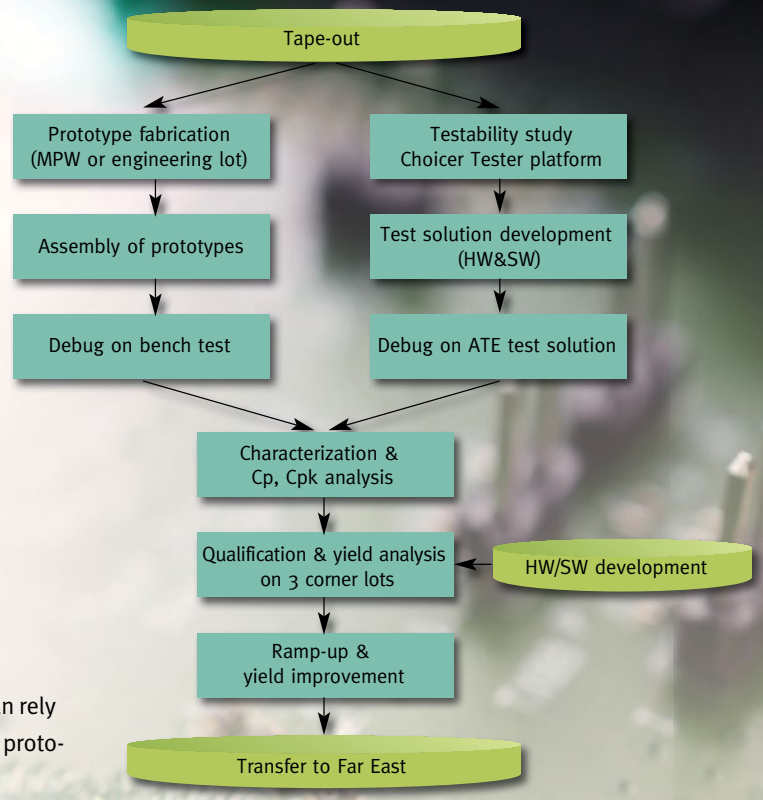
Backend Operation Services through cooperation with certified partners

A history of more than 25 years offering programs to microelectronics industry and academia endorse Europractice as the key partner to your ASIC's success. We embrace COT and turnkey business models to adapt to your requirements with a maximum level of transparency and flexibility. Side by side with world class partners and our long term agreements, Europractice boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.

Through these collaborative agreements our customers can benefit of working with highly recognized chip industry players. The most relevant companies involved in our semiconductor supply chain are listed below:

- **Foundry partners:**
  TSMC, UMC, ON Semi, ams, IHP, LFoundry
- **Ceramic assembly partners:**
  HCM, Systrel, Optocap, Kyocera
- **Plastic assembly partners:**
  ASE, Kyocera, Unisem
- **Wafer bumping partner:**
  Pactech, ASE
- **Test partners:**
  ASE, Microtest, Delta, Rood Technology and Blue test
- **Failure analysis:**
  Maser Engineering
- **Library partners:**
  Faraday, ARM

From prototypes to initial volumes



Thanks to our 25 years of experience, the client can rely on the Europractice service to bring the ASIC from prototype stage to full production stage.

Prototype fabrication

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. Europractice will produce the first prototypes for the customer and organize the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

Development of a test solution

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program.
The devices can be tested on both wafer level as well on packaged devices. The goal is to reduce the test time and to test the ASIC for manufacturing problems using the ATPG and functional patterns.
Europractice will support you during the development of single site test solution as well as with a multi-site test solution when high volume testing is required. Based on the test strategy followed diverse type of implementations can be realized.

Debug and characterization

Before going into production a characterization test program will check if all the ASIC specifications are met according to the customer expectations. Threshold values are defined for each tested parameter. The software will test all different IP blocks and the results will be verified with the bench test results.
A characterization at Low (LT), Room (RT) and High (HT) temperature will be performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

Qualification

When the silicon is proven to be strong against process variations, the product qualification can start. Europractice can support you through the full qualification process using different kind of qualification flows ranging from Consumer, Industrial, Medical to Space according to the Military, Jedec and ESCC standards....
In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

By courtesy of imec

Lot Acceptance tests

- Pre-cap inspection
- Destructive Physical Analysis (DPA)
- Electrical screening
- External and Internal visual inspection
- Cross sectioning: SEM
- Radiation tests (Tid, SEE)

Mechanical Acceptance tests

- Bond pull, Die shear
- Solderability
- Gross & Fine leakage tests
- PIND
- Marking resistance
- Mechanical shock
- Constant acceleration
- Vibration tests

Environmental tests

- Pre-conditioning
- TCT
- HTS
- HAST
- Autoclave, unbiased

Qualification tests

- Static or dynamic burn-in
- Operating life tests (HTOL)
- ESD & LU tests

Failure Analysis

- Non-destructive analysis: X-ray, SAM
- Electrical Failure analysis: Photo Emission Microscopy, probing, OBIRCH
- Physical analysis: SEM, TEM, FIB

From initial volumes to full production

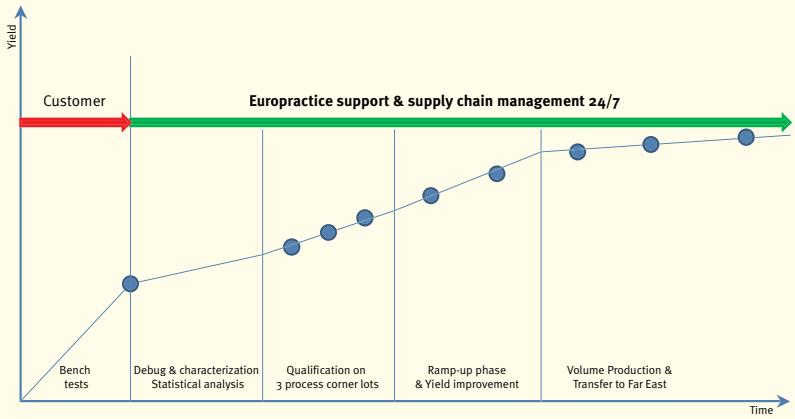
Supply chain management

Europractice is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.
Customer products are treated internally as projects and followed closely by the imec engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. Europratice therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

Yield improvement

Europractice can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the qualification of the device on 3 different corner lots, Europractice can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers will be analyzed to check for yield issues related to assembly or wafer production. Europractice is using the well proven tool Examinator™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.

From protype to production
Keeping cost under control



Europractice supports you from production ramp up till volume production taking into account global project costs. In cases of certain high volume in test is achieved, we are able to transfer the production test solution to Far East. The replicated test solutions are developed in close relationship with the Far East test houses to be fully compliant with their tester platforms.

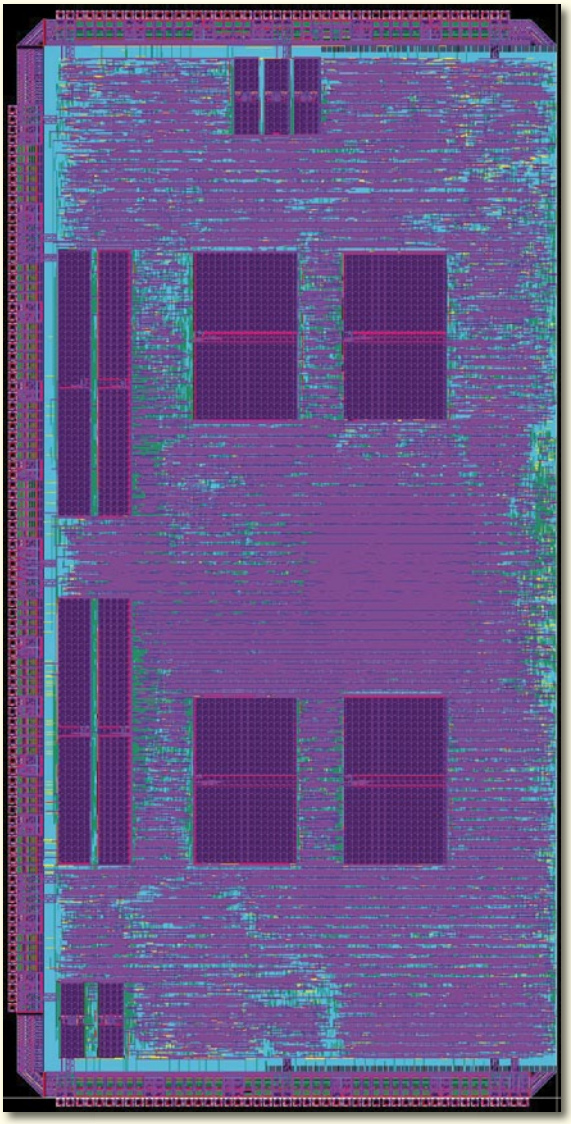
EUROPRACTICE offers deep submicron design support service

Synthesis and layout of deep submicron chips is not straightforward. You need a highly trained team of engineers equipped with expensive state-of-the art EDA tools to tape out first time right Silicon. The chips are growing in size while the technology dimensions are getting smaller and power specifications are becoming more stringent. Because of this, chip designers have to understand how to tackle issues like: hierarchical layout, clock skew, latencies of interacting clock domains, IR-drop on the power distribution, electro-migration and signal integrity, handling many metal layers in the back-end, incorporating IP blocks in the design, on-chip variation, design for packaging, design for manufacturing... And the list goes on.

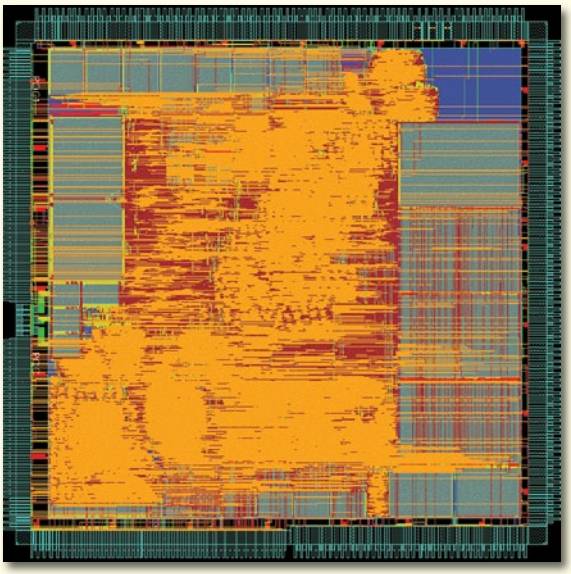
Supporting high-level system designers on the road to tapeout, EUROPRACTICE IC Service provides a physical design support service starting from RTL code in VHDL or Verilog or from a synthesized netlist.

The service supports the whole back-end design flow including synthesis, floorplanning, deep-submicron place and route and multi-mode multi-corner optimization, timing analysis, extraction, scan and BIST insertion and ATPG, tape-out preparation, etc. The service is equipped with state-of-the art tools from the major EDA vendors and has already supported technologies from many different foundries down to 28nm.

Many circuits were successfully taped out for in-house developed Systems-On-a-Chip as well as for ASICs developed by companies, design houses, research institutes and universities. These circuits included a.o. analog full custom blocks, memory macro's from different vendors, special I/O cells and RTL level (soft and firm) IP. The team is well versed in low-power techniques as well as the state-of-the art power format descriptions (CPF/UPF). Interrelated gated clock domains, power shut-off, multi supply-voltage and backbiasing have been successfully implemented.



XentiumDARE: System-on-Chip integrating Recore(NL)'s DSP and NoC based on imec's radiation hardened DARE library cells. (By courtesy of imec)



ASIC for an industrial cryptography application. (By courtesy of imec)

Low cost IC prototyping

The cost of producing a new ASIC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. This is largely due to the NRE (Non-Recurring Engineering) overheads associated with design, manufacturing and test.

EUROPRACTICE has reduced the NRE, especially for ASIC prototyping, by two techniques:

(i) Multi Project Wafer Runs or
(ii) Multi Level Masks.

Multi Project Wafer Runs

By combining several designs from different customers onto one mask set and prototype run, known as Multi Project Wafer (MPW) runs, the high NRE costs of a mask set is shared among the participating customers.
Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full prototyping wafer run. A limited number of tested or untested ASIC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time".

In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.
EUROPRACTICE is organising about 200 MPW runs per year in various technologies.

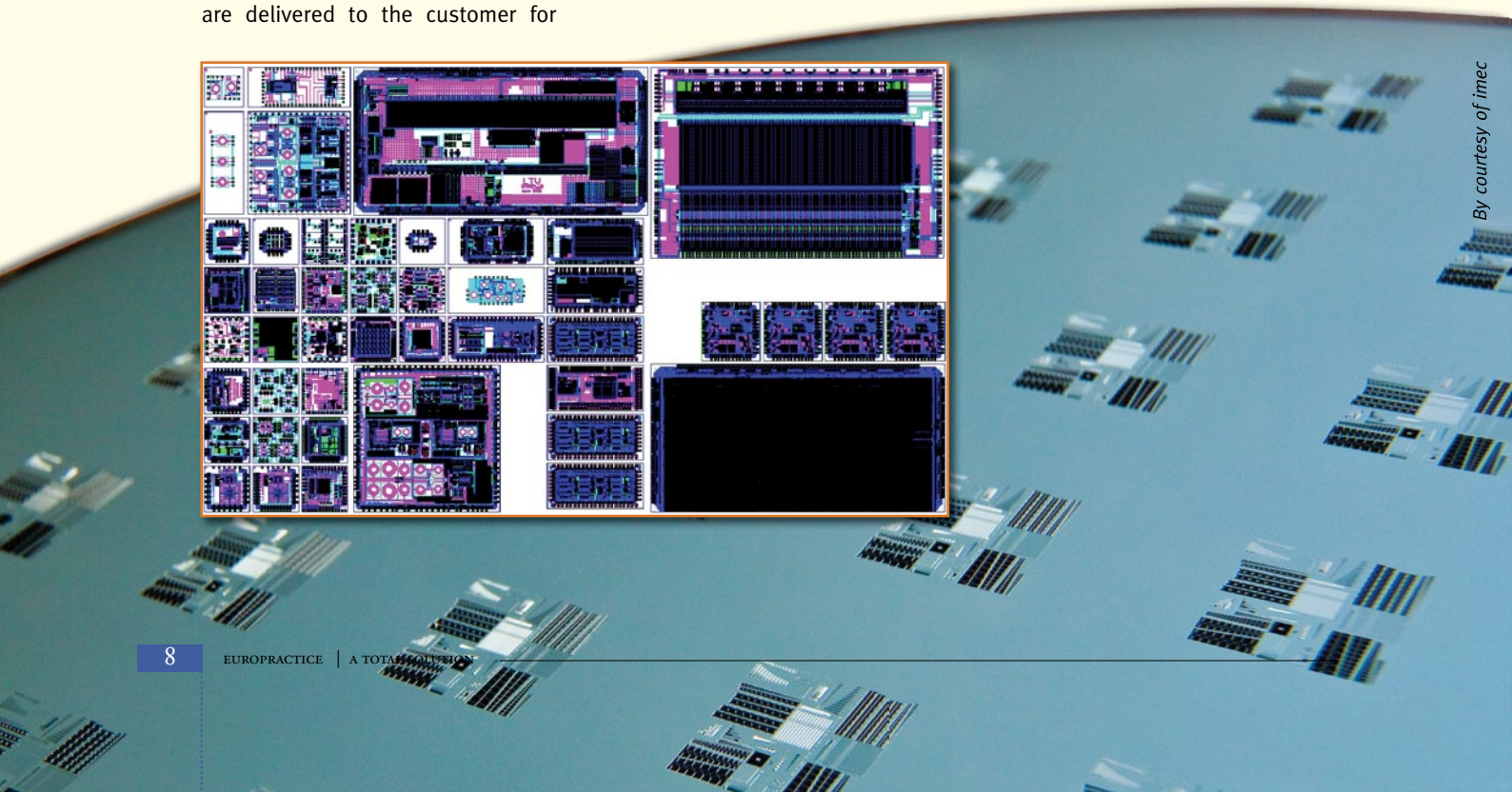
Multi Level Mask Single User Runs

Another technique to reduce the high mask costs is called Multi Level Mask (MLM). With this technique the available mask area (20 mm x 20 mm field) is typically divided in four quadrants (4L/R : four layer per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is thus reduced by a factor of four. By adapting the lithographical procedure it is possible to use one mask four times for the different layers by using the appropriate quadrants. Using this technique the mask costs can be reduced by about 60%.

The advantages of using MLM single user runs are : (i) lower mask costs, (ii) can be started any date and not restricted to scheduled MPW runs, (iii) single user and (iv) customer receives minimal a few wafers, so a few hundreds of prototypes.

This technique is preferred over MPW runs when the chip area becomes large and when the customer wants to get a higher number of prototypes or preserie. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.

This technique is only available for technologies from ON Semiconductor, IHP, LFoundry and TSMC. ■



By courtesy of imec

Technologies

For 2013, EUROPRACTICE has extended its technology portfolio.
Currently customers can have access to prototype and production fabrication in the following technologies :

- AMIS 0.7µ C07M-D 2M/1P & AMIS 0.7µ C07M-A 2M/1P/PdiffC/HR
- AMIS 0.5µ C05M-D 3M/1P & AMIS 0.5µ C05M-A 3M/2P/HR
- AMIS 0.5µ CMOS EEPROM C5F & C5N
- AMIS 0.35µ C035M-D 5M/1P & AMIS 0.35µ C035M-A 5M/2P/HR
- AMIS 0.35µ C035U 4M (3M & 5M optional) only thick top metal
- AMIS 0.7µ C07M-I2T100 100 V - 2M & 3M options
- AMIS 0.7µ C07M-I2T30 & I2T30E 30 V - 2M & 3M options
- AMIS 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)
- AMIS 0.35µ C035 - I3T50 50 V 4M - 3M optional (5M on special request)
- AMIS 0.35µ C035 - I3T25 3.3/25 V 4M (3M & 5M optional) only thick top metal
- ams 0.35µ CMOS C35B3C3 3M/2P/HR/5V IO
- ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO
- ams 0.35µ CMOS C35OPTO 4M/2P/5V IO
- ams 0.35µ HV CMOS H35 120V 3M & 4M
- ams 0.35µ SiGe-BiCMOS S35 4M/4P
- ams 0.18µ CMOS C18 6M/1P/MIM/1.8V/5V
- ams 0.18µ HV CMOS H18 6M/50V/20V/5V/1.8V/MIM
- IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V
- IHP SGB25VGD 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V + RF HV-LDMOS GD-Module 22V
- IHP SG25H1 0.25µ SiGe:C Ft/Fmax=190GHz/220GHz 5M/MIM
- IHP SG25H3P 0.25µ Complementary SiGe:C Ft/Fmax (npn)110/180GHz / (pnp) 90/120GHz 5M/MIM
- IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM
- IHP SG13S SiGe:C Bipolar/Analog/CMOS Ft/Fmax= 250/300GHz 7M/MIM
- IHP SG13C SiGe:C CMOS 7M/MIM
- IHP SG13G2 SiGe:C Bipolar/Analog Ft/Fmax= 300/500GHz 7M/MIM
- IHP BEOL SG25 + RF-MEMS + LBE (M1 and Metal Layers Above)
- IHP BEOL SG13 + LBE + Cu (M1 and Metal Layers Above)
- TSMC 0.25µ CMOS General LOGIC, MS or MS RF
- TSMC 0.18µ CMOS General LOGIC, MS or MS RF (MIM: 1.0 or 2.0 fF/um2 / UTM: 20kÅ)
- TSMC 0.18µ CMOS High Voltage Mixed-Signal (CV018LD 1.8/3.3/32V)
- TSMC 0.13µ CMOS General LOGIC, MS or MS RF (8-inch)
- TSMC 0.13µ CMOS General LOGIC, MS or MS RF (12-inch)
- TSMC 90nm CMOS General or LP Logic, MS or MS/RF (12-inch)
- TSMC 65nm CMOS General or LP MS/RF
- TSMC 40nm CMOS General or LP MS/RF
- UMC L180 Logic GII
- UMC L180 Mixed-Mode/RF
- UMC L180 Low Leakage
- UMC L180 EFLASH Logic GII
- UMC CIS18 - Image Sensor - 1P4M – CONV Diode
- UMC CIS18 - Image Sensor - 2P4M – ULTRA Diode
- UMC L130 Logic
- UMC L130 Mixed-Mode/RF
- UMC L110AE Logic/Mixed-Mode/RF
- UMC L90N Logic/Mixed-Mode/RF
- UMC L65N Logic/Mixed-Mode/RF - LL
- UMC L65N Logic/Mixed-Mode/RF - SP
- MEMSCAP METALMUMPS
- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- ePIXfab-imec SiPhotonics Passives
- ePIXfab-imec SiPhotonics Full Platform
- LFoundry LF150 0.15µ CMOS RF Standard & Low Leakage 1P6M + Thick Metal 1.8V/3.3V MIM

mini@sic prototyping conditions

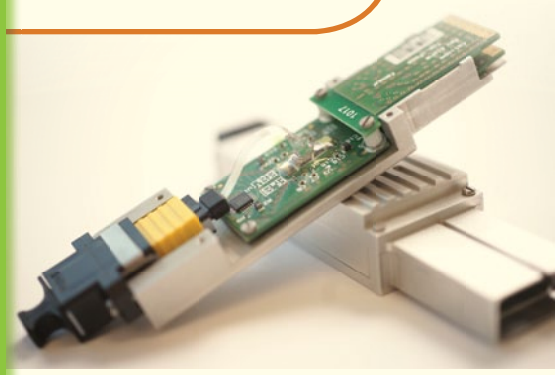
for universities and research laboratories

Prototyping costs have been increasing with scaled technologies due to high mask costs. Even on MPW runs with shared costs, the minimum prototyping fee (corresponding to a minimum chip area) is high for advanced technologies such as 90, 65 and 40nm.

In order to stimulate universities and research institutes to prototype small ASIC designs, Europractice has introduced in 2003 the concept of **mini***@sic*.

That means that Europractice has selected several MPW runs on selected technologies on which universities and research institutes have the opportunity to prototype very small ASIC designs at a highly reduced minimum prototype fee. The minimum charged chip area is highly reduced.

Through the **mini***@sic* concept, the price is reduced considerably. For the most advanced technologies however, the prototyping fee is further reduced through extra funding by the European Commission through the Europractice project (only for European universities and research institutes).



By courtesy of imec

Space Qualification according to ESCC9000

During 25 years, Europractice built up a lot of experience for space qualification. Following the ESCC 9000 standard, the service is providing full support to get your product qualified and ready for flight model. Always pushing the limits of the technology the Europractice is the solution to launch your ASIC to space.

From the start of the project, Europractice provides consulting on the ASIC die pad layout taking into account the parasitics of the full package. Afterwards, if necessary, a dedicated package for your ASIC will be manufactured. The expertise of Europractice together with the professionalism of our partners result in a solution that will fit your space requirements.

In order to increase the yield after packaging, Europractice provides their customers with wafer probing prior before to assembly. All ASIC's are assigned to a unique number at wafer level. Taking this approach Europractice is able to provide full traceability of all the components.

When the ASIC's are ready to be assembled into the package, a pre-cap inspection is done. This step is in close cooperation with the customer, our partners and the experts of the Europractice service.

Before chart F4 of the qualification is performed, Europractice will check if the lot can be accepted by performing the "Lot Acceptance Test". This Lot Acceptance Test includes data analysis of the wafers and radiation tests. The radiation tests include the total dose steady-state irradiation (Tid) and single event effect test (SEE).

Over the years, imec, together with its partner Microtest developed, a portable test system called Hatina. This portable tester enables imec to perform a complete measurement and data log of the devices while performing radiation tests. These real-time measurements provide the customer with an in-depth understanding how the ASIC will behave in space.

By courtesy of Microtest – Hatina ATE

When passing radiation tests, all the remaining parts will enter the chart F3 for screening and will continue from there to chart F4 for qualification. Working with different partners enables imec to implement in their supply chain a significant amount of quality assurance gates (QA gates). Imec has built up huge experience in logistics and an internally developed tool keeps track of the status of all devices.

In order to assess the operating life time of a device, a dedicated burn-in oven was developed. This oven has the ability to heat your ASIC up to the desired temperature, while the auxiliary components are still at room temperature. This makes sure that when a fail is detected, the customer knows that this is related to the device and not to one of the auxiliary components. During the operating life all devices are monitored and all data is written to a log file. Finally a "Qualification report" is delivered together with the ASIC's (flight models) which contain all the data of each device.

WEB site

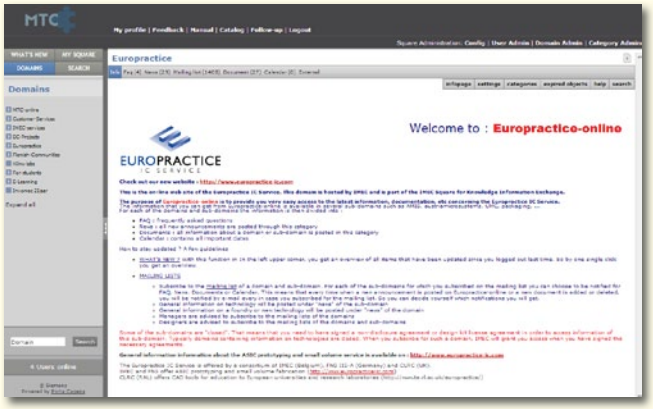
http://www.europractice-ic.com

The Europractice web site for IC prototyping has been totally renewed and provides full information such as:

- Technologies
- Specification sheets
- Available and supported cell libraries and design kits
- MPW runs
- MPW prices
- Small volume possibilities
- Deep submicron netlist-to-layout service
- Procedures for registration of designs for prototyping
- Etc.

Europractice-online

http://www.europractice-online.be



In 2003 Europractice introduced "Europractice-online", a platform for information exchange. This platform is hosted by imec's Microelectronics Training Center.

Users can register to access information available on Europractice-online. The information that is available is grouped per technology and contains:

- Public information
- Confidential information in 'closed' domains, accessible after signature of Non-Disclosure Agreement or Design Kit License Agreement
- News flashes
- Frequently Asked Questions
- Mailing lists

The user can personalize the mailing lists in such a way that he is automatically informed by e-mail whenever a new document is posted, news is posted, FAQ is posted, etc. The user can choose for which technologies he will be notified. As such managers can select to be informed on latest news, whereas designers can ask to be notified on all new items for a specific technology.

Results

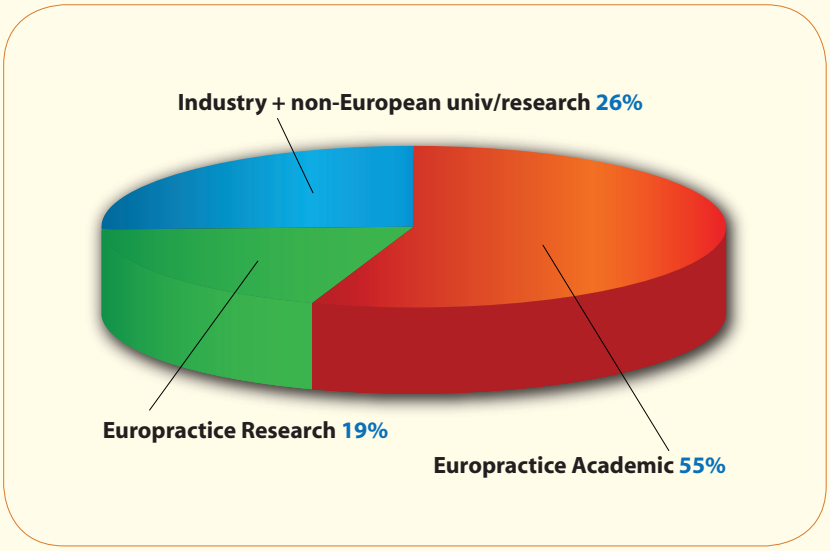
MPW prototyping service

ASICs prototyped on MPW runs

In 2012, a total of 545 ASICs have been prototyped.
74% of the designs are sent in by European universities and research laboratories while the remaining 26% of the designs is being sent in by non-European universities and companies world-wide.

Geometry mix

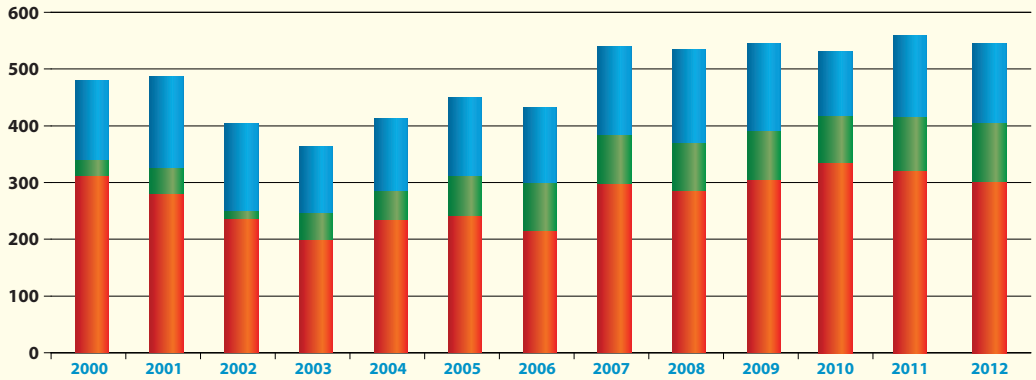
Year over year we see a shift towards newest technologies. Also in 2012 the same trend is shown. For the first time, the majority of designs is done in 0.18µ / 0.15µ technology (32%). Also the number of designs in 65nm technology has taken up.



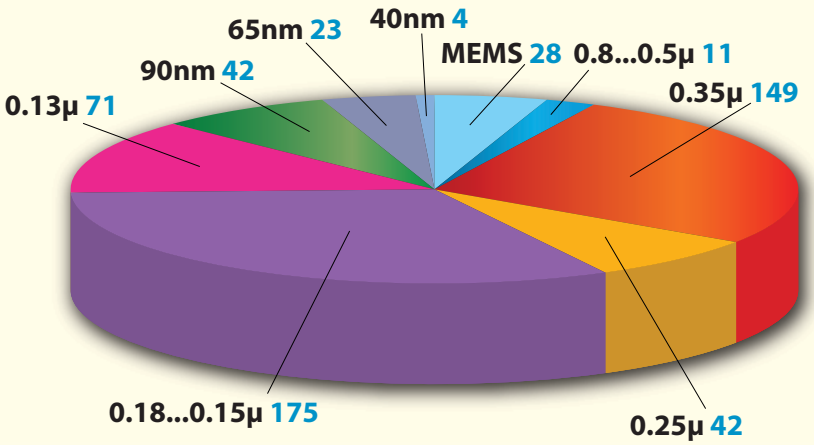
MPW designs in 2012

mini@sic

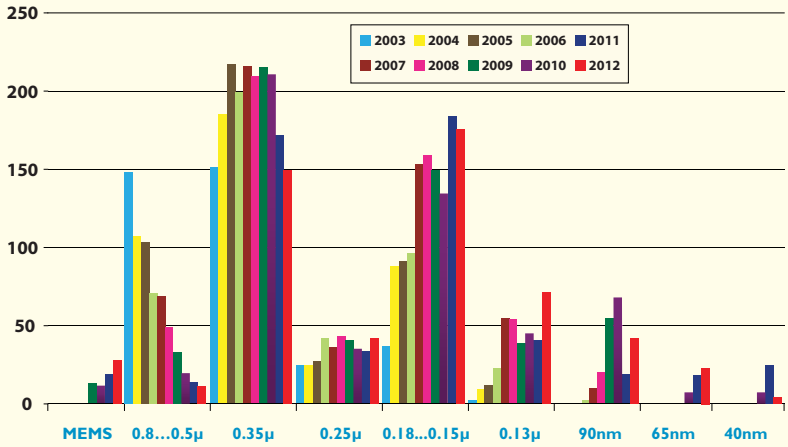
Very encouraging is the fact that the *mini***@sic** concept continues to be accepted very well by the universities in 2012, although the funding by the EC was interrupted for about one year.



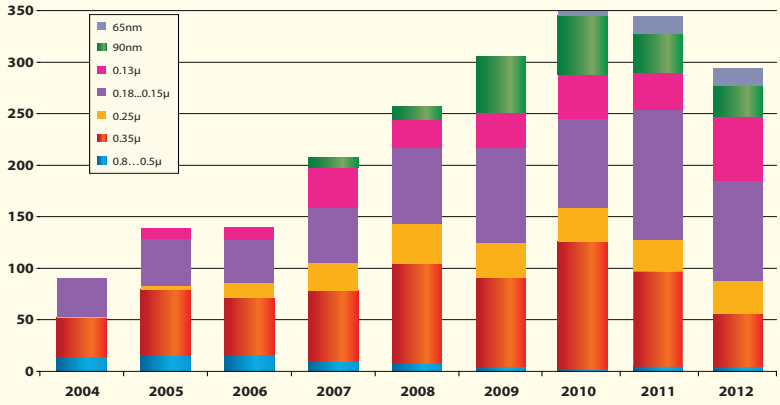
	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
Industry + non-European univ/research	140	159	155	115	128	138	134	154	164	153	113	143	139
Europractice Research	27	46	13	48	52	69	84	87	85	87	83	96	105
Europractice Academic	313	281	237	200	234	243	215	298	285	305	337	321	301



MPW designs in 2012: technology node and number of designs



Geometry mix

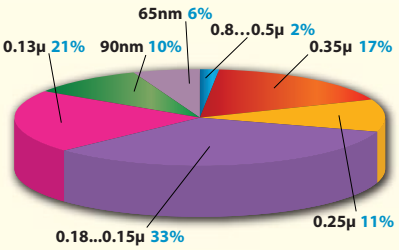


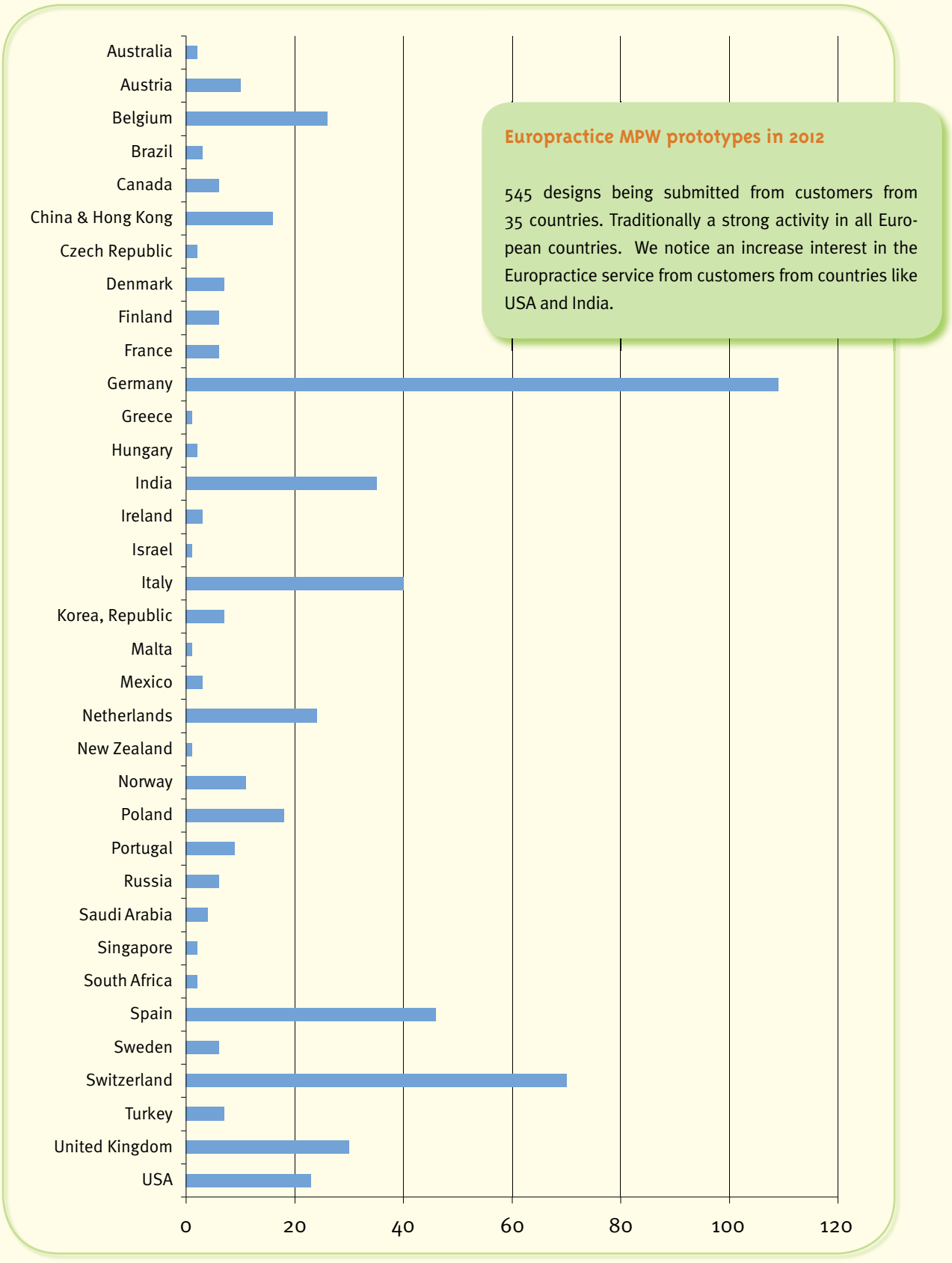
mini@sic designs per gatelength in 2012

Small volume projects

More and more customers are using the COT (Customer Own Tooling) model when they need volume production. Through this COT model they have full control about every aspect of the total design and production flow. Large customers with sufficient ASIC starts and volume production can invest in the COT model as it requires a considerable knowledge and experience about all aspects such as libraries, design kits, transistor models, testing, packaging, yield, etc. For smaller customers the COT model is very attractive but very difficult due to the lack of experience. For those customers EUROPRACTICE offers the solution by guiding the customers through the full production flow applying the COT model. EUROPRACTICE helps you with technical assistance in the selection of the right package, setting up the test solution, yield analysis, qualification, etc.

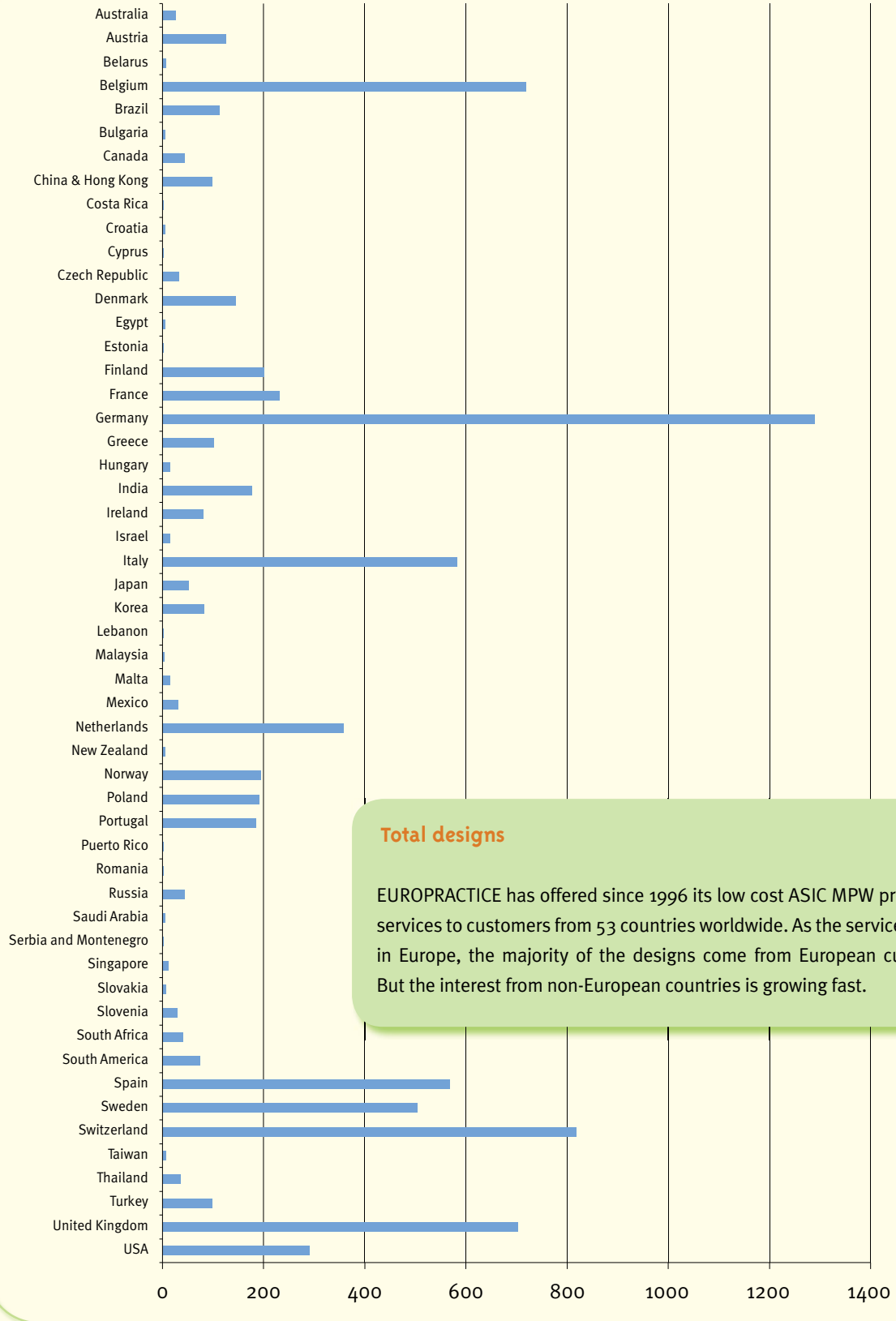
Through EUROPRACTICE you can also experience the benefits of the COT model.





Europractice MPW prototypes in 2012

545 designs being submitted from customers from 35 countries. Traditionally a strong activity in all European countries. We notice an increase interest in the Europractice service from customers from countries like USA and India.



Total designs

EUROPRACTICE has offered since 1996 its low cost ASIC MPW prototyping services to customers from 53 countries worldwide. As the service is based in Europe, the majority of the designs come from European customers. But the interest from non-European countries is growing fast.

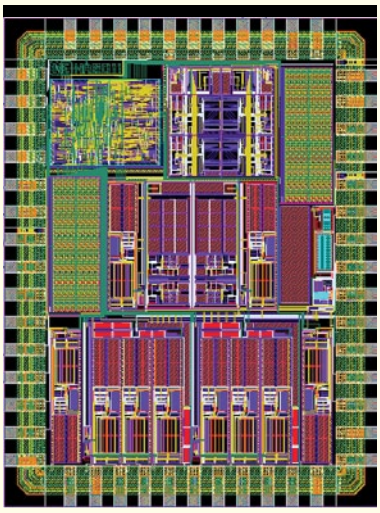
Examples of ASIC projects

ams

Programmable 2-channel ASIC for portable long-term monitoring of biomedical signals

Hamburg University of Technology, Germany
Institute of Nanoelectronics

Contact: Nashwa Abo Elneel, Dietmar Schroeder and Wolfgang Krautschneider
E-mail: nashwa.elsayed@tu-harburg.de
Technology: austriamicrosystems 350nm CMOS C35B4C3
Die size: 3.107 mm x 4.072 mm



Introduction

In recent years, the research and development of CMOS integrated circuits for biomedical signal acquisition systems has increased significantly. This has resulted and will result in novel medical device solutions, as it allows not only a reduction of costs for traditional medical devices, but also facilitates portable long-term applications or implantable solutions.

To cover the wide range of biomedical signals, for e.g. EEG, ECG, EMG and EP, the system should be adaptable to their characteristical features. Hence, providing an optimal setting of the overall system with respect to the signal type and system application achieves the desired system flexibility. In this context, the analog front-end (AFE) is the prime candidate for configurability.

In this regard, the institute of Nanoelectronics at the Hamburg University of Technology, Germany, is developing configurable general purpose ASICs for biomedical signal acquisition, which are able to handle different biomedical signals.

Description - Application

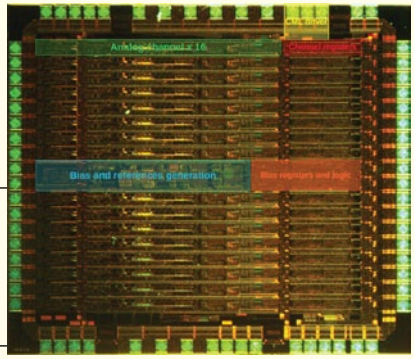
The illustrated layout is for a fabricated 2-channels ASIC. The chip consists of 2 identical channels for the sensitive acquisition of small biomedical voltage signals, where each channel integrates an AFE, a sigma-delta ADC and a DAC. It has the chopper modulation of the input stages for low-noise applications which can be switched on and off. Furthermore, the AFE is programmable as low-power or low-noise by external bias current and can be calibrated in terms of CMRR, gain and bandwidth. The offset compensation is done by a DC-suppression circuit and/or by optional external high pass filter.

The output of the analog to digital converted signals is available via a bidirectional serial interface, which is used for both data reading and chip configuration.

Multi-channel SiPM readout ASIC

Universitat de Barcelona (UB), Institut de Ciencies del Cosmos (ICC-UB), Dept. ECM, Marti Franques 1, 08028 Barcelona, Spain

Contact: Albert Comerma, David Gascón and Lluís Freixas
E-mail: acomerma@ecm.ub.edu
Technology: AMS 0.35 µm SiGe BiCMOS
Die size: 2930x2540 µm2



Application

Silicon Photo-Multipliers (SiPM) are recently developed electronic devices with photon counting capabilities improving current state of the art detectors regarding high voltage requirements, signal gain and magnetic field insensitivity, while keeping at the same time excellent timing characteristics and wide dynamic range. SiPM are semiconductor devices still under development by some manufacturers in order to improve yield, to provide multi-channel architectures and to increase light sensitivity spectrum.
Immunity to magnetic field and compact form factor make SiPM an ideal choice for their usage in particle detectors (specially for calorimeters and Scintillating Fibre Trackers) and also medical applications such as PET (Positron Emission Tomography) scanners when used with an optically coupled scintillating material able to provide the conversion between high energy particles to light pulses.

Description

A mixed mode Front End Readout ASIC for common cathode Silicon Photo-Multipliers is presented with the following features: wide dynamic range, multi-channel (16 channels), low input impedance (around 30 ohms) current preamplifier, low power (6mW per channel), SiPM voltage control and timing, charge and pile-up signal outputs.

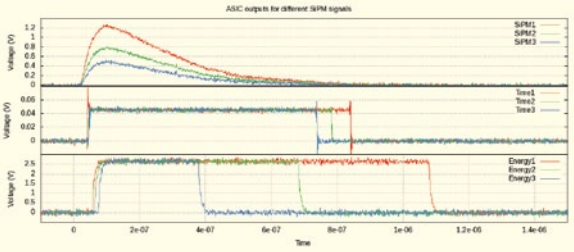


Figure 1. Typical signals

This basic building blocks include: preamplifier with three signal paths (timing and energy)[figure 1], fast current discriminator with digital current mode (CML) output, histeresys comparator for energy measurement and digital slow control. The timing output achieves very small jitter to perform time over threshold measurements (below 40ps jitter measured).
The preamplifier stage includes a novel circuitry with saturation control that permits to be operational on the different signal paths even when the timing output is completely saturated. This circuitry permits the correct operation of the measurement outputs in a wide input dynamic range.

Why Europractice?

For small volume ASIC production EUROPRACTICE offers an excellent solution both in the frequency of MPW runs (*mini***@sic** program) as in price and tools needed for the design. This makes an ideal choice for the submission of prototypes with relevant innovations and test

The main application intended for this ASIC is for the portable long-term monitoring of electrocardiogram (ECG) signals. In such applications, the system's power consumption plays an essential role whereas noise constraints are rather relaxed. Hence, the chip was configured for low-power operation to maximize the battery life-time. Furthermore, the choice of a serial interface rather than a parallel one matches the needs and specifications of a portable monitoring system, which requires a few number of interconnects and a low data rate for communication.

Measurement Results

Tests and measurements of the fabricated ASIC has proven a full functionality in relation to the designed features.

Why Europractice?

Europractice has a variety of fabrication technologies and offers the *mini***@sic** program which allows to fabricate dies having relatively small sizes at affordable prices. In addition, it offers the opportunity for universities to manufacture designs that are based on academic research and not industry related. The Europractice staff, both at the Fraunhofer Institute and IMEC, provide excellent service and supply us with all the necessary information needed to implement such advanced mixed-signal circuits in modern CMOS technologies.

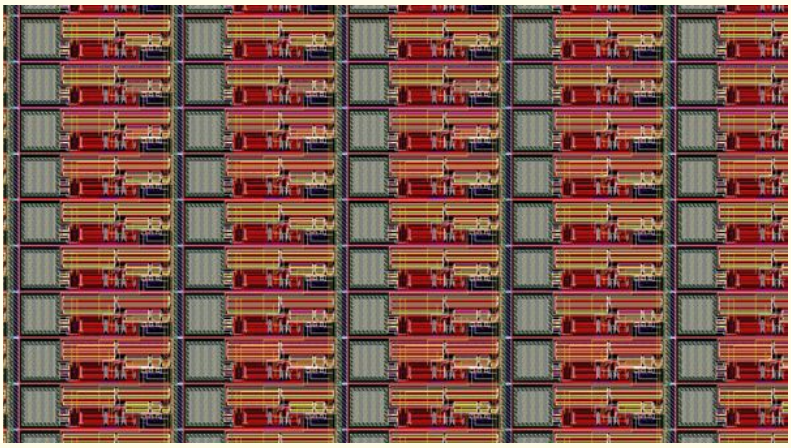


Figure 1: Array of Bio-potential sensors on AMS 0.35µm CMOS

Bio-potential Monitoring and Stimulation Array for Hybrid Organic-Inorganic Machines

Department of Electrical and Electronic Engineering, University of Bristol, UK

Contact: Paul Warr (www.bris.ac.uk/engineering/people/person/paul-a-warr)
Email: paul.a.warr@bristol.ac.uk
Technology: AMS 0.35µm CMOS (C35)
Die size: 7mm²

Description

Direct interaction between the integrated cellular processing domain and the living cellular-neural domain will provide a new platform for computation, communication and control. Potential applications include prosthesis, man-machine interfaces, organic computing, living machines, and targeted drug therapy. However, the first step is a two-way analogue interface between these very different entities and a good first aim is to better understand the operation of a network of living neurons by observation at the neural scale. This work is specifically in-vitro and is at the early stage of proving a technique to observe the bio-potential disturbances generated by an array of brain cortical neurons grown on top of a high-density array of die-top monitoring points. Biochemical techniques for the patterning of brain cortical neuron growth have been developed and the current challenge is the provision of conditions suitable for cellular-level life on an essentially non-bio-compatible IC die.

From the electronics perspective, the living cells have virtually no ability to deliver energy and so the bio-potential disturbances must be observed via a very high input impedance circuit; yet the input FET must be biased correctly. This, coupled with the inherent close proximity of the monitoring points, makes the analogue front end a key element in the design.

There are significant practical problems to overcome. For example, the die must dissipate only small amounts of energy as heat because living cells in an in-vitro environment have no temperature-regulation ability. On-die temperature monitoring can drive integrated heaters (resistors) to bring the die-top temperature up to circa 37 Celsius but cooling the die-top would require extra-die systems of significant bulk. One further practical problem is packaging: an aqueous environment including certain life-supporting chemicals is required on the die-top which,

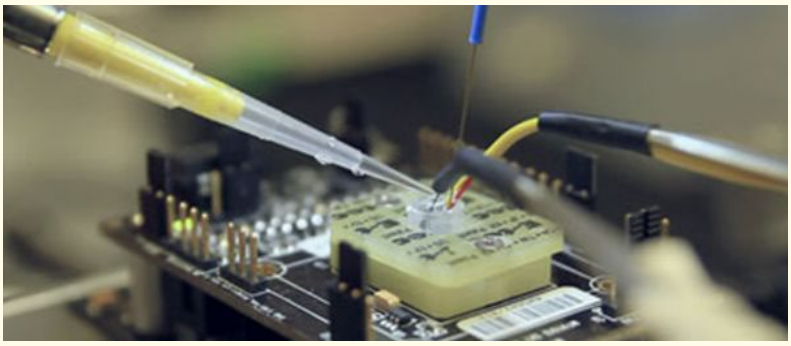


Figure 2: Experimental Set-up for Early Concept-Proving Work.

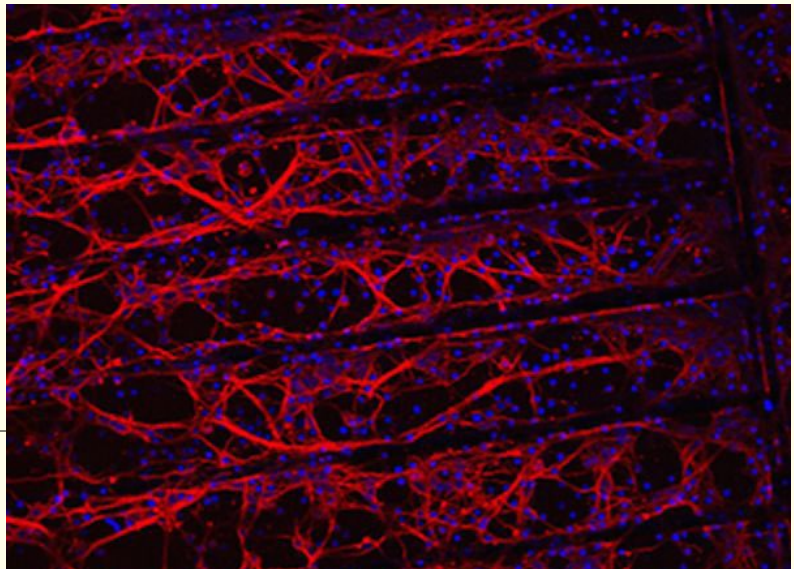


Figure 3: Rat cortical Neurons on Boron-doped Diamond Following Laser Micromachining

consequently, must be exposed. Wire bonds for power and communication must be far from the fluid on a die of area 7mm2. In this early phase of research, a DPMS resin well is formed on the die-top which is extended to encapsulate wire bonds and non-array bond pads around the periphery.

Currently, a sensor-only die is being tested with artificial neural-like inputs via a custom-built wafer probe head and a sensor/stimulator die is being designed with temperature regulation circuits. Two Europractice MPW fabrications are planned for 2013 and no doubt many more engineering challenges will be found and (hopefully) overcome.

Why Europractice?

The University of Bristol uses Europractice-delivered EDA packages in several undergraduate and taught-postgraduate units. This gives our students first-hand experience of industry-standard contemporary tools for analogue and digital design flows. It would not be possible for us to deliver this important learning experience to future IC designers without the support, package-maintenance and cost/subsidy negotiations carried out by the Europractice consortium. Access to MPW runs for the practical validation of research concepts and, in cases such as the bio-chip above, physical experimentation essential to the research methodology is invaluable to us as a research institution active in the area of microelectronics.

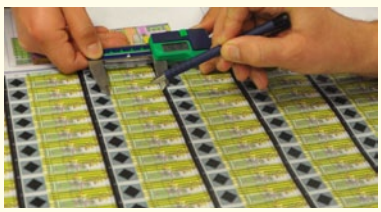


Figure 4: Team Discussion over a Paper Copy of One of the Sensor Arrays

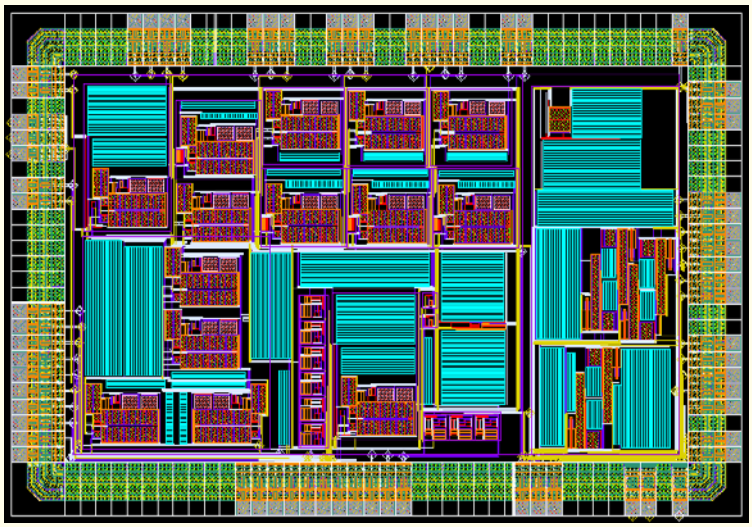


Figure 1: Complete chip layout.

Fully-analog lock-in amplifier with automatic phase and frequency tuning

Dept. Industrial and Information Engineering and Economics, University of L'Aquila, Italy[1]

Dept. Electronic Engineering, University of Roma Tor Vergata, Italy[2]

Contact: Andrea De Marcellis[1] (andrea.demarcellis@univaq.it), Giuseppe Ferri[1], Arnaldo D'Amico[2]

Technology: AustriaMicroSystems 0.35µm CMOS C35B4C3 4M/2P/HR/5V IO
Full-chip die sizes: 4.72mm X 3.26mm (15.39mm2)
Package and PIN: JLCC 68 PIN
Total devices: 228 nMOS; 253 pMOS; 34 capacitors; 62 resistors
Supply voltage: 1.8V (single)
Total current: 1.130mA (max)
Total power consumption: 2.03mW (max)
Operating frequency range: 2.5 ,25Hz (selectable)

Introduction

the accurate measurement of very small signals and noisy signals (i.e., SNR<1), and/or their variations, represents a very important task, especially in sensor applications[1-4]. In this sense, often traditional filtering techniques cannot be adopted, while it results to be very important to perform the optimization/maximization of the measurement system sensitivity and resolution. In particular, the well-known lock-in technique, which is able to extract from noise the amplitude of an AC voltage signal at a known reference frequency, can be taken into account, obtaining a suitable SNR improvement. More in general, both commercial and in the literature lock-in amplifiers, are mainly of digital kind and show high costs and weights, owing to their rather complex architectures (often based on *DSP*). Alternatively, especially in sensor applications, the analog kind of the signal to be revealed suggests the use of analog lock-

in systems. Unfortunately, in order to allow correctly the reading of the output voltage, proportional to noisy input mean value, both analog and digital traditional lock-in amplifiers have the disadvantage of knowing or fixing the operating frequency (reference) and requiring, at power-on and continuously during the system working time, an accurate phase alignment, between input and reference signals, typically achieved by manual operations. Moreover, if an operating frequency variation occurs, the system requires an additional calibration or, in worst cases, the re-design of internal blocks.

Description of the ASIC

We have developed a new fully-analog integrated lock-in amplifier suitable for the accurate measurements of very small and noisy signals[5]. By means of ensured suitable internal feedbacks, the system operates automatically and continuously phase and frequency tunings of input noisy and reference signals, both at power-on and if a variation occurs (of the phase and/or the operating frequency) during the working time, providing constantly correct measurements. This new integrated system, whose layout is reported in Figure 1, has been designed and fabricated in CMOS AMS 0.35µm, as shown in Figure 2, with a single supply voltage (1.8V) and reduced power consumption (2mW). Through some external passive components, it is possible to select the operating frequency range more suitable for the desired application. Preliminary results have demonstrated the capability of this analog lock-in amplifier to measure very small signals, also buried into noise, with improved sensitivity and resolution values which allow to reveal AC voltage signal amplitudes as low as tens of nanovolts.

Why EUROPRACTICE?

The University of L'Aquila is an active academic member of Europractice. The use of Europractice IC services, and in particular of *mini***@sic** programs for our project prototyping, allows us to have access to a comprehensive MPW fabrication service which provides highly competitive pricing to different modern process technologies (e.g., CMOS, BiCMOS, MEMS, etc.). Moreover, we have always achieved excellent support from both the MPW and software services.

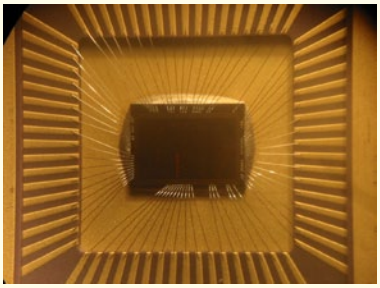
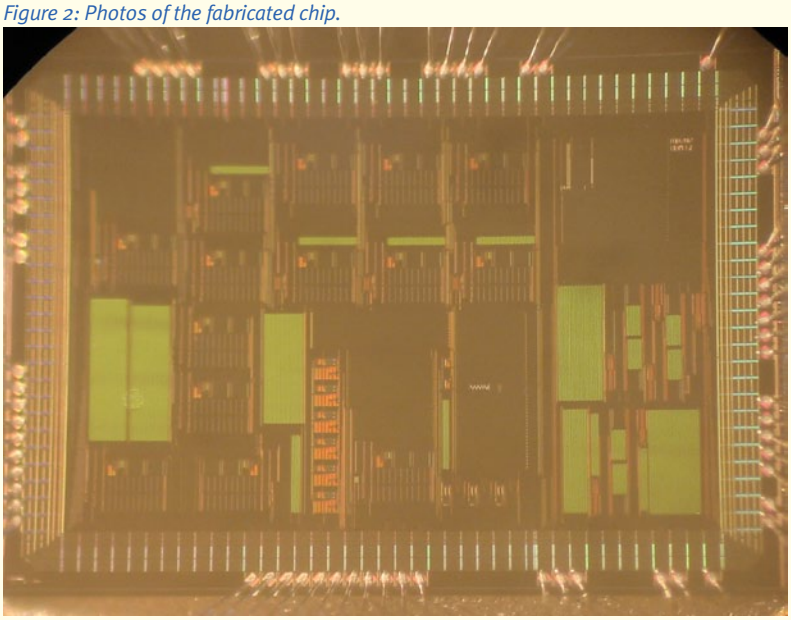


Figure 2: Photos of the fabricated chip.



(courtesy of Nikhef).

Acknowledgements

this work was supported by the Italian Ministry of University (MIUR) under a Program for the Development of a National Interest Research (PRIN Project 2008XZ44B8).

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[3] A. De Marcellis, G. Ferri, C. Di Natale, E. Martinelli, A. D'Amico, "A Fully-Analog Lock-In Amplifier with Automatic Phase Alignment for Accurate Measurements of Very Low Gas Concentrations", IEEE Sensors Journal, 12 (2012), 1377-1383.

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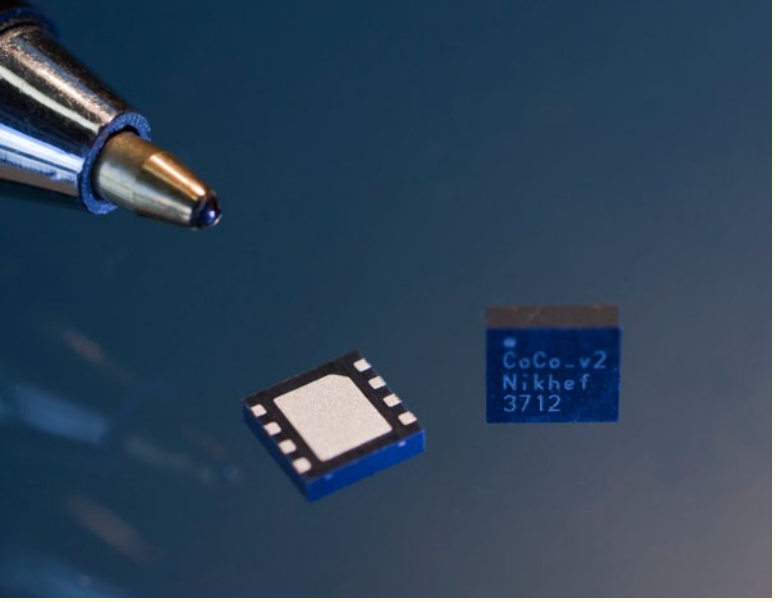
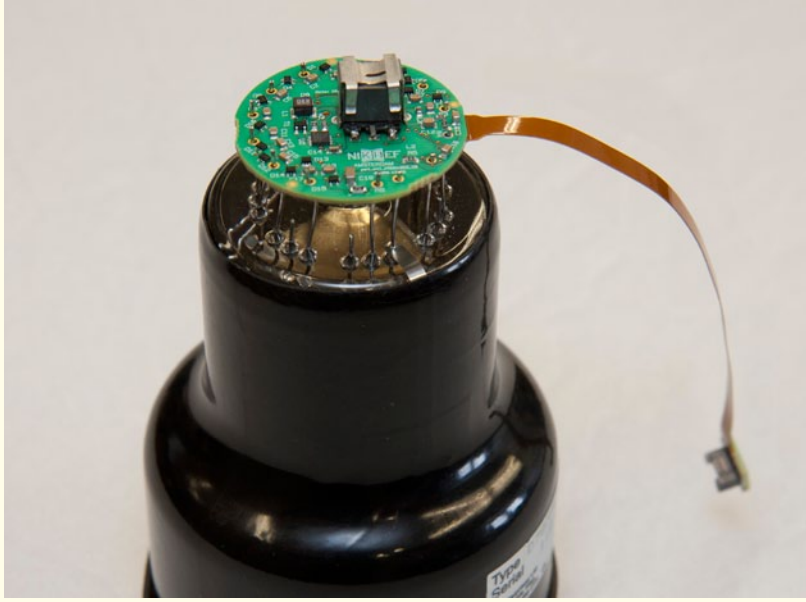




ASIC Designs in the KM3NeT Detector

National Institute for Subatomic Physics - Nikhef, Science Park 105, 1098XG Amsterdam, The Netherlands

Contact: Deepak Gajanana, Vladimir Gromov, Paul Timmer, Ruud Kluit
E-mail: deepakg@nikhef.nl
Technology: ams 0.35µm CMOS C35B3C3
Die size: PROMiS: 2.13 mm²; CoCo: 1.0 mm²

Description

In the KM3NeT project[1,2], Cherenkov light from the muon interactions with transparent matter around the detector, is used to detect neutrinos. Photo multiplier tubes (PMT), used as a photon sensor, are housed in glass spheres (aka Optical Modules) to detect single photons from the Cherenkov light. The PMT needs stable high operational voltage (~1.5 kV) and is generated by a Cockroft-Walton multiplier circuit, using discrete components. A surface mount PCB is designed (38 mm dia) which contains the basic CW multiplier circuit to generate the required voltages to drive the dynodes of the photomultiplier tube. The system draws less than 1.5 mA of supply current (3.3 V) with outputs up to -1500 V DC cathode voltage, a factor 10 less than the commercially available state of the art. The electronics required to collect the signals from the PMTs and to control the CW circuit, is integrated in two ASICs: a) Front-end mixed signal ASIC (PROMiS) for the readout of the PMT and b) Analog ASIC (CoCo) to control the feedback of the high voltage (HV) Cockroft Walton (CW) generator[3,4,5].

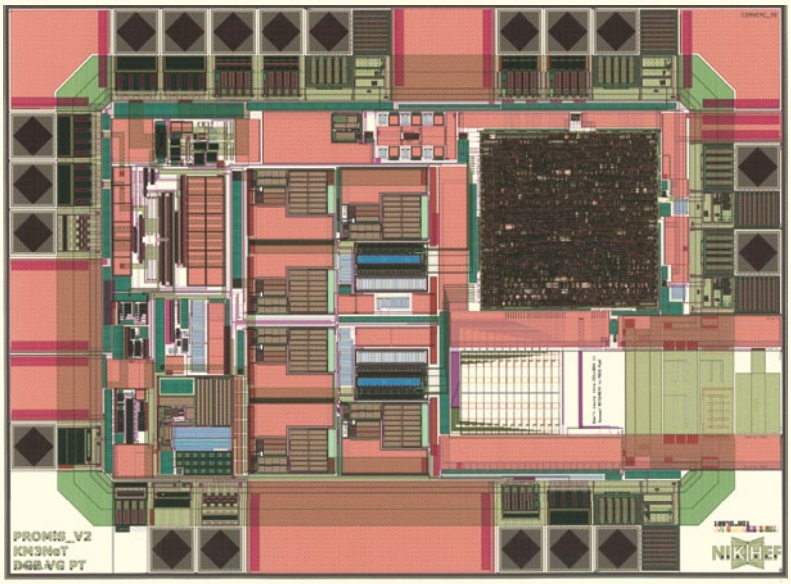
PROMiS IC

The pre- amplifier boosts the input charge from the PMT and a comparator discriminates against an adjustable threshold level. The ToT (Time over Threshold) determines how long the signal is above the threshold value and is transmitted in the form of LVDS signals and is quantified later in the system by TDC (Time to Digital Converter). The functionality of the chip also includes two 8-bit DACs: 1. To control the threshold level of the comparator 2. To control the reference voltage of the High Voltage generation part. An analog output buffer (test purpose only) is added to monitor the pre-amplified signal for qualification of the complete PMT module. An I²C slave configuration is implemented to communicate with the chip. A 24 bit one-time programmable memory is integrated to uniquely identify each chip. The ASIC is designed in 0.35µm ams CMOS technology and consumes <30 mW power and has an area of 1.7mm x 1.25mm in silicon.

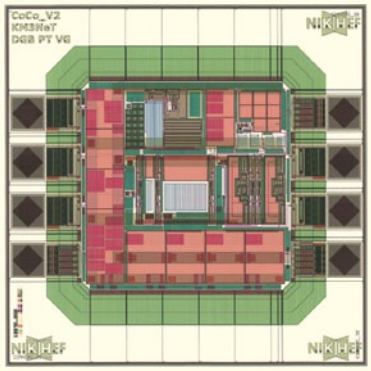
CoCo IC

CoCo is designed to control the feedback of the CW circuit and issue a stable HV supply for the PMT. The CoCo comprises of a current controlled oscillator, a monostable circuit to define the pulse width and over current protection for the transformer. It controls the frequency of the pulses issued to the CW circuit. The feedback voltage from the CW is converted to current and the current is used to charge and discharge a fixed capacitor on board. The change in feedback voltage, means a change in current and hence change in the frequency of the pulses, which results in the smooth operation of the regulator. The ASIC is designed in 0.35µm ams CMOS technology and consumes <2 mW power and has an area of 1mm x 1mm in silicon.
Advantages of the chips are : stable HV, smaller footprint, lesser cost, power and external components on the board.

The RM5-hemisphere from the KM3Net project (Propriety KM3NeT Consortium).



Plot of the PROMiS IC.



Plot of the CoCo IC.

Why Europractice?

The 'General' and '*mini*@sic' MPW runs organized by Europractice makes IC design, prototyping and low volume production affordable for Research Labs like Nikhef and therefore enables physics research to build state of the art experiments.

Acknowledgments

This work is part of the research program of the "Stichting voor Fundamenteel Onderzoek der Materie (FOM)", which is financially supported by the "Nederlandse organisatie voor Wetenschappelijke Onderzoek (NWO)", The Netherlands.

References :

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[2] http://www.km3net.org/CDR/CDR-KM3NeT.pdf

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[4] D.Gajanana et. al. "A Front end ASIC for the readout of the PMT in the KM3NeT Detector" , TWEPP 2010

[5] D.Gajanana et. al. "ASIC Design in the KM3NeT Detector" , TWEPP 2012.

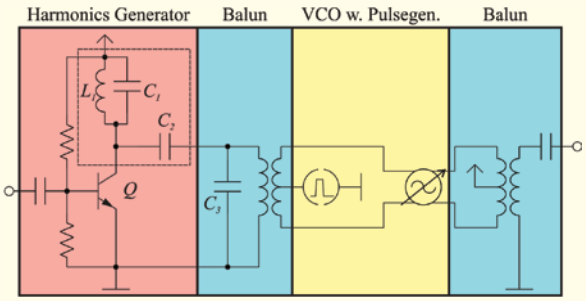
SILO IC Design in IHP SG13S

Lehrstuhl für Technische Elektronik, Universität Erlangen-Nürnberg, Cauerstr. 9, 91058 Erlangen, Germany

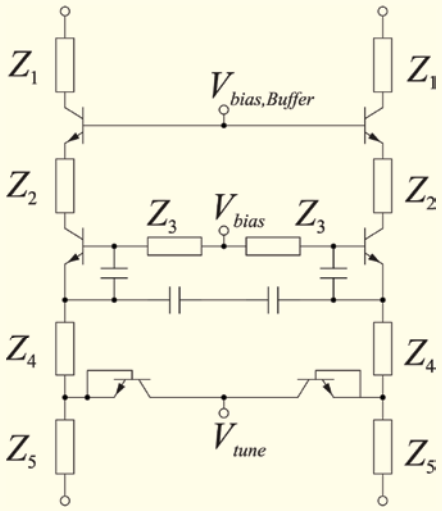
Contact: Alexander Eßwein
E-mail: esswein@lte.eei.uni-erlangen.de
Technology: IHP SG13S
Die size: 1,01 mm²

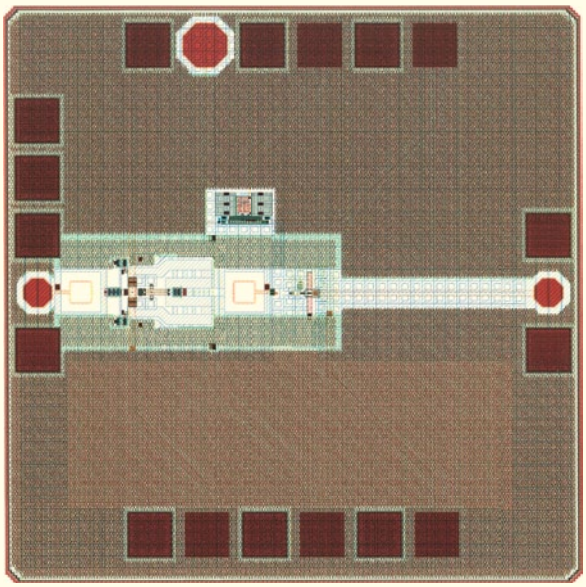
Description

The system is developed for pulsed angle modulated signal generation at mm-wave frequency. It is based on the switched injection-locked oscillator (SILO) approach[1]. The input signal of 5.8 GHz is coupled into the harmonics generator, which consists of a bipolar transistor with a resonant load. The load consisting of a transmission line of inductance L1 and capacitors C1 and C2 is designed to couple the wanted 11th harmonic into the transformer.



For an input power > -3 dBm, the 11th harmonic is the strongest. The now differential signal is used to lock the VCO shown here:





The signal is coupled to the collector load transmission lines of the Colpitts oscillator using a transformer with a center tap. The center tap is connected to the pulsed current source of the oscillator.

The input for the pulse control is a simple sinusoidal signal with a period that coincides with the wanted pulse repetition rate. This signal is is converted to a square wave by a Schmitt-Trigger and then applied to two delay lines. One line is a simple chain of inverters. The other line consists of current starved inverter cells. The signal of both lines is then applied to a simple 2-input AND. Manual control of the second line's delay enables control of the peak duration that is applied to the oscillator's current source.

The SILO approach has already shown promising performance in a 7 GHz system. Our goal for the circuit was testing the on-chip harmonics generation as well as finding the optimal point to couple the injection-locking signal into the tank of the oscillator.

Why Europractice?

The '*mini*@sic' MPW runs organized by Europractice allow prototyping for research in this advanced technology to be affordable for small but important designs.

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URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6185196&isnumber=6185137

MEMSCAP

Co-existence of MEMS antennas and MEMS sensors on a single substrate

Institute of Telecommunications (ITC), Vienna University of Technology

Contact: Dipl. – Ing. Philipp Gentner
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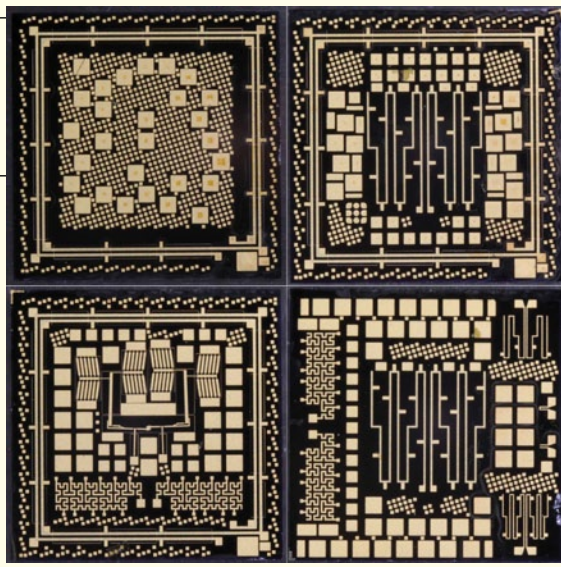
Technology: MetalMUMPS
Die size: 10 x 10 mm²



Introduction

Miniaturized antennas and miniaturized sensors are in the scope of our research for the application of RFID tags. Passive sensor tags can be used for tracking specific physical parameters of goods, for example in the food or medical supply chain.

Using a hybrid communication scheme by simultaneously occupying UHF and UWB frequency bands[1], our system on chip has been designed and manufactured with an overall size of 3mm² [2]. Since the conductivity of the silicon in the CMOS process used for this device is large and the available area for an antenna is very small, antennas manufactured with the MetalMUMPS technology offer several advantages. In particular, reduced conductivity of the substrate, increased area, gold cladded nickel, and the possibility to raise the radiating structures above the substrate help to improve the performance. To be able to make comparisons with our available CMOS devices, the antennas have been scaled to fit into an area of 25mm². In three of the four regions of the die, a UHF loop antenna, a loop with a dipole structure, a loop with a temperature sensor (MEMS version of [3]) together with a fractal dipole have been placed. On the fourth region test structures for on-wafer probing were foreseen (see Fig.1).

Description

As a basis for all designs the loop antenna is placed on the circumference of the respective regions. To fulfill the metal density rules, the center of the loop is filled randomly with metal patches. The loop is formed out of two gold cladded turns of nickel. Conductor width is 46µm, and the spacing was chosen as 54µm. To increase the Q-factor of the inductor, four 25µm deep trenches are used underneath the conductors. Anchors are needed to fix the structure. Simulations of the structure yield an inductance of 65nH at 850MHz with a Q-factor of 12.

The width of the conductor for the dipol used for wideband transmission is 30µm. The meandered dipole is placed inside the loop antenna, with the rest of the die filled with metal patches, according to the metal density rule. For the dipole no trenches are used, because bandwidth is inversely proportional to the Q-factor. A combination of two antennas and one temperature

sensor is placed onto the third region. Instead of the original meandered dipole, a fractal shaped dipole is layouted to decrease the necessary area. The passive MEMS structures were connected to the CMOS devices, and are by now available at the institute. Their functionality has been demonstrated, with the details of the performance being still under investigation. The power transfer between a commercially available 866MHz RFID reader could be increased with the MEMS loop as compared to the CMOS loops. This improvement yields a significantly increased reading range.

Fig.1: Fabricated MEMS antennas and sensors.

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[3] Steiner, H., Keplinger, F., Hortschitz, W. and Stifter, M.: "The Non-linear Thermal Behavior of SU–8" in 35th Int. Spring Seminar on Electronics Technology, 2012.

Acknowledgements

This project was supported by the Austrian research promotion agency (Contactless (RFID) Sensing Project, Project Nr. 830604).

Why Europractice?

The MEMS technology provided by Europractice is a highly appreciated design platform, because it gives insight into state of the art in MEMS design. It lets us significantly improve antennas, which up to now have been produced monolithically in CMOS. The gain in performance has been verified by careful laboratory evaluation.

Thermal actuator for temperature sensing

Institute for Sensor and Actuator Systems (ISAS), Vienna University of Technology

Contact: DI Harald Steiner
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Technology: MetalMUMPS
Die size: 10x10mm²

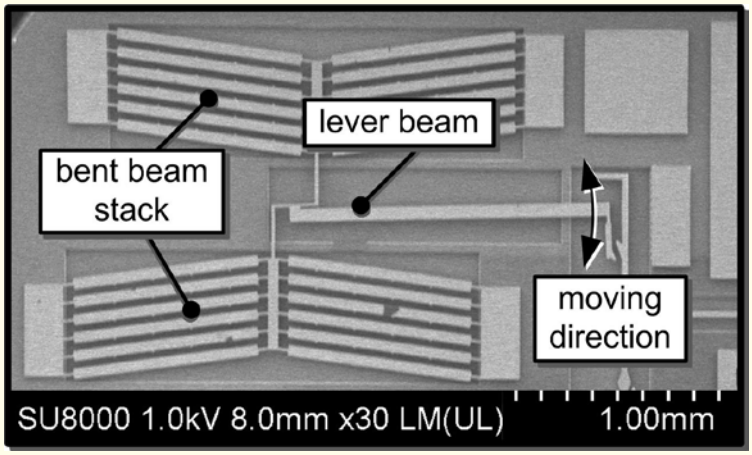


Fig.1: SEM image of the fabricated Actuator.

Introduction

Thermal actuators are broadly used, e.g. as microgrippers. Many of them rely on resistive heating elements and are locally heated up to several hundred degrees Celsius[1], with power requirements in the range of mW.

A completely passive thermal actuator was designed, to reduce this energy consumption. Only the temperature of the surrounding environment is used to deflect the tip of the actuator. State-of-the-art actuators show sensitivities in the range of 0.01µm/°C up to 0.17µm/°C [1][3]. Our goal was to increase these sensitivities, and get reasonable deflections already in the temperature range of several ten degrees, in order to enable its use as a temperature indicator. Common polymers used in the MEMS fabrication (such as SU-8) exhibit large thermal expansion coefficients but also show instabilities in the needed temperature range of the sensor[4]. Therefore, Ni was chosen as base material for the actuator.

Description

The actuator consists of two symmetrical bent beam stacks. Each stack consists of 6 beams in parallel. The stacks are coupled facing each other and only slightly shifted along the mirror axis. Both stacks are connected to a lever beam. Due to the thermal expansion of the material, the tip of the lever moves up- and downwards perpendicular to the mirror axis. The device is built up of galvanic deposited Nickel with a height of 20µm. To avoid the so called stiction phenomenon, the silicon substrate beneath the movable parts of the structure is etched away with in a KOH-solution, generating 25µm

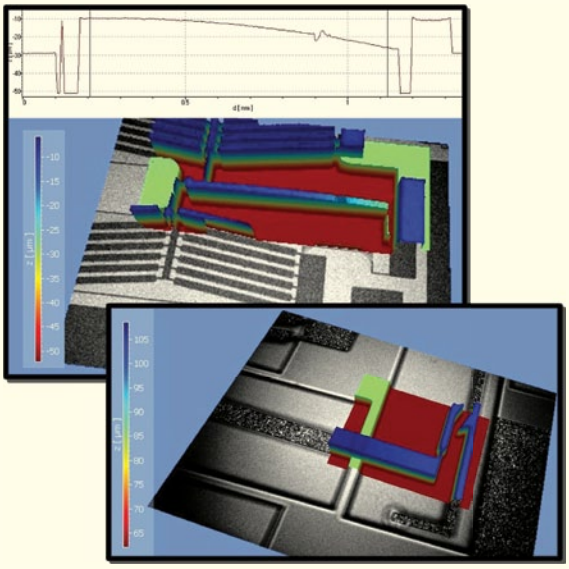
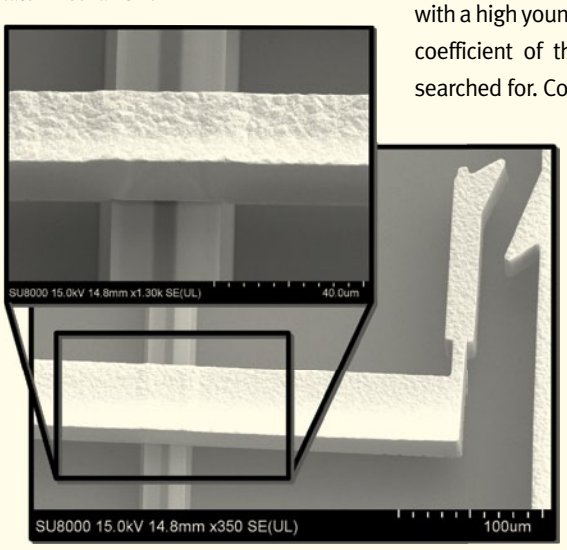


Fig.2: Topographic measurements with and without supporting bridge. The supporting bridge levers the structure in-plane.

depth cavities. Due to stress gradients within the height of the material, the freestanding structure bends towards the substrate[5]. Therefore, supporting bridges were designed to lever the structure and to keep it in-plane. It has been shown that the structure can slide easily on these bridges, and they do not disturb the functionality of the device. A basic functionality check was implemented in form of a simple latching mechanism.

Fig.3: SEM image and detail view of the supporting bridge and the rudimentary latch mechanism.



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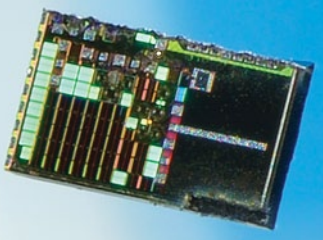
Acknowledgements

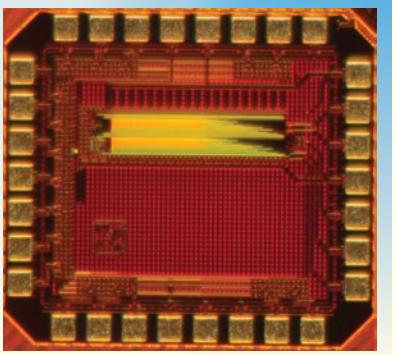
This project was supported by the Austrian research promotion agency (Contactless (RFID) Sensing Project, Project Nr. 830604).

Why Europractice?

For the temperature sensor a material with a high young's modulus and a high coefficient of thermal expansion was searched for. Compared to other materials, Nickel has been proofed as excellent material of choice. Galvanic processes are tricky to handle and Europractice offers with the Metal-MUMPS process a cost efficient way to manufacture such Ni based MEMS devices.

TSMC





A Battery-Less Wireless Temperature Sensor and a 12bit SAR ADC with Data-Driven Noise-Reduction

Eindhoven University of Technology, Centre for Wireless Technology Eindhoven, Mixed-signal Microelectronics Group, The Netherlands

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Technology: TSMC 65nm LP MS/RF CMOS
Die size: 1920 x 1920 um

A Battery-Less Wireless Temperature Sensor

It is expected that the number of wireless sensors in future buildings will increase from a few smoke detectors to hundreds of detectors for e.g. burglary, fire, smoke, gas, temperature, light and motion. The regular replacement of batteries becomes a serious problem for the maintenance and reliability of the building as well as the green environment.

Inspired by this problem, the Centre for Wireless Technology Eindhoven (CWTe) at the TU/e developed a research roadmap for the development of technologies for battery-less wireless sensors. Apart from previously mentioned advantages, this also enables extremely small-size and cheap solutions as all components can be integrated in silicon.

Within the STW project PREMISS, supported by Philips and imec-NL, a battery-less wireless temperature sensor node was developed on a single piece of silicon. It receives energy wirelessly from a central access point using mm-wave frequencies. As the amount of energy that can be transferred and stored was limited to about 1nJ, the sensor and radio are strongly simplified to create an efficient low-power solution. The realized sensor has a volume of only 0.4mm^3 and a weight of 1.6mg and can measure temperature wirelessly without any battery.

A SAR ADC with Data-Driven Noise-Reduction

In more advanced wireless sensor applications (for a.o. environmental and health monitoring), ADCs are required to digitize the sensor information. To maximize the life-time of these portable systems, extremely low power consumption is mandatory. Supported by the CATRENE project Pasteur, a SAR ADC was developed that contains a special Data-Driven Noise-Reduction algorithm. This algorithm can selectively enhance the performance of the comparator, the most power-critical block in the ADC. Only if needed, the performance is boosted while it is set to a very low-power mode in other situations. The 12bit ADC consumes only 97nW from a 0.6V supply when operating at 40kS/s. A world-record power-efficiency of 2.2fJ/conversion-step was achieved, and the chip was recently published at ISSCC 2013.

Why Europractice?

Europractice offers a wide range of design tools that are used throughout TU/e. The *mini***@sic** program brings the possibility to implement small-scale designs in modern CMOS at an affordable price. The complete Europractice team is always extremely helpful and supportive. This is greatly appreciated, especially in the last days before tape-out.

Fully integrated and self-powered interface electronic circuit for vibration based electromagnetic energy harvester

METU-MEMS Center and REDAR Group, Middle East Technical University, Turkey

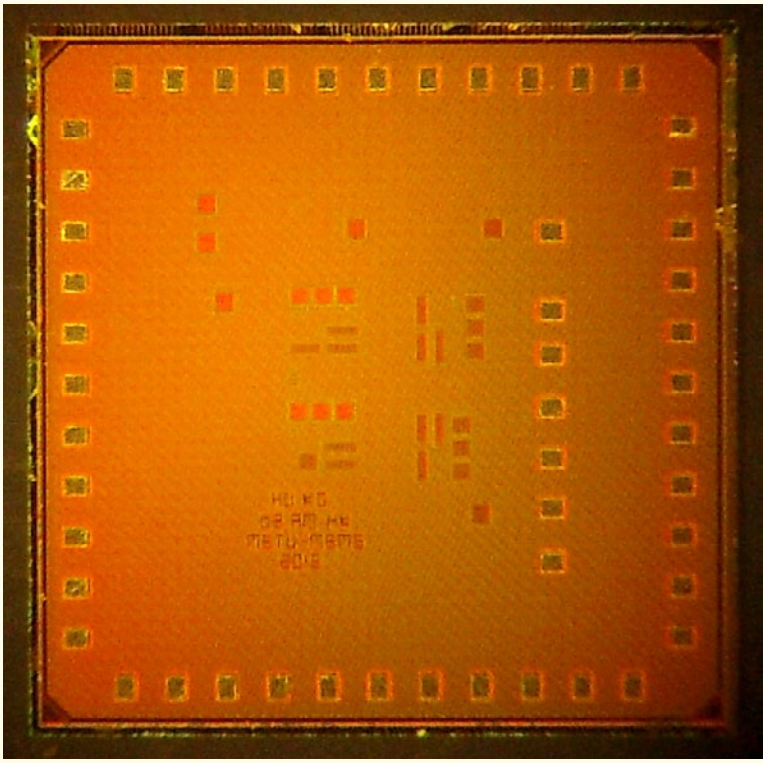
Contact: Hasan Ulusan, Kaveh Gharehbaghi, Ozge Zorlu, Haluk Kulah, Ali Muhtaroglu
E-mail: hulusan@metu.edu.tr
Technology: TSMC 90nm CMOS technology
Die size: 1960x1960 µm²

Description

As technology evolves, demand on wireless and portable systems is increasing. For many years power requirement of these systems are supplied with batteries, however batteries are temporary storage devices with a limited lifetime. Therefore, researches on small sized and continuously charging energy supply elements which are named as energy harvesters have become popular recently. These harvesters use several ambient energy sources such as light, heat, and vibration for generating electrical power. Vibration is especially attractive among these sources due to its abundance in daily life. The power generated by the vibration based energy harvesters is highly dependent on vibration acceleration and frequency. Unfortunately, daily life vibrations are usually at low levels, limiting the generated voltage and power values. Therefore, a highly efficient interface electronic circuit must be designed for such systems to convert the generated power into a usable form.

The fully integrated and self-powered interface electronic circuit is designed for vibration based electromagnetic energy harvester systems. The first block of the circuit is an AC/DC converter, rectifying the generated AC harvester output. Since the generated AC voltage is at low levels, the voltage drop at the AC to DC converter stage is significant. Thus a high-efficiency active rectifier block with considerably low drop-out voltage is used and this block is supplied by another passive rectifier. The second block of the circuit is a DC to DC converter, which steps-up the rectified voltage to a desired value. The DC to DC converter block uses a charge pump and an oscillator circuit. Finally, a regulator circuit block, sensing the output voltage and giving feedback to the DC to DC converter, is utilized.

The proposed system is specifically designed for conditioning low voltage and low power signals in energy harvesting applications, and the first tests of the fabricated chip gives promising results.



Why Europractice?

The frequent CMOS *mini***@sic** fabrication runs that are organized by Europractice are advantageous for academic members of Europractice. Since Middle East Technical University is one of these members, accessing required design kit tools is very comfortable. Furthermore, the technical support given by the Europractice is considerably helpful for researchers in such institutions.

Acknowledgment

This work is in part supported by Intel under Middle East Energy Efficiency Research Program (MER), to conduct and promote research in the Middle East. This work is in part supported by TUBITAK, Turkey under project number 109E220.

ASIC solution for piece-wise-affine forms

Microelectronics Institute of Seville (IMSE-CNM, CSIC), University of Seville

Contact: Dr. Piedad Brox, J. Castro, M. C. Martínez-Rodríguez, E. Tena, C. J. Jiménez, I. Baturone, A. J. Acosta
E-mail: brox@imse-cnm.csic.es
Technology: TSMC Nine-Layer Metal 90 nm CMOS Low Power
Die size: 1860mm x 1860mm

Description-Results

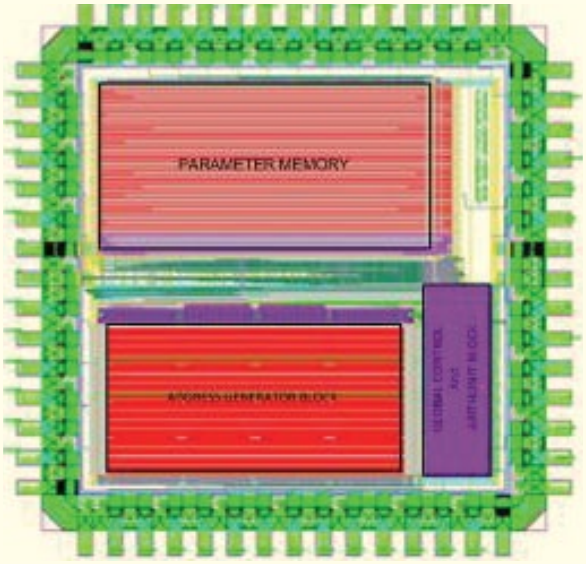
Piece-Wise Affine (PWA) functions are universal approximating functions that can be used to represent control laws and/or estimation laws, such as those used in "virtual sensors" to replace expensive physical sensors with estimates measurements inferred from other related measurements. Canonical forms describe multi-variate PWA functions with the minimum possible parameters. The choice of a specific canonical form is of immediate concern in applications where functions are defined on a multiple dimension input domain, or with many partitioned domains.

This research team developed a VLSI solution to generate PWA functions using the Generic PWA canonical form in[1]. This new circuit implements the Simplicial Piece-Wise Affine (PWAS)[2], the hyper-rectangular Piece-Wise Affine (PWAR)[3], and the Lattice Piece-Wise Affine (PWAL) canonical forms[4]. The implemented architecture provides the three canonical forms, sharing the blocks that have similar functionalities in the three forms, reaching a high level of reusability and optimizing hardware resources. In this way, the architecture disables those blocks that are not used when a specific PWA form has been selected, saving power consumption. The architecture allows configurability and programmability in the operation for the three PWA forms. The ASIC works with a maximum number of dimensions equal to four, being also able to implement PWA functions with one, two and three input dimensions. The possibility of selecting one or two outputs is also covered.

The implemented architecture is composed of four functional blocks:

- PARAMETER MEMORY stores the parameters needed to compute the output of the PWA function. This memory is an IP block provided via Europractice.
- ARITHUNIT, this block provides the output of the PWA function.
- ADDRESS GENERATOR BLOCK generates the address of the Parameter Memory. This block contains three different modules that tackle the address generation of each canonical form. One of these modules is a memory that corresponds to an IP block provided via Europractice.
- GLOBAL CONTROL, a finite state machine that configures the Address Generator Block, the Parameter Memory and the ArithUnit.

Layout and structure of the prototyped chip are shown here:



The ASIC can implement any PWA function with a maximum number of inputs equal to four and one or two outputs. This list enumerates the main specifications fixed for the VLSI circuit:

- Canonical form to be implemented: PWAL, PWAR, PWAS.
- Number of inputs: configurable from 1 to 4.
- Number of outputs: configurable from 1 to 2.
- Input resolution: 12 bits.
- Output resolution: 26 bits.
- Parameters resolution: 12 bits.

Fig. 2: Photograph of the test PCB with the packaged ASIC

Chips have been packaged and a corresponding test board has been designed to be used as interface with the instrumentation equipment and to include the resources needed for characterization measurements (see Fig. 2). The samples have been tested for different PWA forms, and considering different operation conditions. The correct operation for several case studies has been confirmed.

Why Europractice?

Europractice's *mini***@sic** program allows academic institutions to do affordable prototyping in state-of-the-art nanoscale CMOS technologies. The straightforward access to design tools, IP modules, support team and frequent MPW runs makes Europractice program very attractive.

Acknowledgements

This work was partially supported by MOBY-DIC project FP7-INFSO-ICT-248858 (www.mobydic-project.eu) from European Community, TEC2011-24319 project from the Spanish Government, and P08-TIC-03674 project from the Andalusian Regional Government (with support from the PO FEDER). P. Brox is supported under the post-doctoral program called `Juan de la Cierva' from the Spanish Ministry of Science and Innovation.

References

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An Inverter-based readout system for implantable continuous glucose sensor *and* An Inductorless 3–5 GHz Band-Pass Filter with Tunable Center Frequency for IR-UWB Applications

University of Oslo, Departement of Informatics, Nanoelectronics

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Technology: TSMC 90nm CMOS Low Power MS/RF
Die size: 1920µm x 1920 µm

The chip consists of two projects, first:

A complete transponder IC for continuous monitoring glucose sensor has been implemented in 90nm TSMCrf technology.

The power and data link is transferred wirelessly through a couple of inductor coils with a 13.56MHz RF signal. The on-chip power management part will rectify a RF input signal and generate a clean and stable supply voltage for the circuitry inside the chip. This IC features a novel inverter based readout circuitry which both amplifies the small input voltage signal from the sensor and converts it into a digital output code. The power consumption of the transponder has been reduced by using a single sensor branch which interchanges the polarities of the supply voltage for the sensor. In this way, the net input voltage swing is equal to that in the differential sensor topology. In addition, a sub-threshold inverter has been utilized for both low power and high gain. The digital output code is sent out wirelessly by load modulation scheme (LSK).

Results

The inverter-based readout circuit achieves 8.7 ENOB. The power-on time for the system is 100µs with an average power of 80µW. The energy consumption is 7.7 nJ per sample including data transmission circuitry and input clock buffer. Assuming a single sample every 5 minutes and a complete cut off of the power in between, the system will actually run on 25 pW.

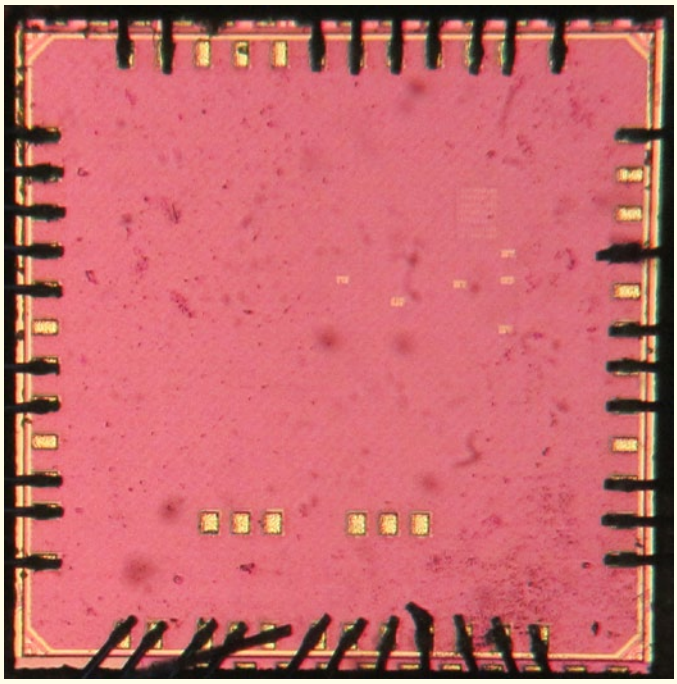
The second project on the chip:

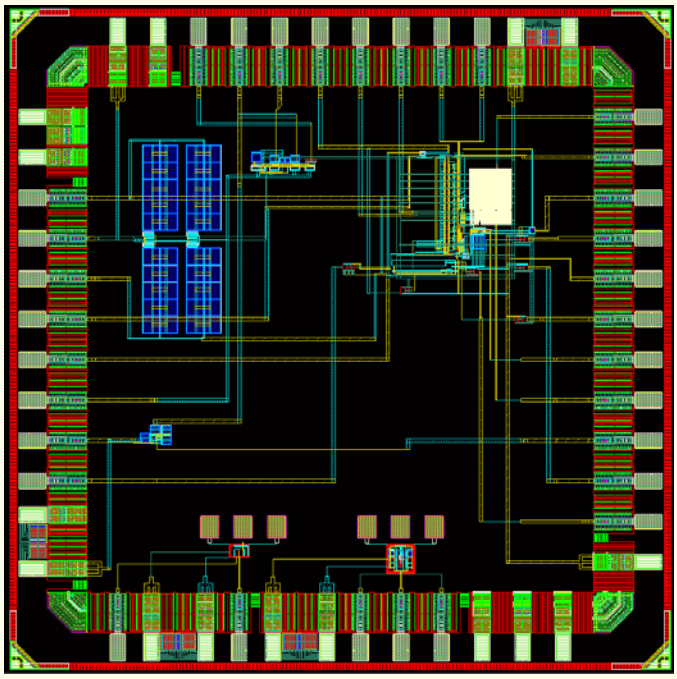
An Inductorless 3–5 GHz Band-Pass Filter with Tunable Center Frequency for IR-UWB Applications

Typically, off-chip passive filters like surface acoustic wave (SAW) filters are used as preselect filters in receiver front-ends. However, the demand for fully integrated systems is favoring solutions with no external components. There are various filter types that are appropriate for the implementation of RF on-chip BPFs include bulk acoustic wave (BAW) filters, active-RC filters, LC filters, often with Q-enhancement techniques, gm-C filters and N-path filters. Each topology has distinct advantages and limitations. The N-path filter is chosen in this design since it can realize a band-pass filter whose center frequency can be tunable by a simple tuning scheme. In addition, it can be implemented in an inductorless configuration for saving chip area that is suitable for low-cost applications. An inductorless switched-capacitor filter based on N-path periodically time-variant networks has been demonstrated in standard 90 nm CMOS technology. The filter basically transfers the low-pass characteristic of a network to a band-pass one by means of frequency mixer. As a part of the filter, a multiphase clock generator is proposed suitable for RF frequencies. The multi-phase clock generator is built with digital logic gates, thus, can be easily scaled to finer pitch technology. The filter is compact, suitable for standard digital technology, and can be fully integrated without any external clock reference. It is competitive to other state-of-the-art tunable band-pass filters, and could substitute passive SAW filters for broadband wireless radio-communication.

Results

The filter occupies a chip area of 0.004 mm^2, and consumes a power of 1.1 mW from 1.2 V supply voltage. It achieves a -3 dB bandwidth of 2 GHz with center frequency tuning range between 4 GHz and 4.4 GHz. NF is approximately 14 dB over 3–5 GHz bandwidth with minimal dispersion.





Why Europractice?

The department of Informatics and the department of Physics at the University of Oslo has been members of EUROPRACTICE for a long time. Europractice gives our departments access to state of the art software and CMOS fabrication at affordable rates and excellent support for these tools and processes. Thanks to Europractice, the University of Oslo can provided tools and IC design facilities in modern CMOS technologies for students and researchers.

UMC

A Multiview Rendering Core in 65nm CMOS

ETH Zurich, Integrated Systems Laboratory (IIS), Switzerland

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Description

A drawback of current three dimensional video systems is that viewers must wear glasses in order to experience the depth effect. Cues, such as motion parallax that would provide an enhanced perception of the depth, cannot be provided using this technology either. Next generation 3D therefore relies on autostereoscopic displays, i.e. displays that provide stereoscopic 3D (S3D) effects without cumbersome glasses or the like[1]. Simple autostereoscopic displays force the user to a very specific position in front of the display. To overcome this problem of strong spatial confinement and to allow several persons to simultaneously use the same display, modern displays – so called multiview autostereoscopic displays (MADs) – use multiple views of the same scene. However, larger numbers of views (currently 8-9) render content creation an increasingly difficult process. Large camera rigs are required for direct capture of multiview video, and the transmission and storage requirements are multitudes of S3D content with its two views. Moreover, the number of views and the post processing for MADs are highly display-type dependent. Therefore, so called Multiview Synthesis techniques have gained increased interest over the last years.

The idea is to generate the large number of views from a small subset, e.g. from ordinary S3D footage.

The main multiview synthesis technology today is Depth Image Based Rendering (DIBR) which uses a dense depth estimation of the footage in order to reproject it to the new views. Despite the physical correctness of this approach, an accurate depth estimation and a subsequent hole filling mechanism are required. The approach we considered in this project follows a diverse concept based on Image Domain Warping (IDW).

Sparse image features and saliency information are extracted in order to calculate nonlinear, two-dimensional image transformations for the generation of the multiple views [2]. Although this is not physically correct it leads to visually pleasing results and circumvents the need for accurate depth maps and in-painting.

The ASIC shown in Fig. 1 was developed during a Masters thesis in collaboration with Disney Research Zurich. It implements an IDW rendering stage compliant with the framework proposed in[2]. The chip receives two 1080p images plus warp information, generates the required views and interleaves them appropriately into one 1080p output image which can directly be displayed on a MAD (Fig. 2 shows such an interleaved im-

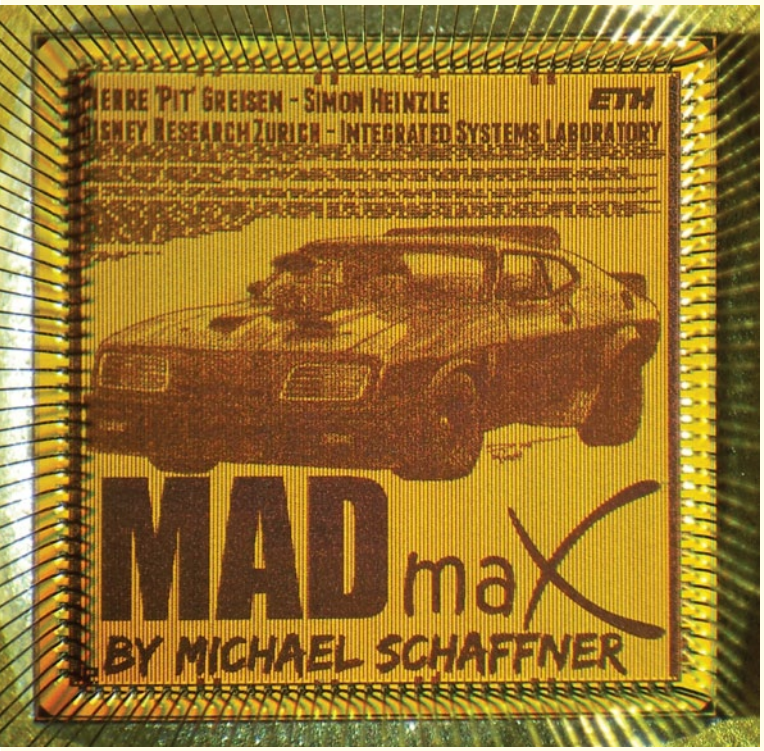


Fig.1. Photo of the fabricated chip. The top metal layer (ME8) was devoted to the power distribution grid (i.e. no signals where routed on this layer). After the chip was finished, the empty space between the power grid stripes was utilized to interleave a large logo. The chip shares its name with the movie Mad Max by George Miller from 1979. The artwork is the Interceptor used in the movie and was drawn by Dan Poll (used with his permission).

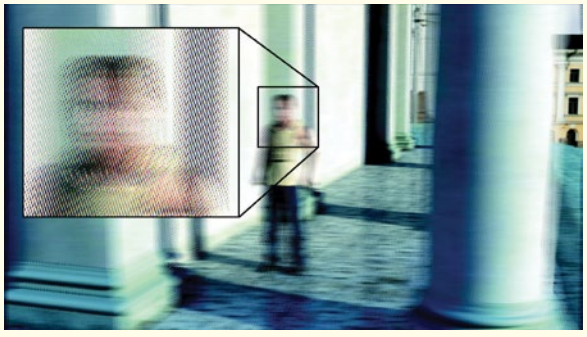


Fig.2. Example of rendered image with 8 interleaved views (test image from [3]).

age). It supports a maximum number of 9 views and has a throughput of 44.2 interleaved frames per second with 8 enabled views.The design has two different clock domains: the rendering core operates with a 400 MHz clock. The in- and outputs run at 100 MHz, which allows for relaxed timing constraints at the interfaces. Parameters, such as the view positions, the display interleaving pattern and the view-to- display-subpixel allocation, are fully programmable.

Realistic assumptions on the vertical displacement of image pixels allowed to design a hardware architecture that does not require an off- chip memory. Our design exhibits 5.046 MBit on-chip SRAM and supports a maximum vertical displacement of 11 pixels. The gate count of the chip is 2289.15 kGE (excluding memory) and its simulated power consumption is around 1.5 W. Fig. 3 shows the FPGA board developed in order to functionally verify the ASIC and to embed it into the whole multiview synthesis system.

Why Europractice?

From our experience, we at ETH Zurich firmly believe that completing a full design and test cycle is the best, if not the only, way to prepare for an engineering career in the electronics and microelectronics industry. Education and research confounded and across all ETH labs and semiconductor technologies, more than 600 persons have actively participated in VLSI design projects and more than 375 chips have been fabricated since 1986. Roughly half of these circuits have been manufactured via various MPW services made available by Europractice IC Manufacturing Services over the years. What's more, the vast majority of circuits have been synthesized, simulated, placed, routed and verified using EDA tools licensed to ETH through Europractice Software Services.

References

[1] J. Konrad and M. Halle, "3-D displays and signal processing,"Signal Processing Magazine, IEEE, vol. 24, no. 6, pp. 97 –111, 2007.

[2] M. Farre, O. Wang, M. Lang, N. Stefanoski, A. Hornung, and A.Smolic, "Automatic content creation for multiview autostereoscopic displays using image domain warping," in 2nd IEEE International Workshop on Hot Topics in 3D (Hot3D 2011). IEEE.

[3] "Call for proposals on 3rd video coding technology," ISO/IEC JTC1/SC29/WG11, Geneva, Switzerland, Tech. Rep. N12036, March 2011, approved

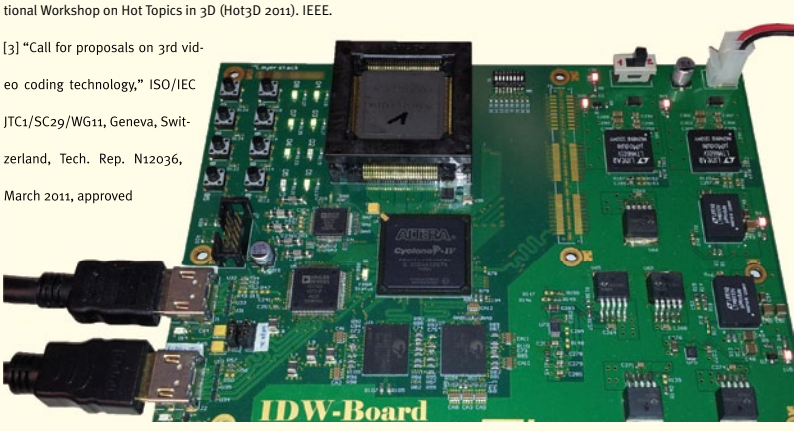


Fig.3. Test environment with MadMax, an Altera Cyclone IV FPGA and two HDMI video links.

List of Customers per country and number of designs they have sent in for MPW fabrication

CUSTOMER	TOWN	Number of ASICs
Australia		
Edith Cowan University	Joondalup	11
La Trobe University	Bundoora, Victoria	1
Monash University	Clayton	3
Motorola Australian Ressearch Centre	Botany	1
Royal Melbourne Inst. of Technology (RMIT)	Victoria	1
University of South Wales	Sydney	7
University of Western Australia	Crawley	1
Austria		
A3Pics	Vienna	1
ARC Seibersdorf Research	Vienna	5
austriamicrosystems	Unterpremstaetten	74
Austrian Academy of Sciences	Wiener Neustadt	1
Austrian Aerospace	Vienna	2
Austrian Institute of Technology - AIT	Vienna	1
Carinthia Tech Institute	Villach-St.Magdalen	1
Fachhochschule Technokum Kaernten	Villach-St.Magdalen	3
FH Joanneum Graz	Graz	1
IEG	Stockerau	1
Johannes Keppler University	Linz	3
MED-el	Insbruck	2
Riegl Laser Measurement System	Horn	3
Securiton	Wien	1
TU Graz	Graz	4
TU Wien	Vienna	19
Univ. of Applied Sciences Technikum Wien	Vienna	1
Belarus		
NTLab	Minsk	6
Belgium		
Alcatel Space	Hoboken	4
Audax Technologies	Leuven	1
AnSem	Heverlee	3
Browning International SA	Herstal	1
Cochlear Technology Centre Europe	Mechelen	9
ED&A	Kapellen	3
EqcoLogic	Brussels	52
Universit de Mons, Faculte Polytechnique	Mons	9
FillFactory	Mechelen	2
ICI - Security Systems	Everberg	6
ICSense	Leuven	1
IMEC	Leuven	209
K.U. Leuven	Heverlee	145
Katholieke Hogeschool Brugge-Oostende	Oostende	23
KHLim	Diepenbeek	9
KHK	Geel	13
KIHA	Hoboken	2
Macq Electronique	Brussel	1
Neurotech	Louvain-la-Neuve	2
Q-Star Test nv	Brugge	2
SDT International	Bruxelles	1
SEBA Service N.V.	Grimbergen	1
SIEMENS ATEA	Herentals	2
SIPEX	Zaventem	4
Societe de Microelectronique	Charleroi	1
Universite catholique de Louvain	Louvain-la-Neuve	16
Universiteit Gent	Gent	87
University of Antwerp	Wilrijk	3
Vrije Universiteit Brussel	Brussels	88
Xenics	Leuven	1
Brazil		
State University of Campinas - CenPRA	Campinas	29
CPqD - Telebras	Campinas	7
Genius Instituto de Tecnologia	Manaus - Amazonas	3
Centro de Tecnologica da Informacao Renato Archer Brasil	Sao Paulo	2
Federal University of Minas Gerais (UFMG)	Belo Horizonte	1
University Federal Pernambuco	Recife	6
UNESP/FE-G	Guaratingueta - SP	3
UNICAMP- University of Campinas	Campinas, SP	30
Universidade de Sao Paulo	Sao Paulo-SP	31
Bulgaria		
Technical University of Sofia	Sofia	4
Canada		
Canadian Microelectronics Corporation	Kingston, Ontario	17
Epic Biosonics	Victoria	4
NanoWattICs	Quebec	1
Queens University	Kingston, Ontario	1
Scanimetrix	Edmonton	12
TBI Technologies	Waterloo	1
University of Alberta	Edmonton	1
University of Toronto	Toronto	1
University of Waterloo	Waterloo	6
China		
Beelab Semiconductor	Hong Kong	1
Dept.Computer Science and Technology	Beijing	1
Fudan University	Shanghai	2
Hirain	Beijing	1
Microelectronics Center	Harbin	1
The Chinese University of Hong Kong	Shatin-Hong Kong	41
University of Macau	Macau	8
The Chinese Univ. of Hong Kong - ASIC Lab	Hong Kong	17
Hong Kong Univ. of Science and Technology	Hong Kong	25
Zhejiang University	Yuquan	1
Costa Rica		
Instituto Tecnologico de Costa Rica	Cartago	1
Croatia		
University of Zagreb	Zagreb	5
Cyprus		
University of Cyprus	Nicosia	2
Czech Republic		
ASICentrum s.r.o.	Praha 4	6
Brno University of Technology	Brno	17
Czech Technical University-FEE	Prague	7
Institute of Physics ASCR	Prague	2

CUSTOMER	TOWN	Number of ASICs
Denmark		
Aalborg University	Aalborg	50
Aalto University	Aalto	7
Algo Nordic A/S	Copenhagen	1
Bang & Olufsen	Struer	4
DELTA	Hoersholm	11
GN-Danavox A/S	Taastrup	4
Microtronic A/S	Roskilde	1
Oticon A/S	Hellerup	14
PGS Electronic Systems	Frb.	1
Techtronic A/S	Roskilde	1
Technical University of Denmark	Lyngby	11
Thrane&Thrane	Lyngby	1
Egypt		
American university of Cairo	Cairo	1
Bahgat Group - IEP	Cairo	4
Estonia		
Tallinn Technical University	Tallinn	1
Finland		
Aalto University	Espro	1
Detection Technology Inc.	Li	1
Fincitec Oy	Oulu	4
Kovilta Oy	Salo	1
Helsinki University of Technology	Espoo	9
Nokia Networks	Espoo	2
Tampere University of Technology	Tampere	8
University of Oulu	Oulu	19
University of Turku	Turku	3
VTI Technologies	Vantaa	2
VTT Electronics	Espoo	107
France		
Atmel	Nantes, Cedex 3	3
C4i	Archamps	14
CCESMAA -IXL	Talence	2
CEA	Grenoble	39
CMP-TIMA	Grenoble	7
CNES	Toulouse Cedex 01	4
CPPM	Marseille	2
Dibcom	Palaiseau	1
Dolphin Integration	Meylan	4
EADS Defense&security		1
ELA Recherche	Meylan	4
ENSEA	Cergy Pontoise	2
ENST Paris	Paris	2
ESIEE	Noisy Le Grand	3
IN2P3 - LPNHE - Universites 6 et 7	Paris Cedex 5	9
Institut des Sciences Nucleaires	Grenoble	5
Institut de Physique Nucleaire	Villeurbanne	7
Institut Sup. d Electronique de Bretagne	Brest	2
ISEN Recherche	Lille cedex	5
LAAS/CNRS	Toulouse	9
Labo PCC CNRS/IN2P3	Paris cedex05	2
Laboratoire de l Accelerateur Lineaire	Orsay	6
Laboratoire de Physique des Plasmas, LPP	Saint-Maur des Fosss	1
LAPP	Annecy-le-Vieux	7
LEA	Cesson Sevigne	1
LEPSI	Strasbourg	15
Ecole Polytechnique route de Saclay , LPP	Palaiseau	1
LETI-CEA	Grenoble	4
LIRMM	Montpellier	2
Midi Ingenierie	Labege	1
MXM Laboratories	Vallauris	3
NeoVision France	Bagneux	3
NXP Semiconductor	Caen	2
PMIPS - IEF	Orsay	2
SODERN	Limeil-Brevannes	2
ISAE	Toulouse Cedex	14
Supelec	Gif-sur-Yvette	3
TTPCOM	Sophia Antipolis	1
Universite Joseph Fourier	Grenoble	1
Universite Pierre et Marie Curie	Paris	4
Vision Integree	Nogent sur Marne	3
Germany		
AEG infrarot-module		1
Albert-Ludwig University - IMTEK	Freiburg	3
ALV-Laser Vertriebsgesellschaft mbH	Langen	1
austriamicrosystems	Dresden	2
Balluff		1
Bergische Universitaet Wuppertal	Wuppertal	2
Biotronik GmbH & Co	Erlangen	9
Bruker AXS	Karlsruhe	3
Bruker Biospin		6
Cairos Technologies	Karlsbad	8
Comtech GmbH	St. Georgen	3
Daimler-Benz AG	Ulm	3
Darmstadt University of Technology	Darmstadt	3
Dr. Johannes Haidenhain		1
ESM Eberline	Erlangen	1
ETA	Erlangen	1
Fachhochschule Aalen	Aalen	3
Fachhochschule Aschaffenburg	Aschaffenburg	2
Fachhochschule Augsburg	Augsburg	1
Fachhochschule Brandenburg	Brandenburg	12
Fachhochschule Bremen	Bremen	3
Fachhochschule Darmstadt	Darmstadt	9
Fachhochschule Dortmund	Dortmund	3
Fachhochschule Esslingen	Goeppingen	2
Fachhochschule Furtwangen	Furtwangen	6
Fachhochschule Giessen-Friedberg	Giessen	16
Fachhochschule Koeln	Gummersbach	3
Fachhochschule Mannheim	Mannheim	3
Fachhochschule Nuernberg	Nuernberg	1
Fachhochschule Offenburg	Offenburg	28
Fachhochschule Osnabrueck	Osnabrueck	4
Fachhochschule Pforzheim	Pforzheim	1
Fachhochschule Ulm	Ulm	18
Fachhochschule Wilhelmshaven	Wilhelmshaven	1
Fachhochschule Wuerzburg	Wuerzburg	1
FAG-Kugelfischer	Schweinfurt	3
FH Hannover	Hannover	5
FH Karlsruhe	Karlsruhe	1
FH Niederrhein	Krefeld	5
FH-Mnster	Steinfurt	1
FORMIKROSYS	Erlangen	2
Forschungszentrum Juelich GmbH	Juelich	2

CUSTOMER	TOWN	Number of ASICs
Fraunhofer Heinrich - Hertz	Berlin	16
Fraunhofer IIS	Erlangen	238
Fraunhofer institute silicontechnology	Itzehoe	18
Fraunhofer IPMS	Dresden	6
Fraunhofer ISC		1
Friedrich-Schiller-University	Jena	3
GEMAC	Chemnitz	7
Gesellschaft fr Schwerionenforschung	Darmstadt	40
Geyer	Nuernberg	6
GMD	St. Augustin	1
Hella		1
Hyperstone AG	Konstanz	1
iAd GmbH	Grosshabersdorf	1
IHP	Frankfurt(Oder)	1
IIP-Technologies GmbH	Bonn	6
IMKO Micromodultechnik GmbH	Ettlingen	3
IMMS	Ilmenau	2
IMST GmbH	Kamp-Lintfort	4
INOVA Semiconductor	Munich	1
Institut fuer Mikroelectronik Stuttgart	Stuttgart	2
Institut fur Mobil- und Satellitenfunktechnik	Kamp-Lintfort	9
Institute for Integrated Systemes	Aachen	1
Institute of Microsystem Techology	Freiburg	2
Jakob Maul GmbH	Bad Koenig	1
Joh.-Wolfgang-Goethe-Universitaet	Frankfurt	5
Johannes Gutenberg-Universitaet	Mainz	9
Karlsruher Institut fuer Technologie (KIT)	Karlsruhe	1
KVG Quatrz Crystal	Neckarbisch	1
Lenze GmbH	Aerzen	2
LHR Comtech	St. Georgen	1
MAN	Nremberg	1
Marquardt GmbH	Rietheim-Weilheim	1
Max Planck Institute	Munchen	11
MAZ Brandenburg	Brandenburg	2
Med-El GmbH		1
MEODAT	Ilmenau	2
Metzeler Automotive		3
MPI-Halbleiterlabor	Munich	2
NeuroConnex	Meckenheim	2
Optek Systems Innovations		1
OPTRONICS		1
Phisikalisches Institut	Bonn	2
Preh Werke	NA	2
Rechner Industrieelektronik GmbH		1
Rohde & Schwarz	Mnchen	2
Ruhr-University Bochum	Bochum	6
RWTH Aachen	Aachen	48
Scanditronix Wellh fer	NA	3
Schleicher GmbH & Co Relais-Werke KG		1
Schleifring und Apparatebau GmbH		3
Seuffer	Calw-Hirsau	5
Sican Braunschweig GmbH	Braunschweig	1
Siemens		4
Technical University Ilmenau	Ilmenau	75
Technical University of Berlin	Berlin	11
Technische Hochschule Mittelhessen	Friedberg	1
TESAT-Spacecom	Backnang	3
Trias	Krefeld	1
Trinamic	Hamburg	1
TU Berlin	Berlin	13
TU Braunschweig	Braunschweig	12
TU Chemnitz	Chemnitz	12
TU Darmstadt	Darmstadt	15
TU Dresden	Dresden	28
TU Hamburg-Harburg	Hamburg	51
Universitaet Dortmund	Dortmund	2
Universitaet Hannover	Hannover	13
Universitaet Kaiserslautern	Kaiserslautern	19
Universitaet Paderborn	Paderborn	14
Universit		
t Rostock	Rostock	8
University of Bonn	Bonn	11
University of Bremen	Bremen	37
University of Erlangen-Nuernberg	Erlangen	32
University of Freiburg	Freiburg	11
University of Hamburg, HAW - Applied Sciences	Hamburg	2
University of Heidelberg	Heidelberg	83
University of Kassel	Kassel	5
University of Magdeburg	Magdeburg	13
University of Mannheim	Mannheim	36
University of Munich	Munich	1
University of Oldenburg	Oldenburg	1
University of Saarland	Saarbruecken	4
University of Siegen	Siegen	17
University of Stuttgart	Stuttgart	1
University of Ulm	Ulm	27
Vishay semiconductor	Heilbronn	2
Wellhoeffer	Schwarzenbruck	2
Work Microwave GmbH	Holzkirchen	1
Greece		
ACE Power Electronics LTD	AG Dimitrios	1
Aristotle Univ. of Thessaloniki	Thessaloniki	12
Athena Semiconductors SA	Alimos - Athens	2
Crypto SA	Marousi	1
Datalabs	Athens	1
Democritus University of Thrace	Xanthi	5
Found. for Research and Techn.-Hellas	Heraklion	1
InAccess	Athens	1
HELIC SA	Athens	1
Hellenic Semiconductor Applications	Athens	2
Intracom	Paiania	1
National Tech. Univ. of Athens	Athens	16
NCSR	Athens	23
NTNU	n/a	2
RETECO LTD.	Athens	1
Technical University of Crete	Crete	1
Technological Educational Institute of Chalkis		Chalkis
3		
Unibrain SA	Athens	1
University of IONNINA	Ioannina	2
University of Patras - VLSI Laboratory	Rio - Patras	24
Hungary		
Hungarian Academy and Science	Budapest	2
Peter Pazmany Catholic University	Budapest	5
Computer and Automation Inst.	Budapest	6
JATE University	Szeged	1
India		
Bengal Engineering and Science University	Shibpur	1
CEERI	Pilani	7
College of Eng. Guindy Anna Univesity	Chennai	2
Concept2Silicon Systems	Bangalore	1
Electronics Corporation of India	Hyderabad	15
Indian Institute of Science	Bangalore	19

CUSTOMER	TOWN	Number of ASICs
Indian Institute of Technology - Bombay	Mumbai	13
Indian Institute of Technology - New-Dehli	New Dehli	14
Indian Institute of Technology, Kanpur	Assam	2
Indian Institute of Technology, Kharagpur	Kharagpur	11
Indian Institute of Technology - Madras	Chennai	39
Indian Institute of Science	New Dehli	6
Integrated Microsystem	Gurgaon	1
National Institute of Technology, Karnataka	Surathkal	1
National Institute of Technology Trichirappalli	Trichirappalli	1
SITAR	Bangalore	28
TIFR	Colaba	1
VECC	Kolkata	6
Ireland		
ChipSensors Ltd	Limerick	3
Cork Institute of Technology	Cork	3
Duolog LtD	Dublin	2
National University of Ireland	Kildare	3
Farran Technology	Ballincollig	1
Tyndall National Institute	Cork	20
Parthus Technologies (SSL)	Cork	7
TELTEC	Cork	1
University College Cork	Cork	15
University of Limerick	Limerick	17
Waterford Institute of Technology	Waterford	8
Israel		
CoreQuest	Petach Tikva	2
Check - Cap Ltd	Isfiya	1
DSP Semiconductors	Givat Shmuel	1
Technion - Israel Institute of Techn.	Haifa	4
Tel Aviv University	Tel Aviv	6
Italy		
Alcatel Alenia	L'Aquila	1
Agemont	Amaro	1
Alimare SRL	Favria Canavese (Torino)	1
Aurelia Microelettronica S.p.A.	Navacchio PISA	18
BIOTRONIC SRL	San Benedetto	1
Cesvit Microelettronica s.r.l.	Prato	2
DEEI - University of Trieste	Trieste	2
Fondazione Bruno Kessler	Trento	53
INFN	Bari	1
INFN	Bologna	1
INFN	Cagliari	1
INFN	Catania	15
INFN	Ferrara	1
INFN	Genova	2
INFN	Milano	10
INFN	Padova	4
INFN	Roma	5
INFN	S.Piero a Grado (PISA)	2
INFN	Torino	8
INFN	Trieste	10
Instituto di Sanita	Roma	4
IIT - Instituto Italiano di Tecnologia	Torino	1
ISE	Vecchiano	1
Italian Institute of Technology	Genova	10
LABEN S.p.A.	Vimodrone (MI)	3
Microgate S.r.L	Bolzano	5
Microtest	Altopascio	1
Neuricam	Trento	3
Optoelettronica Italia	Terlago	1

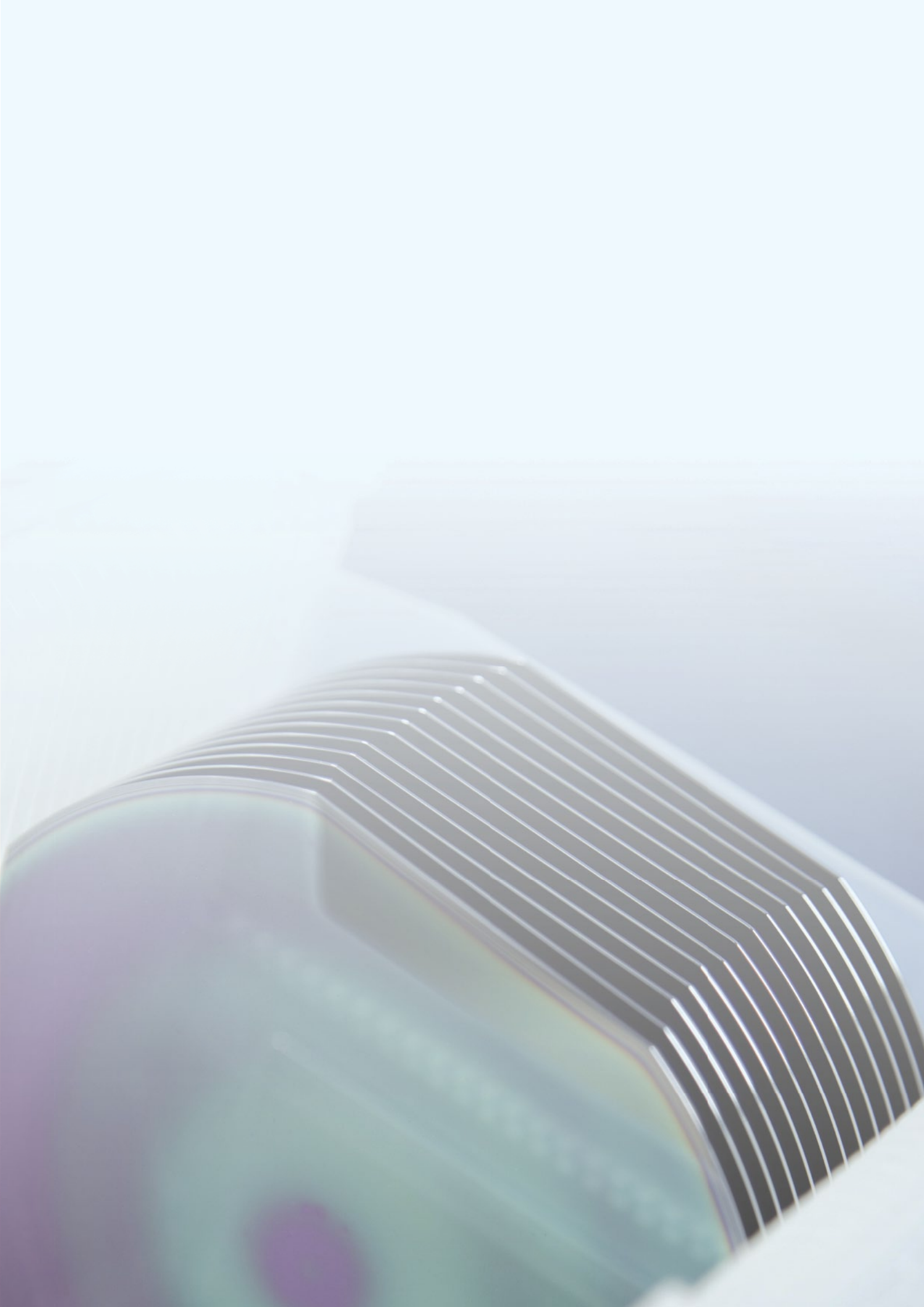
CUSTOMER	TOWN	Number of ASICs
Politecnico di Bari	Bari	8
Politecnico di Milano	Milano	118
Politecnico di Torino	Torino	7
Scuola Superiore Sant'Anna	Pisa	4
Silis s.r.l	Parma	1
Sincrotrone Trieste SCpA	Trieste	3
SITE Technology s.r.l.	Oricola	1
SYEL S.r.l.	Pontadera	1
Universita degli Studi Dell Aquila	L Aquila	3
Universita di Torino	Torino	7
Universit degli Studi di Ancona	Ancona	4
Universita degli Studi di Firenze	Firenze	3
Universita della Calabria	Arcavacata di Rende	1
Universita di Cagliari	Cagliari	17
Universita di Catania	Catania	38
University of Bologna	Bologna	30
University of Brescia	Brescia	12
University of Genova	Genova	15
University of Milano-Bicocca	Milano	3
University of Modena and Regio Emilia	Modena	4
University of Naples	Napoli	6
University of Padova	Padova	29
University of Parma	Parma	13
University of Pavia	Pavia	16
University of Perugia	Perugia	7
University of Pisa	Pisa	27
University of Rome La Sapienza	Roma	1
University of Rome Tor Vergata	Roma	10
University of Salento	Lecce	5
University of Siena	Siena	2
XGLab	Milano	7
Japan		
MAPLUS	Kitsuki-City	1
Marubeni Solutions	Osaka	11
Hokkaido University	Sapporo	21
Kobe University	Kobe	9
Rigaku Corporation	Tokyo	6
Tokyo Institute of Technology	Tokyo	1
Yamatake	Kanagawa	1
Korea		
3SoC Inc.	Seoul	1
JOSUYA TECHNOLOGY	Taejon	1
KAIST	Daejeon	3
Korean Elektrotechnology Research Institute	Changwon	1
Macam Co., Ltd	Seoul	2
M.I.tech Corp.	Gyeonggi-do	1
Nurobiosys	Seoul	10
Radtek	Yusung-Ku, Daejeon	1
Samsung Advanced Institute of Technology	Yongin-si Gyeonggi-do	5
Samsung Electro-Mechanics	Suwon	1
Seoul National University	Seoul	7
Seloco	Seoul	40
SoC8611	Gyeonggi-do	3
SML	Seoul	7
Lebanon		
American university of Beirut	Beirut	1

CUSTOMER	TOWN	Number of ASICs
Malaysia		
MIMOS	Kuala Lumpur	1
SunSem Sdn. Bhd.	Kuala Lumpur	1
University of Technology	Skudai	1
Malta		
University Of Malta	Msida	15
Mexico		
INAOE	Puebla	31
Netherlands		
Aemics	Hengolo	8
ASTRON	Dwingeloo	1
Catena Microelectronics BV	Delft	1
Cavendish Kinetics	's Hertogenbosch	1
Delft University of Technology	Delft	178
ESA - ESTEC	AG Noordwijk ZH	4
GreenPeak Technology	Utrecht	12
Hogeschool Heerlen	Heerlen	1
IMEC-NL	Eindhoven	46
Intrinsic-ID	Eindhoven	1
Lucent Technologies Nederland BV	Huizen	1
Mesa Research Institute	Twente	4
NFRA	Dwingeloo	1
Nikhef	Amsterdam	5
Smart Telecom Solutions		1
Sonion	Amsterdam	3
SRON	Utrecht	13
Technische Universiteit Eindhoven	Eindhoven	47
TNO - FEL	The Hague	18
TNO Industrie	Eindhoven	1
University of Amsterdam	Amsterdam	1
University of Twente	Enschede	5
Xensor Integration	Delfgauw	3
New Zealand		
Industrial Research Ltd	Lower Hutt	4
Massey University	Albany	1
Norway		
AME As	Horten	1
IDE AS	Oslo	2
Interon	Asker	19
Nordic VLSI	Trondheim	38
Norwegian Institute of Technology	Trondheim	21
Novelda	Oslo	1
Nygon	Asker	1
SINTEF	Trondheim	19
University of Bergen	Bergen	6
University of Oslo	Oslo	84
Vestfold University College	Tonsberg	2
Poland		
AGH University of Science and Technology	Krakow	75
Institute of Electron Technology	Warsaw	46
Military University of Technology	Warsaw	2
Technical University of Gdansk	Gdansk	9
Technical University of Lodz	Lodz	10
University of Mining and Metallurgy	Krakow	24
University of Technology & Agriculture	Bydgoszcz	1
University of Technology - Poznan	Poznan	2
Warsaw University of Technology	Warsaw	19
Portugal		
Acacia Semiconductor	Lisboa	6
Chipidea	Oeiras	22
INESC	Lisboa	37
INETI	Lisboa	1
Instituto de Telecomunicacoes	Lisboa	33
Instituto Superior Tecnico	Lisboa	6
Universidade de Aveiro	Aveiro	19
University of Minho	Guimaraes	7
University of Porto	Porto	13
ISEL-IPL	LIsboa	1
University of Tras-os-Montes e Alto	Vila Real	3
Universidade Nova de Lisboa - Uninova	Caparica	10
Puerto Rico		
University of Puerto Rico	Mayaguez	1
Romania		
National Inst. for Physics and Nuclear Engineering	Bucharest	1
Polytechnic inst. Bucharest	Bucharest	1
Russia		
IPMCE	Moscow	3
"JSC ""NTLAB"""	Moscow	2
Moscow Institute of Electronic Technology	Moscow	5
Moscow Institute of Physics and Technology	Moscow	3
Moscow Engineering Physics Institute	Moscow	14
N.I. Lobachevsky State Univ	Nizhni Novgorod	7
SRIET-SMS CJSC	Voronezh	5
University St Petersburg	St Petersburg	3
Vladimir State university	Vladimir	1
Saudi Arabia		
King Abdullah Univ. of Science and Technology	Thuwal	4
King Saud University	Riyadh	1
Serbia and Montenegro		
University of Nis	Nis	2
Singapore		
Agilent	Singapore	2
DSO National Laboratories	Singapore	6
Nanyang Technology University	Singapore	3
Slovakia		
Inst. of Computer Systems	Bratislava	1
Slovak University of Technology	Bratislava	5
Slovenia		
Iskraemeco d.d.	Kranj	19
NOVOPAS	Maribor	1
University of Ljubljana	Ljubljana	8
University of Maribor	Maribor	1
South Africa		
Solid State Technology	Pretoria	8
University of Pretoria	Pretoria	31
South America		
CNM/Iberchip		74

CUSTOMER	TOWN	Number of ASICs
Spain		
Acorde S.A.	Santander	29
Anafocus	Sevilla	2
CNM	Bellaterra	87
Design of Systems on Silicon	Paterna	7
EUSS	Barcelona	1
Facultad de Informatica UPV/EHU	San Sebastian	2
Oncovision	Valencia	2
Technical University of Madrid	Madrid	3
Univ. Las Palmas Gran Canaria	Las Palmas de Gran Canaria	17
Universidad Autonoma de Barcelona	Barcelona	15
Universidad Carlos III Madrid	Madrid	1
Universidad de Cantabria	Santander	32
Universidad de Extremadura	Badajoz	27
Universidad de Navarra	San Sebastian	36
Universidad de Santiago de Compostela	Santiago de Compostela	2
Universidad del Pais Vasco	Bilbao	3
Universidad Politecnica de Cartagena	Cartagena	4
Universidad Politecnica de Madrid	Madrid	1
Universidad Publica de Navarra	Pamplona	16
Universitat de Barcelona	Barcelona	46
Universitat Illes Balears	Palma Mallorca	3
Universitat Politecnica de Catalunya	Barcelona	44
Universitat Rovira i Virgili	Tarragona	2
University of Malaga	Malaga	3
University of Seville	Sevilla	82
University of Valencia	Valencia	1
University of Valladolid	Valladolid	1
University of Vigo	Vigo	3
University of Zaragoza	Zaragoza	31
Sweden		
Bofors Defence AB		2
Chalmers University	Goteborg	6
Chalmers University of Technology	Gothenburg	66
Defence Researh Establishment	Linkoping	5
Ericsson	Molndal	2
Ericsson Microelectronics	Kista	2
Halmstad University	Halmstad	2
Institutet for Rymdfysik	Kiruna	1
Imego AB	Goteborg	1
Lulea University of Technology	Lulea	10
Lund University	Lund	178
Malardalens University	Vasteras	2
Mid Sweden University	Sundsvall	12
Royal Institute of Technology	Kista	34
RUAG Aerospace Sweden	Goteborg	2
SiCon AB	Linkoping	4
Svenska Grindmatriser AB	Linkoping	3
University of Trollhattan	Trollhattan	3
University of Link ping	Link ping	157
Uppsala University	Uppsala	11
Switzerland		
Agilent Technologies	Plan-les-Ouates	2
Asulab SA	Marin	22
austriamicrosystems		2
Bernafon	Bern	1
Biel School of Engineering	Biel	9
CERN	Geneva	24
CSEM	Zurich	57
CT-Concept		9

CUSTOMER	TOWN	Number of ASICs
Ecole d'ingenieurs de Geneve	Geneve	1
Ecole d'ingenieurs et d'Archtectes	Fribourg	6
EPFL IMT ESPLAB	Neuchatel	13
EPFL Lausanne	Lausanne	280
ETH Zurich	Zurich	155
HMT Microelectronics Ltd	Biel/Bienne	3
Hochschule Rapperswill	Rapperswill	1
HTA Luzern	Horw	2
HTL Brugg-Windisch	Windisch	2
id Quantique	Carouge	19
Innovative Silicon S.A.	Lausanne	1
Institut MNT	Yverdon-les-Bains	1
Institute of Microelectronics, Uni. of Applied Sciences Northwest	Windisch	2
University of Applied Sciences HES-SO	Valais	2
Landis + Gyr AG		1
Leica Geosystems	Heerbrugg	1
LEM	Plan-les-Ouates	3
MEAD Microelectronics S.A.	St-Sulpice	2
MICROSWISS	Rapperswil	2
Paul-Scherrer-Institute	Villigen	17
Photonfocus	Lachen	3
Senis	Zurich	1
Sensima technologies	Nyon	5
Sensirion	Staefa	2
Sentron AG	Lausanne	7
siemens	Zug	2
Smart Silicon Systems SA	Lausanne	2
Suter IC-Design AG	Waldenburg	4
University of Neuchatel	Neuchatel	22
University of Zurich	Zurich	60
Uster Technolgies	Uster	1
Xemics SA - CSEM	Neuchatel	33
Taiwan		
Feng Chia University	Taichung	1
National Cheng Kung University		1
National Tsing Hua University	Hsinchu	4
Thailand		
Microelectronic Technologies	Bangkok	2
NECTEC	Bangkok	34
Turkey		
ASELSAN	Ankara	1
Bahcesehir Universitesi	Istanbul	1
Bilkent University	Ankara	6
Bogazici University	Istanbul	15
Istanbul Technical University	Istanbul	25
Kardiosis	Ankara	1
KOC University	Istanbul	1
Kocaeli University	Izmit	1
Middle East Technical Univ.	Ankara	9
Sabanci University	Istanbul	20
Tubitak Bilten	Ankara	4
Yeditepe University	Istanbul	5
United Kingdom		
Aberdeen University	Aberdeen	1
Barnard Microsystems Limited	London	2
Bournemouth University	Poole	3
Bradford University	Bradford	7
Brunel university	Uxbridge	1

CUSTOMER	TOWN	Number of ASICs
Cadence Design Systems Ltd	Bracknell	1
Cambridge Consultants Ltd.	Cambridge	3
Cardiff University	Cardiff	5
CCLRC - RAL	Oxon	57
CML Microcircuits Ltd.	Maldon	19
Control Technique	Newtown	4
Data Design & Developmentsq	Stone	1
Dukosi	Edinburgh	2
Edinburgh University	Edinburgh	66
ELBIT Systems Ltd.		1
Epson Cambridge research lab	Cambridge	2
Heriot-Watt University	Edinburgh	2
Imperial College	London	53
Jennic Ltd	Sheffield	1
K.J. Analogue Consulting	Malmesbury	1
King's College London	London	1
Lancaster University	Lancaster	7
Leicester University	Leicester	1
Middlesex University	London	6
Napier University	Edinburgh	4
National Physical Laboratory	Teddington	3
Nokia Research Center	Cambridge	1
Nortel	Harlow	1
Plextek Ltd	Essex	4
Positek Limited	Glos	1
Roke Manor Research Ltd.	Southampton	11
Saul Research	Towcester	22
Sheffield Hallam University	Sheffield	1
Sofant Technologies	Edinburgh	1
Swansea University	Swansea	1
Swindon Silicon Systems Ltd	Swindon	3
Tality	Livingston	1
The Queens University of Belfast	Belfast	5
The University of Hull	Hull	1
The University of Liverpool	Liverpool	14
UMIST	Manchester	57
University College London-UCL	London	2
University of Bath	Bath	24
University of Birmingham	Birmingham	6
University of Brighton	Brighton	1
University of Bristol	Bristol	3
University of Cambridge	Cambridge	30
University of Dundee	Dundee	1
University of East London	London	1
University of Glasgow	Glasgow	43
University of Hertfordshire	Hatfield	1
University of Kent	Canterbury	13
University of London	London	38
University of Newcastle upon Tyne	Newcastle upon Tyne	17
University of Nottingham	Nottingham	39
University Of Oxford	Oxford	28
University of Plymouth	Plymouth	2
University of Reading	Reading	1
University of Sheffield	Sheffield	7
University of Southampton	Southampton	33
University of Stirling	Stirling	1
University of Surrey	Guildford	6
University of the West of England	Bristol	2
University of Wales, Aberystwyth	Aberystwyth	5
University of Warwick	Coventry	5
University of Westminster	London	7
University of York	Heslington	1
Walmsley (microelectronics) Ltd	Edinburgh	1
USA		
Analog	Phoenix	1
Arizona State University	Tempe	17
austriamicrosystems USA		1
Boston university	Boston	11
Brookhaven National Laboratory	Upton, NY	1
Carnegie Mellon University	Pittsburgh	1
Columbia University	Irvington, New York	18
Discera		1
Duke Universtity	Durham	1
Eutecus Inc	Berkeley	3
Exelys Ilc	Los Angeles	2
Flextronics	Sunnyvale	1
Forza Silicon Corporation	Pasadena	1
Fox Electronics	Fort Myers	5
Future Devices		1
General Electric	Niskayuna	3
Glacier Microelectronics	San Jose	1
Goddard Space Flight Center, NASA	Greenbelt	1
Intellectual Property, LLC	Cross Plains	1
Intrinsix	Fairport	1
Iwatsu	Irving	4
Kaiam Corporation	Newark	1
Lawrence Berkeley National Laboratory	Berkeley	5
Linear Dimensions, Inc.	Chicago	1
Micrel Semiconductor	San Jose	11
Microchip Technology		1
MIT - Lincoln Lab	Cambridge	25
MOSIS	Marina del Rey, CA	54
Neofocal Systems	Portland	8
Nova R&D	Riverside	3
Parallax Inc.	Rocklin	2
Philips Medical Systems	Andover	1
Princeton University	Princeton, NJ	4
Rockwell Scientific	Thousand Oaks, CA	13
Signal Processing Group	Chandler	1
Stanford Linear Accelerator	Meno Park	11
Symphonix	San Jose	5
Tachyon Semiconductor	Naperville, IL	2
Tekwiss USA, Inc	Costa Mesa	2
Telemetric Medical Applications	Los Angeles	1
Triad Semiconductor		1
TU Dallas	Richardson	1
University of California	Santa Cruz	1
University of Chicago	Illinois	3
University of Colorado	Boulder	5
University of Delaware	Newark	3
University of Florida	Gainesville	5
Univ. of Maryland - Joint Quantum Institute	Maryland	2
University of Pennsylvania	Philadelphia, Pa.	2
University of Texas at Austin	Austin	27
University of Washington	Seattle	2
USRA	Washington	1
Vectron International Inc.	Hudson NH	5
Xerox	El Segundo	1
Yanntek	San Jose, CA	5



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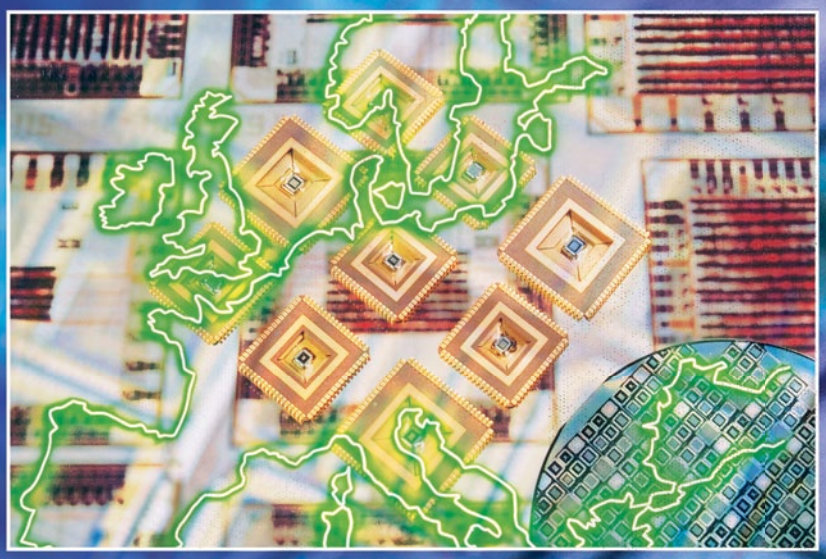

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SEVENTH FRAMEWORK PROGRAMME

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