ACTIVITY REPORT 2017

EUROPRACTICE

EUROPRACTICE

EUROPRACTICE IC SERVICE

ASIC DESIGN AND MANUFACTURING FOR INDUSTRY AND ACADEMIA

EUROPRACTICE was launched by the European Commission in 1989 to help companies improve their competitive position in world markets by adopting ASIC, Multi-Chip Module or Microsystems solutions in the products they manufacture. The program helps to reduce the perceived risks and costs associated with these technologies by offering potential users a range of services, including initial advice and ongoing support, reduced entry costs and a clear route to chip manufacture and product supply. The ultimate goal of EUROPRACTICE is to enhance European industrial competitiveness in the global marketplace. Their services are open to industrial companies (especially SMEs), research institutes and academic users.

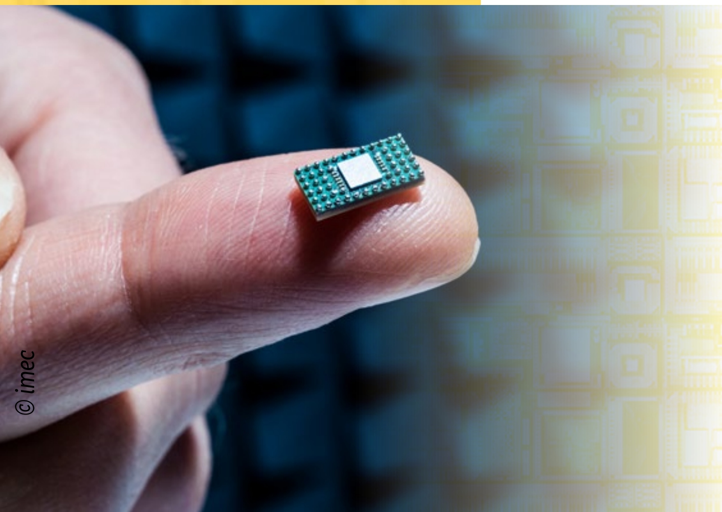
SERVICES OFFERED TO EUROPEAN ACADEMIC INSTITUTIONS:

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by offering more than 600 European universities and research institutes affordable access to the latest IC (Integrated Circuits) design tools and technologies. This is reflected in the training provided by universities from which the best IC design engineers emerge, essential for the SMEs innovation in new IC products.

- Affordable access to industry-standard and state-of-the-art CAD tools
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- Low-cost prototyping in various technologies (both ASIC and More than Moore) via MPW runs
- Training courses in advanced design flows

IC SERVICES OFFERED TO THE GLOBAL INDUSTRY:

EUROPRACTICE also offers industry worldwide access to microelectronic and microsystem design services, MPW prototyping, small volume production, packaging and test operations. Note, this does not include access to design tools.
Industry from all over the world have rapidly discovered the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who do not always need the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise. This you can get all from EUROPRACTICE IC service, a service that is already established for 20 years in the market.



THE EUROPRACTICE SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:

- imec, Leuven (Belgium)
- Fraunhofer-Institut für Integrierte Schaltungen (Fraunhofer IIS), Erlangen (Germany)
- STFC Rutherford Appleton Laboratory (United Kingdom)

FOREWORD

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Dear colleagues and friends,

2017 was a busy year with a record-number of designs taped out through our Europractice service. We realized a total of 614 tape-outs in a wide range of technologies with 70% of the designs submitted by European universities and research institutes with the remaining 30% of the designs from non-European universities (20%) and commercial companies (10%).

The trend of pushing towards smaller technologies continued in 2017, where we realized 7 design tape-outs in the 22nm FDSOI technology from GLOBALFOUNDRIES. Also, the number of designs in Silicon Photonics and MEMS has increased considerably compared to 2016, which is thanks to the high number of designs in the imec Si-photonics technologies (namely 59 designs in total). Finally, many of our foundries improved their portfolio for example with advanced packages such as Wafer Level Chip Scale Package (WLCSP), Flip Chip Bumping, Through Silicon Via (TSV) and soon Fan-Out Wafer-Level packaging (FOWLP). In 2018 and the years to come we will continue to innovate our offering by providing a good mix of different technologies and design tools.

To help ensure that Europe remains competitive in this sector (IP, IC, MEMS, heterogeneous systems) and retain high-value design roles within Europe, it is absolutely necessary that European industry and innovative start-ups have enough high quality well-trained engineers graduating from university. Thanks to the continuously evolving EUROPRACTICE service, more than 600 European universities, research institutes and over 300 small and medium-sized companies are provided with a vital infrastructure. EUROPRACTICE has grown to become an indispensable part of the European research and training landscape and part of the solution to helping Europe remain competitive.

In the recent years, Europractice has launched multiple first-user Stimulation Actions (supported by EU funding). After initial design competitions to stimulate European universities to design a first IC in standard 0.18 μ technology or to start a first IC in an advanced technology (90nm and beyond) this was continued in 2017 with new competitions to stimulate fabrication of Si-Photonics and MEMS designs. In both categories, the 5 winning designs were selected by an Independent Committee and the designs are expected to be fabricated during the course of 2018. Some examples of these selected designs are described further in this report.

We thank the European Commission (DG Connect) for their support. The current EUROPRACTICE 2016 project has been extended till 31 December 2018 and in April this year a new successor project proposal will be submitted to secure the EC funding until 2020 and beyond. This EC funding will ensure that we can continue our commitment to continue the EUROPRACTICE service and to offer our members easy and affordable access to state-of-the-art design tools and to IC technologies.

Last but not least we thank all of you, our customers, universities and research institutes; our technology and design tool suppliers; for supporting our services and we wish you all a successful 2018.

Looking forward to another successful year.

Romano Hoofman (project manager EUROPRACTICE2016)
and the entire Europractice team

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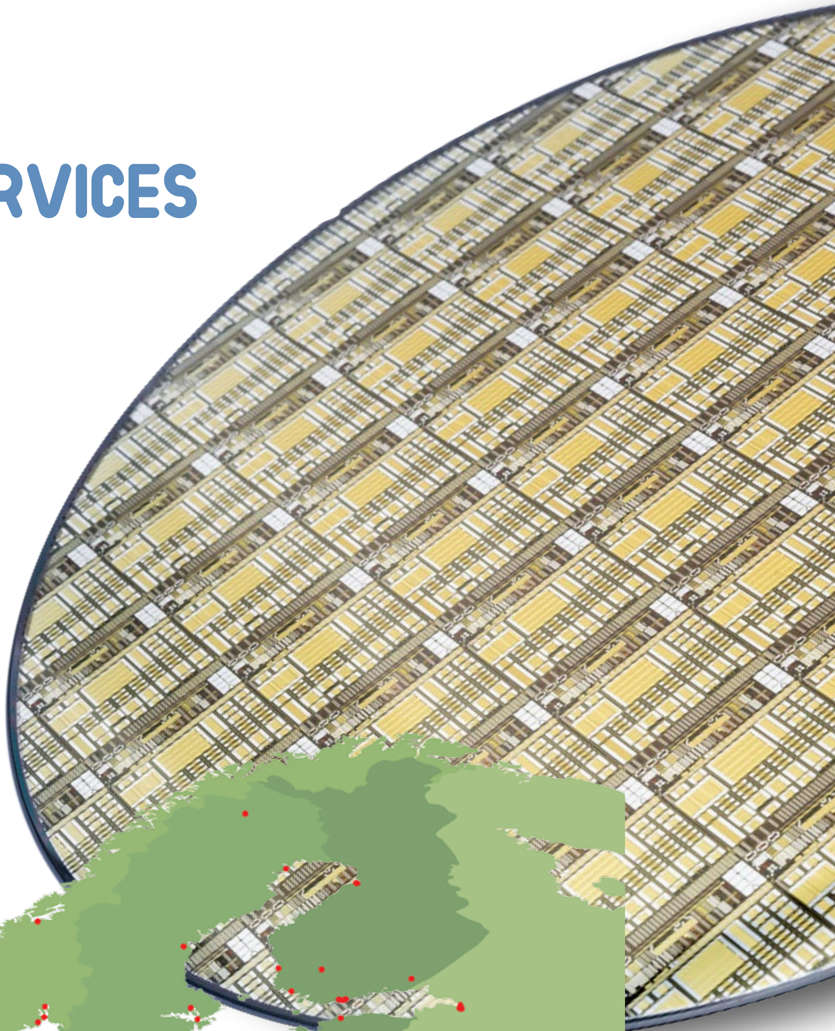
EUROPRACTICE SERVICES

NOW ACTIVE FOR MORE THAN 25 YEARS



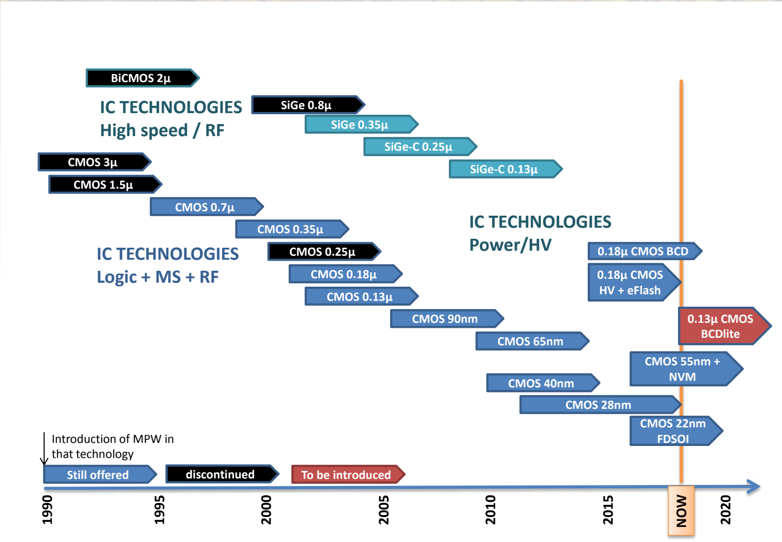
The European Commission has financially supported broker services that offer the European universities, researchers appropriate access to CAD tools, advanced technologies, design kits, IP blocks and training to support their education, prototyping and small volume production. These services have been offered by EUROCHIP (1989-1995) and multiple phases of EUROPRACTICE projects (1995-present) and are widely recognized as world-leading. Currently approximately 600 academia from the EU member States and "extended" Europe are supported by this EUROPRACTICE service funded by the EC. Eligible institutions are currently able to access CAD services and MPW services at discounted prototyping prices.

AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated low cost prices with the major CAD vendors world-wide and also with IP and programmable device vendors. Consequently, European academic institutions can purchase EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics, ...) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service also provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows them to participate in EC-funded projects, ranging from IP block and component design to complete system design.

MPW PROTOTYPING FOR CUSTOMIZED ASICS



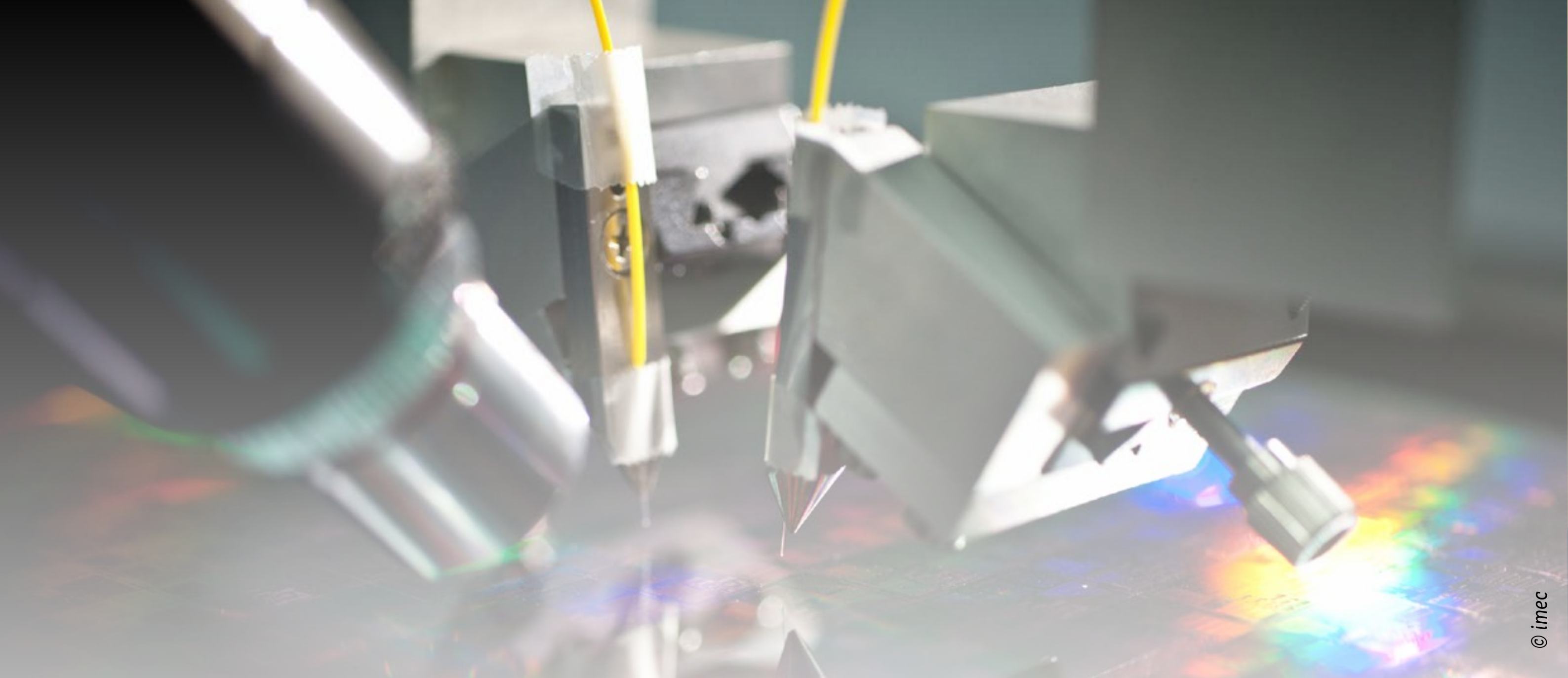
In general, foundries are not willing to give access to their fabrication lines to academic institutes and small companies due to the high level of technical support required, unless a high-volume production is guaranteed – which is not the case for university prototype fabrication or SME small volume needs.

Over the last 15 years, leading IC-foundries have recognized that EUROPRACTICE is the ideal partner to offer MPW services to smaller users and academia as EUROPRACTICE is the entity that offers both access and technical support (and the foundry does not need to bother with the large scale of users). Currently, 5 of the 7 foundries have ASIC manufacturing facilities in Europe (namely OnSemi, ams, IHP, X-FAB and GLOBALFOUNDRIES).

The EUROPRACTICE IC Service watches closely not only the evolution in scaling logic CMOS technologies but also the evolution of new add-ons for the standard CMOS technology such as SiGe, RF, SOI, etc. MPW runs in new and/or add-ons in existing technologies will be installed when there is sufficient demand from its users and when financially viable. Over the last 20 years, new technologies have been introduced by EUROPRACTICE (and EUROCHIP 1989-1995) from 3µ to 22nm today.

The EUROPRACTICE-PLUS partners have installed a comprehensive support infrastructure with the following tasks:

1. Negotiating with foundries and cell library vendors to introduce new technologies and associated new or updated technical information (documentation, design kits, cell libraries),
2. Checking new design kits and adapting existing design kits received from the foundry to CAD versions,
3. Completion of NDAs with academics in order to distribute the design kits and libraries (currently more than 4000 NDA's in place),
4. Distribution of design kits and libraries under NDA control,
5. Providing technical support to European Academia for teaching and IC design on the different design flows in the different CAD tools, cell libraries (models, cell information, RAM, ROM, spice parameters, models, ..), technologies issues (thickness of layers, specific characteristics, special process information not available in the standard documentation, ...), and also checking of their designs before fabrication.



MPW PROTOTYPING FOR MORE-THAN-MOORE TECHNOLOGIES

For several years, EUROPRACTICE has offered CAD tools and MPW runs for discrete MEMS design in MEMSCAP technologies, which include Poly-MUMPs, SOI- MUMPs and piezo-MUMPs. In addition, Teledyne Dalsa MEMS MIDIS technology has also been offered through CMC in Canada as part of the cooperation between the MPW centers worldwide. The Teledyne Dalsa technology can be used for accelerometers, gyroscopes, resonators, inertial sensors or combinations of those. In 2018, it is expected that the MEMS offering will be extended with X-FAB MEMS technologies.

Besides the traditional MEMS technologies, EUROPRACTICE also offer optical photonics technologies (in particular Si-photonics). The MPW service in these technologies at CEA-Leti and IMEC was set-up in ePIXfab, but has been transferred to EUROPRACTICE since 2015. In addition, IHP offers an integrated SiGe-Photonics technology based on their SG25H4 high frequency technology. EUROPRACTICE also offers photonics packaging together with Tyndall National Institute in Ireland. The photonics ecosystem continues to gather momentum attracting new users (both from academia and from industry) and increasing technical scope of the photonics offering via EUROPRACTICE. Research and development continues to be active amongst telecom, datacom and bio-sensing sectors.

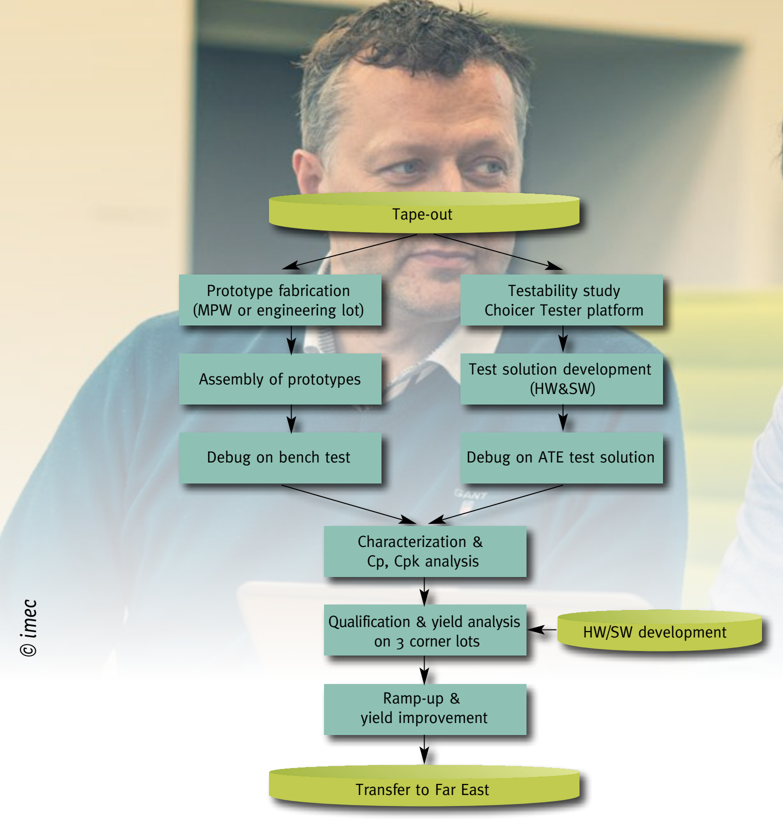
All-in-all, this is a significant More-than-Moore portfolio, which complements the ASIC portfolio. The offered MPW services in these selected technologies are set up in the same way as described for the ASICs including technical support, distribution of foundry design kits, etc.

BACKEND OPERATION SERVICES

Standardly, EUROPRACTICE delivers unpackaged untested prototypes. However, EUROPRACTICE offers a low cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of packages are available ranging from DILs to PGAs and QFNs.

Side by side with world class partners and our long-term agreements, Europractice boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management. The most relevant companies involved in our semiconductor supply chain are listed below:

- **Foundry partners:** TSMC, UMC, ON Semi, ams, IHP, X-FAB, GLOBALFOUNDRIES, MEMSCAP, imec and CEA-LETI
- **Ceramic assembly partners:** HCM.Systrel, Optocap, Kyocera
- **Plastic assembly partners:** ASE, Kyocera
- **Wafer bumping partner:** Pactech, ASE
- **Test partners:** ASE, Microtest, Delta, RoodMicrotec and Blue test
- **Failure analysis:** Maser Engineering
- **Library partners:** Faraday, ARM, eMemory



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FROM PROTOTYPES TO VOLUME PRODUCTION

After successful ASIC prototyping, the Europractice partners (Fraunhofer IIS and imec) can also provide the customer access to the full production and qualification stage (from low to mid-high volumes).

PROTOTYPE FABRICATION

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. Europractice will take care of the production for the first prototypes of the customer and organize the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program.

The devices can be tested on both wafer level as well on packaged devices. The goal is to reduce the test time and to test the ASIC for manufacturing problems using the ATPG and functional patterns.

Europractice will support you during the development of single site test solution as well as with a multi-site test solution when high volume testing is required. Based on the test strategy followed diverse type of implementations can be realized.

DEBUG AND CHARACTERIZATION

Before going into production, a characterization test program will check if all the ASIC specifications are met according to the customer expectations. Threshold values are defined for each tested parameter. The software will test all different IP blocks and the results will be verified with the bench test results.

A characterization at Low (LT), Room (RT) and High (HT) temperature will be performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be strong against process variations, the product qualification can start. Europractice can support you through the full qualification process using different kind of qualification flows ranging from Consumer, Industrial, Medical to Space according to the Military, Jedec and ESCC standards....

In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

SUPPLY CHAIN MANAGEMENT

Europractice is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.

Customer products are treated internally as projects and followed closely by the imec engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. Europratice therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

YIELD IMPROVEMENT

Europractice can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the qualification of the device on 3 different corner lots, Europractice can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers will be analyzed to check for yield issues related to assembly or wafer production. Europractice is using the well proven tool Examinator™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.

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LOW COST IC PROTOTYPING

The cost of producing a new ASIC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. This is largely due to the NRE (Non-Recurring Engineering) overheads associated with design, manufacturing and test.
EUROPRACTICE has reduced the NRE, especially for ASIC prototyping, by two techniques:

1. Multi Project Wafer Runs or
2. Multi Level Masks.

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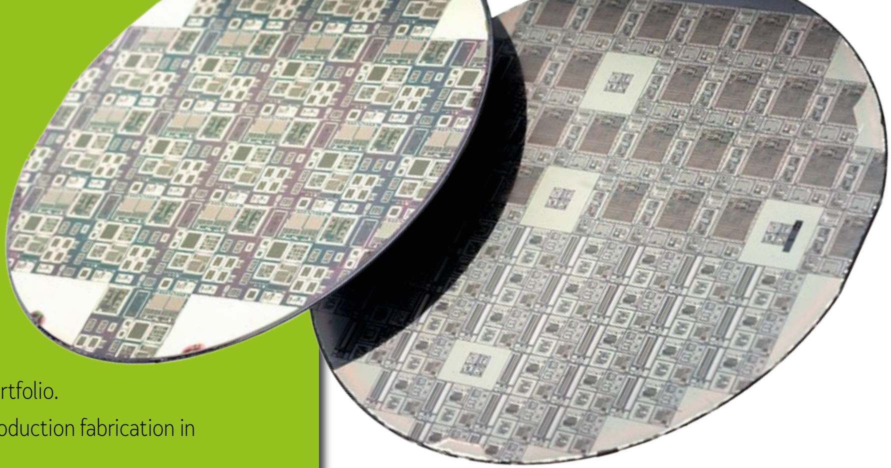
MULTI PROJECT WAFER RUNS

By combining several designs from different customers onto one mask set and prototype run, known as Multi Project Wafer (MPW) runs, the high NRE costs of a mask set is shared among the participating customers.
Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full prototyping wafer run. A limited number of tested or untested ASIC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function “right first time”.
In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.
EUROPRACTICE is organising about 200 MPW runs per year in various technologies.

MULTI LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi Level Mask (MLM). With this technique the available mask area (20 mm x 20 mm field) is typically divided in four quadrants (4L/R : four layer per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is thus reduced by a factor of four. By adapting the lithographical procedure it is possible to use one mask four times for the different layers by using the appropriate quadrants. Using this technique the mask costs can be reduced by about 60%.
The advantages of using MLM single user runs are : (i) lower mask costs, (ii) can be started any date and not restricted to scheduled MPW runs, (iii) single user and (iv) customer receives minimal a few wafers, so a few hundreds of prototypes.
This technique is preferred over MPW runs when the chip area becomes large and when the customer wants to get a higher number of prototypes or preserie. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.
This technique is only available for technologies from ON Semiconductor, IHP, TSMC, GLOBALFOUNDRIES and XFAB.



TECHNOLOGIES

For 2018, EUROPRACTICE has extended its technology portfolio. Currently, customers can have access to prototype and production fabrication in the following technologies:

- On Semi 0.7µ C07M-D
- On Semi 0.7µ C07M-A
- On Semi 0.35µ C035U
- On Semi 0.7µ C07M-I2T100 100V
- On Semi 0.35µ C035-I3T80U 80V
- On Semi 0.35µ C035-I3T50U 50V
- On Semi 0.35µ C035-I3T50U (E) 50V
- On Semi 0.35µ C035-I3T25U 3.3/25V
- ONC18MS 0.18µm
- ONC18MS-LL 0.18µm
- ONC18HPA 0.18µm
- ONC18-I4T 0.18µm 45/70V
- On Semi 0.5µ CMOS EEPROM C5F
- On Semi 0.5µ CMOS EEPROM C5N

- ams 0.35µ CMOS C35B4C3
- ams 0.35µ CMOS C35OPTO
- ams 0.35µ HV CMOS H35B4D3
- ams 0.35µ SiGe-BiCMOS S35D4M5
- ams 0.30µ A30B4S3 4M/4P Low VT
- ams 0.18µ CMOS aC18
- ams 0.18µ HV CMOS aH18
- BARC Diode for ams C35OPTO
- WLSCP for ams C35B4C3

- IHP SGB25V 0.25µ SiGe:C
- IHP SG25H3 0.25µ SiGe:C
- IHP SG25H4 0.25µ SiGe:C
- IHP SG25H_EPIC (BiCMOS + photonics)
- IHP SG25 PIC (photonics)
- IHP SG13S 0.13µ SiGe:C
- IHP SG13C 0.13µ SiGe:C
- IHP SG13G2 0.13µ SiGe:C
- IHP BEOL SG25
- IHP BEOL SG13

- X-FAB XH018 0.18µ HV NVM E-Flash
- X-FAB XT018 0.18µ HV SOI
- X-FAB XS018 0.18µ OPTO

- TSMC 0.18 CMOS L/MS/RF (G)
- TSMC 0.18 CMOS HV BCD Gen2
- TSMC 0.13 CMOS L/MS/RF (G,LP)
- TSMC 90nm CMOS L/MS/RF (G,LP)
- TSMC 65nm CMOS L/MS/RF (G)
- TSMC 40nm CMOS L/MS/RF (G)
- TSMC 28nm CMOS HPL/HPC
- TSMC 28nm CMOS RF HPC

- UMC L180 Logic GII
- UMC L180 MM/RF
- UMC L180 Logic LL
- UMC L180 EFLASH Logic GII
- UMC CIS18 – CONV diode
- UMC CIS18 – ULTRA diode
- UMC L130 Logic
- UMC L130 MM/RF
- UMC L110AE Logic/MM/RF
- UMC L65N L/MM/RF (SP)
- UMC L65N L/MM/RF (LL)
- UMC 40N Logic/MM – LP
- UMC 28N Logic/MM – HPC

- GF 130nm LP
- GF 130nm BCDlite
- GF 55nm LPe/LPx-NVM/LPx-RF
- GF 40nm LP/LP-RF/RF-mmWave
- GF 28nm SLP/SLP-RF
- GF 22nm FDSOI

- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- MEMSCAP PIEZOMUMPS

- ePIXfab-imec SiPhotonics Passives
- ePIXfab-imec SiPhotonics ISIPP50G
- ePIXfab-LETI SiPhotonics Passives + Heater

- Teledyne Dalsa MIDIS

MINI@SIC PROTOTYPING CONDITIONS FOR UNIVERSITIES AND RESEARCH LABORATORIES

In order to stimulate universities and research institutes to prototype their design also in the advanced technologies (such as 90, 65, 40, 28 and 22nm) at affordable costs, Europractice has introduced the concept of **mini**@sic already since 2003.

That means that Europractice has selected several MPW runs on selected technologies on which universities and research institutes have the opportunity to prototype very small ASIC designs at a highly reduced minimum prototype fee. The minimum charged chip area is highly reduced.

Through the mini@sic concept, the price is reduced considerably. For the most advanced technologies however, the prototyping fee is further reduced through extra funding by the European Commission through the Europractice project (only for European universities and research institutes).

In 2018, Europractice has also added a **MICROBLOCK** in the 28nm technology from TSMC. The Micro-block size is 1110 x 1110 microns (designed area – pre-shrink), which is available for ~10kEUR. Microblock designs can be placed on any of the 28nm-mini@sic runs. However note that in case of only one microblock there is no commitment that the run will be launched.

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TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

EUROPRACTICE training courses for European universities and Research Institutes are primarily aimed at academic staff and PhD students. Unlike training courses which address single topics or individual design tools, the EUROPRACTICE training courses address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow. Since the courses are based on the EUROPRACTICE EDA/CAD tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organisation and make full use of the EUROPRACTICE services/infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants will be able to extensively practice the concepts described in lectures and have access to experts who are able to answer questions about the concepts, design tools or technology process discussed on the course. Where it is known that a design flow is well supported by multiple vendors and/or processes then multiple course variants will be offered that reflect the design tool / processes installed base.

Offered training courses follow a "train-the-trainer" philosophy, so that participants can convey the knowledge acquired to colleagues within their own organisation. Training course participants will be provided with course notes (manuals) which they can then keep and refer to at a late date when applying the techniques to their own work.

During 2017 a total of 262 delegates (27 Lecturers, 118 Postgraduate students, 117 Researchers) attended 31 training courses organized by the Europractice partners at 4 locations (yellow dots). The delegates came from 124 Europractice Member Institutions in 29 countries (red dots) as shown above.

Since Europractice Training courses began in April 2014, a total of 665 delegates from 208 Member Institutes in 35 countries have attended 79 training courses making 2564 days of practical training.

FIRST USER STIMULATION PROGRAM

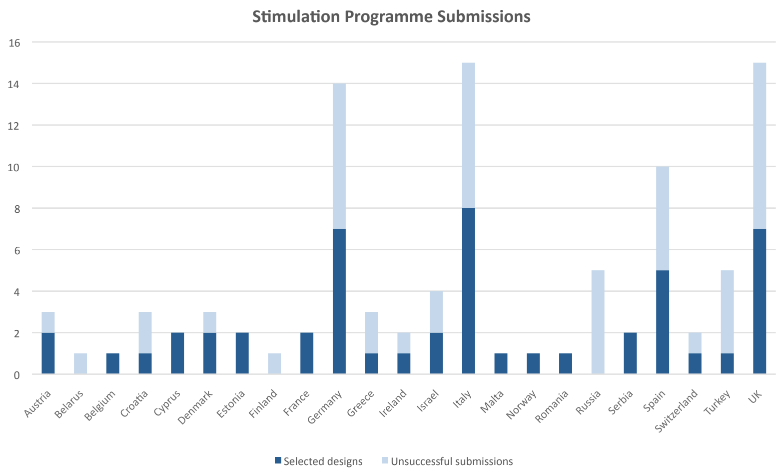
At the end of 2015, a first stimulation action was launched to encourage EUROPRACTICE university members to have an ASIC prototyped for the first time or to move to more advanced technology nodes.

Implementation was proposed as follows:

- To stimulate university members that have not yet prototyped an ASIC. Europractice selected 10 first user application, who were granted free (excluding assembly) prototyping of a minimum block on a mini@sic run in 0.18u CMOS (UMC, TSMC and ams).
- To stimulate university members that have not yet prototyped an ASIC in a technology of 90nm or below. Europractice selected 10 such first users prototyping of a min. area block of a mini@sic run in 65nm/55nm (TSMC, UMC and GLOBALFOUNDRIES) at a price of €5,000 (excluding assembly).

After the success of this first stimulation action in Europractice, two new ASIC, one MEMS and one Silicon-Photonics Stimulation Actions for FIRST USER European EUROPRACTICE university members were defined as a part of the EUROPRACTICE2016 project funded by the European Commission. Once again, the 10 best designs in the two categories were selected by an Independent expert Committees. These designs are expected to be realized in silicon by the end of 2018.

Overall a total of 98 applications were submitted to 6 First User Stimulation Programmes by 73 universities from 23 countries. These design proposals were and judged by 5 independent expert committees and 50 designs were selected for fabrication.



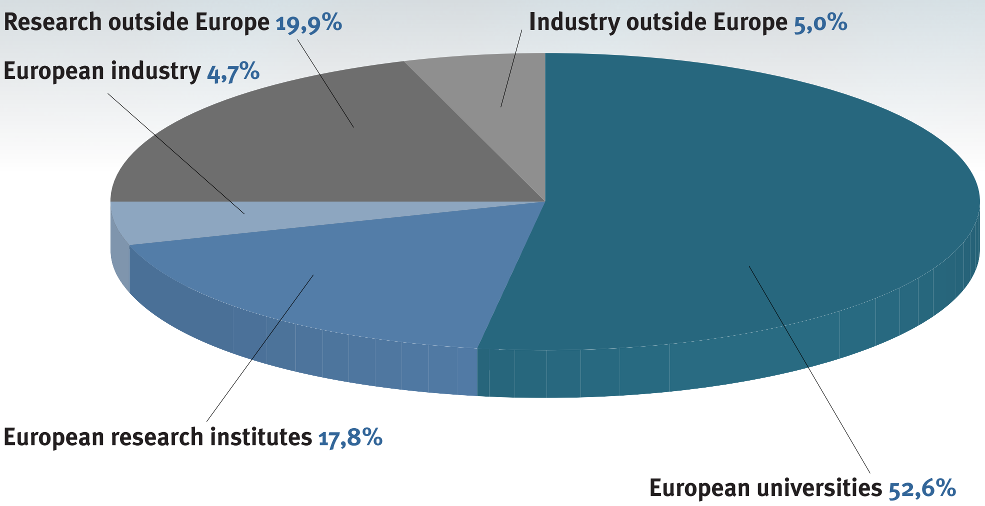
EUROPRACTICE WEBSITES

The current Europractice service is holding 2 web pages in order to promote the service and to keep all (potential) users updated on new available tools and technologies.

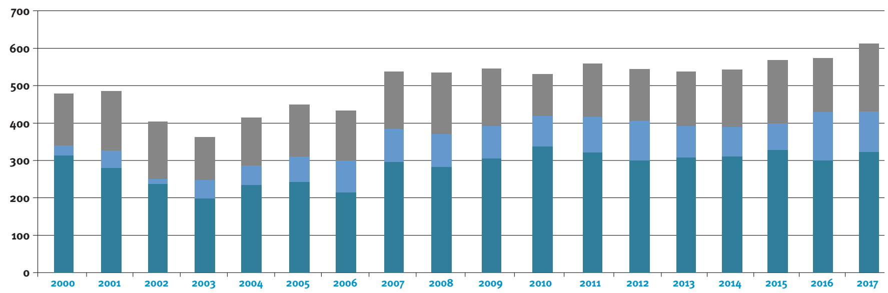
- The EDA / CAD tool web site (**www.europractice.stfc.ac.uk**) is hosted and maintained by STFC. This page is updated at least twice per week by STFC and contains all the latest information about the design tools, training courses and events
- The IC technology / fabrication web site (**www.europractice-ic.com**) is hosted and maintained by IMEC and is regularly updated with the latest news on MPW offering, schedule and pricings.

RESULTS

MPW PROTOTYPING SERVICE



MPW designs in 2017



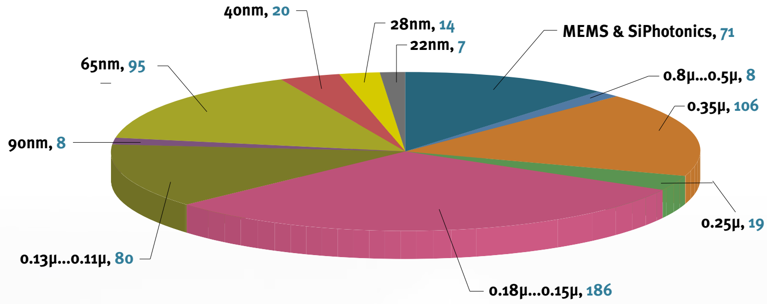
	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
Industry + non-European univ/research	140	159	155	115	128	138	134	154	164	153	113	143	139	144	153	169	145	182
Europractice Research	27	46	13	48	52	69	84	87	85	87	83	96	105	87	80	72	128	109
Europractice Academic	313	281	237	200	234	243	215	298	285	305	337	321	301	307	311	328	301	323

ASICS PROTOTYPED ON MPW RUNS

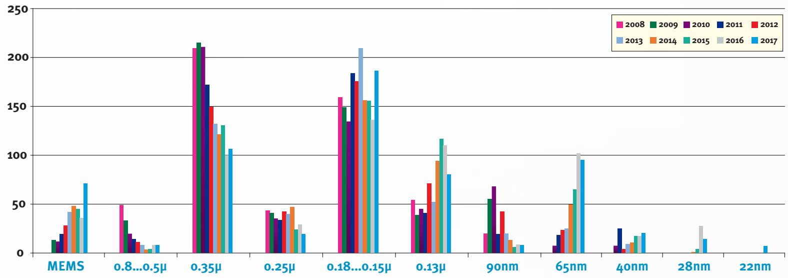
In 2017, a total of 614 designs have been prototyped, a significant increase compared to 2016, when already a record-high number of 575 designs were noted.
70% of the designs are sent in by European universities and research institutes while the remaining 30% of the designs is accorded for by non-European universities (20%) and commercial companies world-wide (10%).

A GOOD TECHNOLOGY AND GEOMETRY MIX

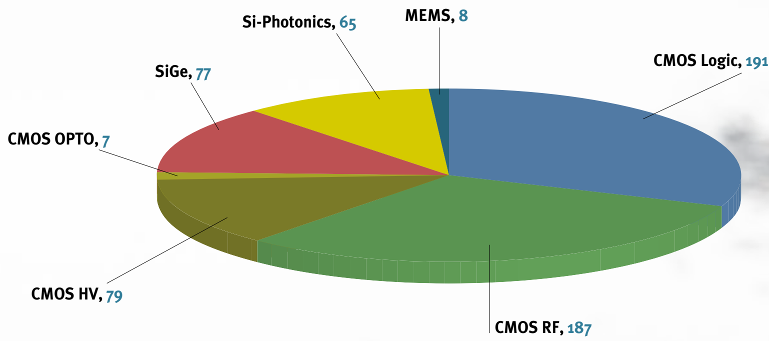
Year over year a shift towards more advanced technologies can be observed, however in 2017 this trend seems to have stabilized as is shown in the bar graphs. For the advanced technology nodes, the number of designs in 28nm has decreased considerably, while in 65 and 40nm the number of design remains more or less constant. On the good side, it has to be noted that in 2017 Europractice fabricated 7 designs in the 22nm FDSOI technology from GLOBALFOUNDRIES. The 0.18μ / 0.15μ and 0.13μ / 0.11μ technologies still represent almost half of the total designs and even the older nodes such as 035μ still remain very popular with more than 100 design. In addition, the number of designs in Silicon Photonics and MEMS has increased considerably compared to 2016, which is thanks to the high number of designs in the imec Si-photonics technologies (namely 59 designs in total).
Finally, a very good mix of different technologies is being offered through the Europractice prototyping service. The most popular technologies are CMOS logic and RF CMOS, for which the number of fabricated designs represents a bit more than 60%. HV-CMOS and SiGe represent together 25%, while for the More-than-Moore technologies Si-photonics is clearly the most popular one. During the coming years, a special effort will be made to promote and boost the MEMS fabrication services.



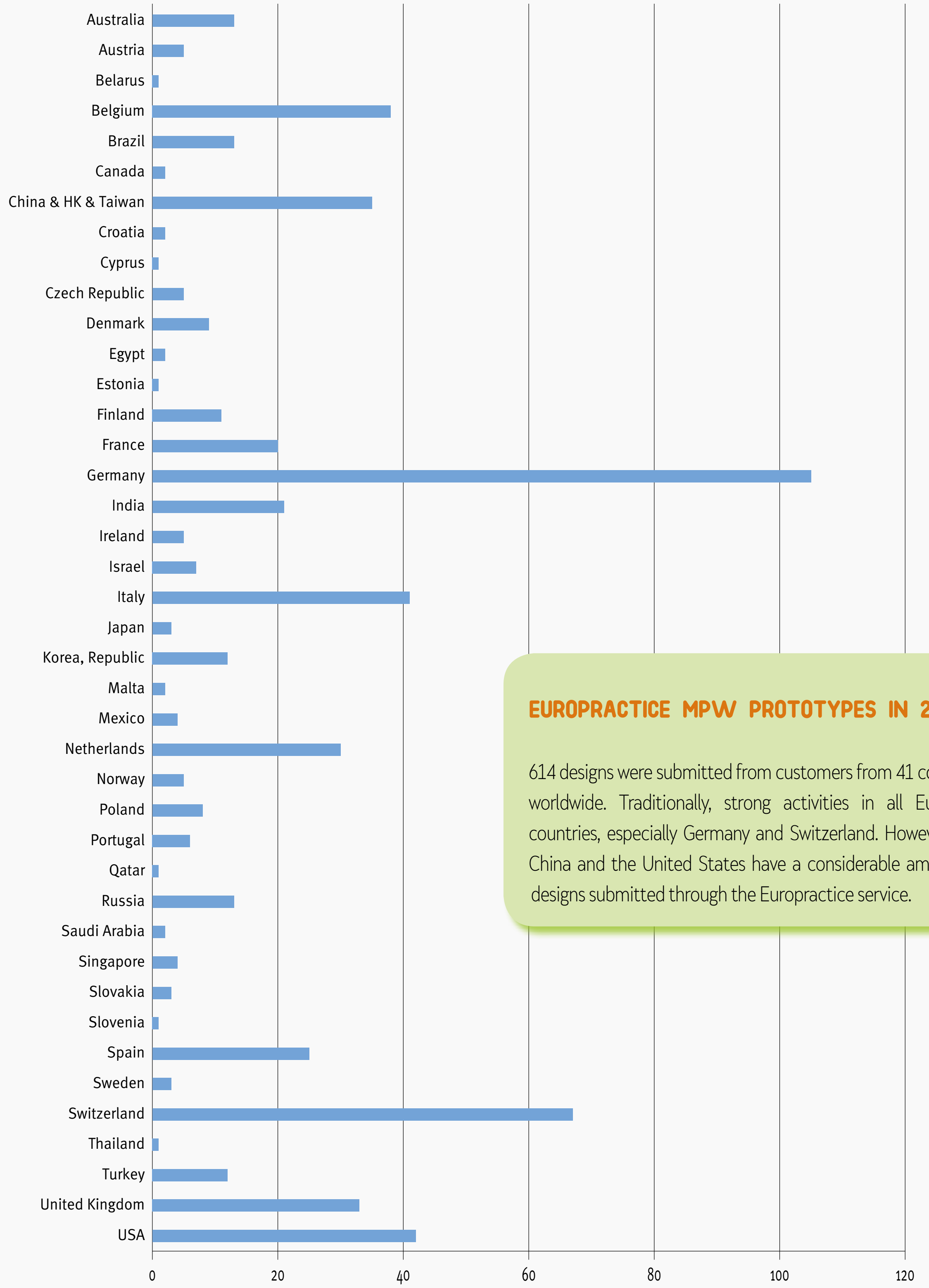
MPW designs in 2017: technology node and number of designs



Geometry mix

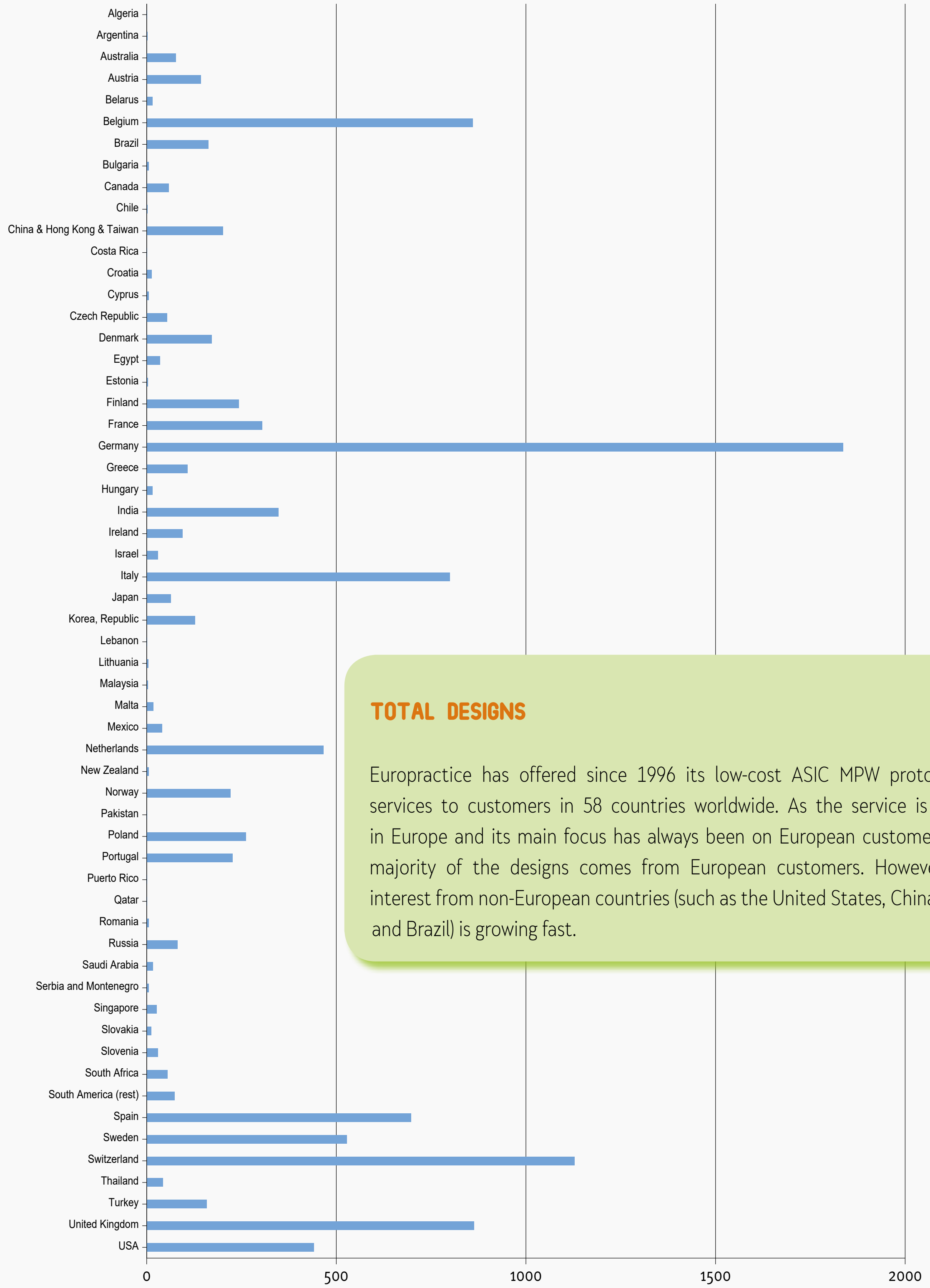


number of *designs per technology in 2017*



EUROPRACTICE MPW PROTOTYPES IN 2017

614 designs were submitted from customers from 41 countries worldwide. Traditionally, strong activities in all European countries, especially Germany and Switzerland. However, also China and the United States have a considerable amount of designs submitted through the Europractice service.



TOTAL DESIGNS

Europractice has offered since 1996 its low-cost ASIC MPW prototyping services to customers in 58 countries worldwide. As the service is based in Europe and its main focus has always been on European customers, the majority of the designs comes from European customers. However, the interest from non-European countries (such as the United States, China, India and Brazil) is growing fast.

ARTROC - a multichannel ASIC for readout of position-sensitive detector of X-rays based on Gas Electron Multiplier (GEM) technology

AGH University of Science and Technology, Faculty of Physics and Applied Computer Science, Kraków, Poland

Contact: Władysław Dabrowski, Tomasz Fiutowski, Krzysztof Świentek, Piotr Wiacek
E-mail: W.Dabrowski@ftj.agh.edu.pl

Technology: ams CMOS C35B4C3 4M
Die size: 6750 µm x 7930 µm

Application

The ARTROC ASIC [1] is dedicated for readout of position sensitive and energy dispersive X-ray detectors based on the GEM (Gas Electron Multiplier) technology. The driving application of such a detection system is nondestructive investigation of cultural heritage objects using X-ray fluorescence (XRF) technique, which allows mapping of hidden pigment layers by recording element-specific Xray fluorescence radiation. There are two possible implementations of this technique: macro-XRF and full-field, illustrated schematically in Fig. 1. The macro-XRF technique utilizes a focused X-ray microbeam for exiting the fluorescence radiation, a mechanical scanning system, and a high energy resolution X-ray detector, typically a silicon-drift detector. Thus, the spatial resolution in this method is determined primarily by the spot size of the exciting beam. Such a system can be built of commercially available components. The full-field imaging technique requires a position sensitive and energy dispersive X-ray detector. An investigated object is illuminated by a broad X-ray beam and excited fluorescence X-ray is projected onto a 2-D position sensitive detector through a pin-hole camera. In the developed system the active area of the GEM detector is 10 cm × 10 cm, which is read out by two sets of orthogonal strips with a pitch of 0.8 mm. The main advantage of such a system is shortening of the measurement time, but it requires developing a custom readout electronics. A key component of the readout system is the ARTROC ASIC, which is capable of reconstructing 2-D positions of detected photons with pixel pitch 0.8 mm, clustering the signals from adjacent pixels, and measuring energy spectra for individual pixels.

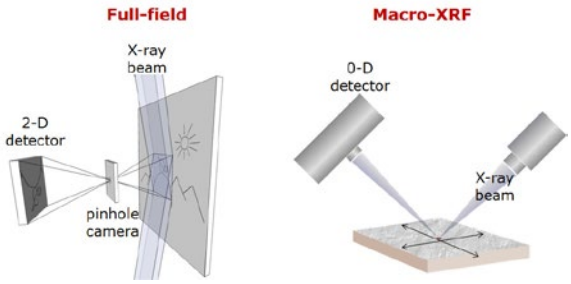


Fig. 1: Schematic views of the full-field and macro-XRF imaging systems.

ARTROC architecture and functionality

A simplified block diagram of the ARTROC ASIC is shown in Fig. 2. The ASIC comprises 64 independent channels providing high performance analog processing of signals from the GEM detector. The circuits are optimized to maximize signal-to-noise ratio for the amplitude measurements and minimize time jitter and time walk for the time measurements. Since the signals from the detector occur randomly the circuit has to provide also self-triggering function, which initiates the Peak Detect & Hold (PDH) circuit and the readout sequence. For each signal its amplitude and time is extracted and stored in the analog and digital FIFO respectively. The FIFOs work as derandomising buffers. The readout of both buffers is performed via a token-ring based multiplexer providing data sparsification and full zero suppression. The analog data are read out via a single differential link at a rate of 31.25 MHz, while the digital data are read out via a parallel 8-bit LVDS bus at a rate of 125 MHz. Matching of signals from X- and Y-strips is performed in an external FPGA-based readout system according to their time stamps.

The layout of the ARTROC ASIC is arrange such that the inputs can be connected directly to the detector readout strips in order to minimize the stray capacitances at the preamplifier inputs, which affect directly signal to noise ratio. A photograph of the bare die mounted and bonded to the PCB is shown in Fig. 3. Each coordinate of the detector is read out by 128 strips so for readout of the complete detector we need four 64-channel ARTROC ASICs.

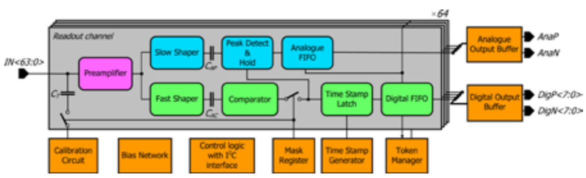


Fig. 2: Functional block diagram of the ARTROC ASIC

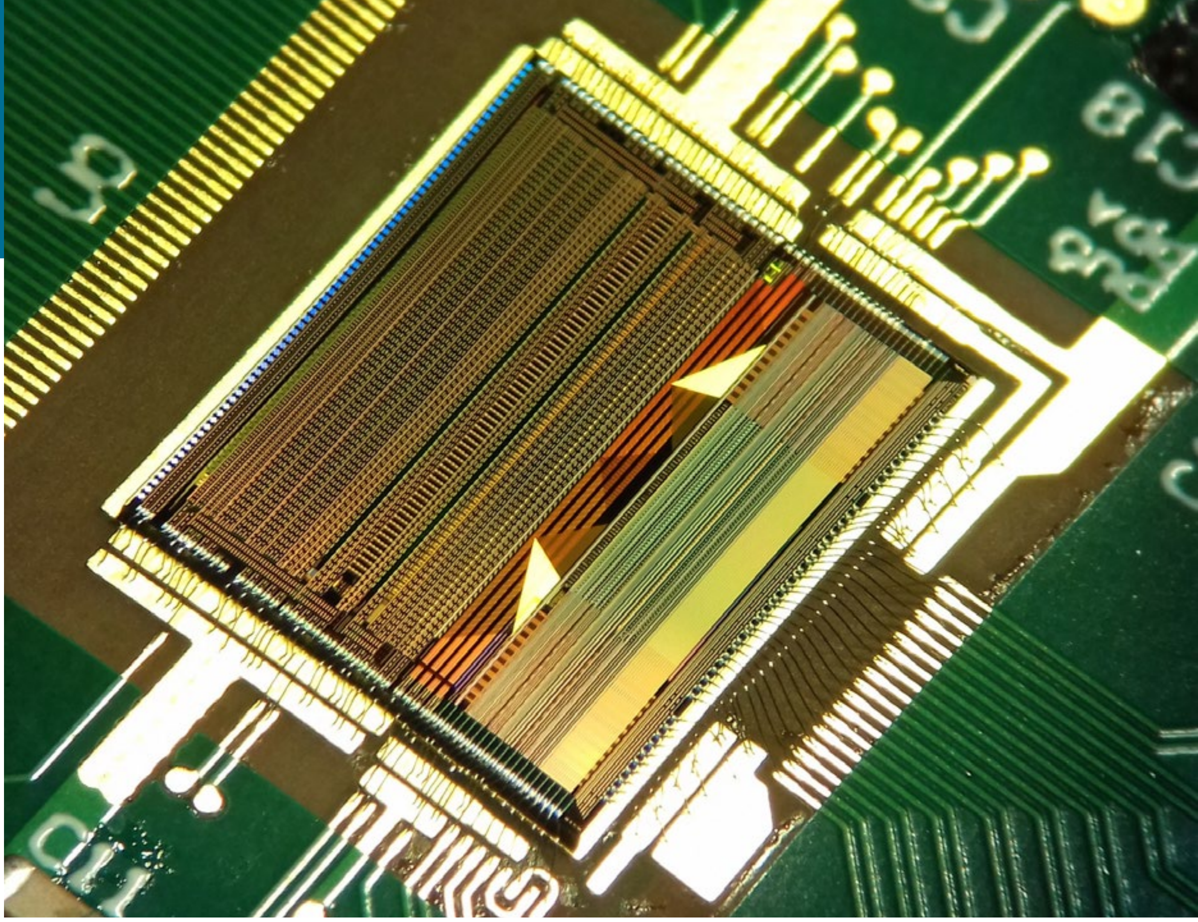
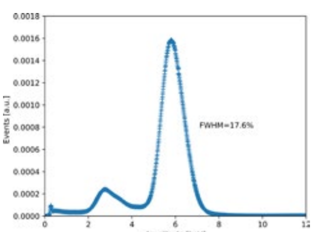


Fig.3: The ARTROC ASIC mounted on PCB in the GEM detector readout system.

System Performance

A critical parameter of the detection system is the energy resolution as this determines the capability of identifying specific pigments. Figure 4 shows a spectrum of X-ray from Fe-55 radioactive source measured with the demonstrator system. The spectrum is the sum of individual spectra of all 128 × 128 pixels so smearing of the peak is affected not only by fluctuations of the primary charge generated in the GEM detector and noise of the front-end circuits, but also by matching of parameters (gains and offsets) across the channels in the ARTROC ASICs. The energy resolution measured, according to the commonly used standard, as the ratio of the Full Width at Half Maximum (FWHM) to the amplitude for the 5.9 keV line is 17,6%. To our best knowledge this is the best ever reported result for a GEM detector.



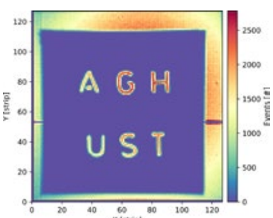


Fig. 4. Cumulative spectrum of X-ray from Fe-55 radioactive source measured with a GEM detector equipped with ARTORC ASICs.
Fig. 5. 2-D image taken with a detector equipped with the ARTROC ASICs.

An example of simple 2-D image obtained with X-rays from Fe-55 source in the transmission mode is shown in Fig, 5. A brass plate with milled letters "AGH UST" was used as a target. The width of the cutout pattern was of about 2 mm. The X-rays source was placed at a distance of about 10 cm above the detector window without a collimator. In such a geometry the image quality is affected by scattering of X-rays and by the parallax effect. Therefore, the edges of the cutouts are not particularly sharp, but the image illustrates proper functionality of the overall detection system, including the ARTROC ASICs.

Why Europractice?

We rely on Europractice services over past two decades to develop ASICs with very unique architectures and parameters for applications in various scientific projects on radiation detection and neurobiology. Both aspects, access to the state-of-the art technology and relatively low cost, are important for making real progress in scientific research projects with limited budgets. Excellent technical support by the team from Fraunhofer ISS is invaluable and it is highly appreciated.

Acknowledgement

We acknowledge financial support of this project by the Polish National Centre for Research and Development, grant no. PBS3/A9/29/2015.

References

[1] T. Fiutowski, S. Koperny, B. Łach, K. Świentek, P. Wiacek and W. Dabrowski, "ARTROC – a readout ASIC for GEM-based full-field XRF Imaging", 2017, Journal of Instrumentation 12, C12016.

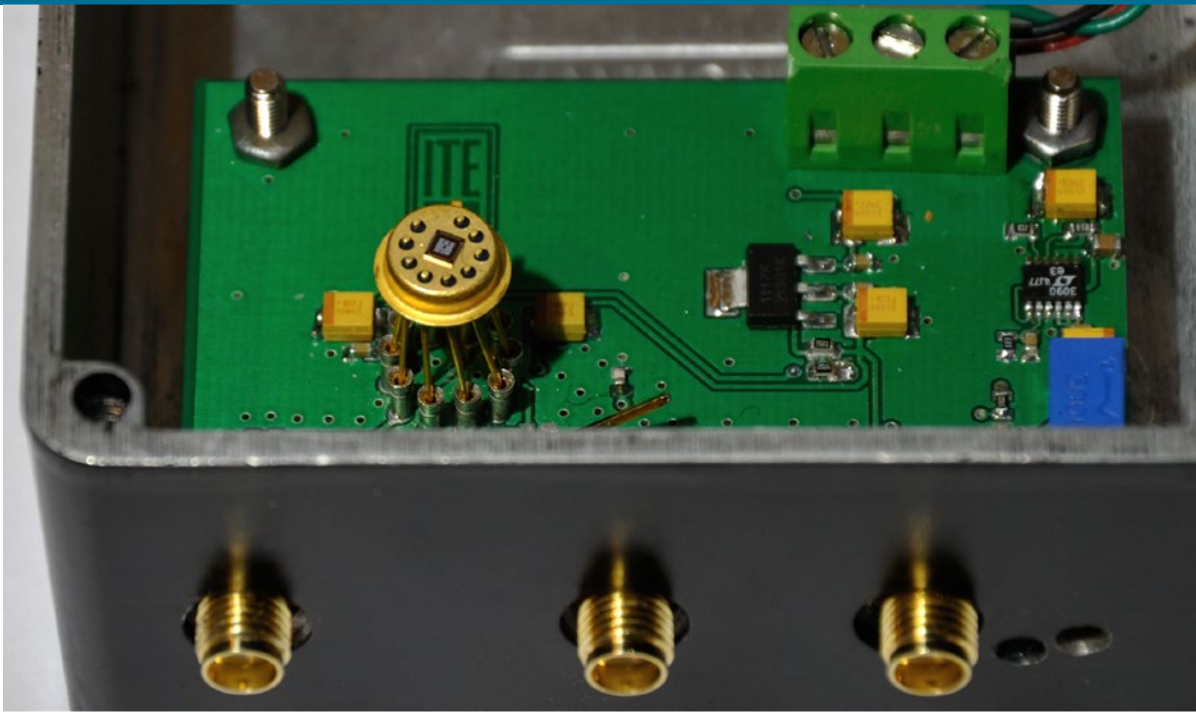


Fig. 1: Fabricated structure assembled in TO-39-10 package and placed in dedicated test setup

Readout Structure for FET-based THz Detectors

Institute of Electron Technology, Department of Integrated Circuits and Systems Design, Warsaw, Poland

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E-mail: ckolacin@ite.waw.pl
Technology: ams CMOS aC18
Die size: 2000 x 2000 µm

Introduction

Properly polarized Field Effect Transistor (FET) with dedicated on-chip antenna can act as a detector for THz radiation. Nowadays, this type of devices is considered to be one of the most promising solutions in dealing with the THz imaging, spectroscopy and communication. FET detectors provide low fabrication costs, satisfactory noise parameters, at room temperature, and easy on-chip integration with read-out electronics.

Description

Proposed readout structure is aimed at THz communication – it must provide large bandwidth and upper frequency limit of several hundreds of MHz. In our target application, the THz source is modulated with a pure digital signal representing data to be transmitted. Illuminated by the THz wave, FET-based detector demodulates the carrier wave and restores the input data signal (direct detection mechanism). In general, output signal from these detectors is a small voltage generated over the relatively high output impedance. Therefore proper signal processing requires high gain and high input impedance of the readout circuit.

Designed chip contains nine test circuits targeting readout for FET-based detectors. Each of these sub-circuits is fully independent and equipped with own I/O and power pads. They are all based on the relative simple architectures - such as cascode and folded-cascode - and equipped with input RC elements to provide desired bandwidth and input impedance. During measurements each of them will be first tested individually and next -with THz detector connected to its input. By analysis of achieved results, the best circuit solution for THz communication link will be determined.

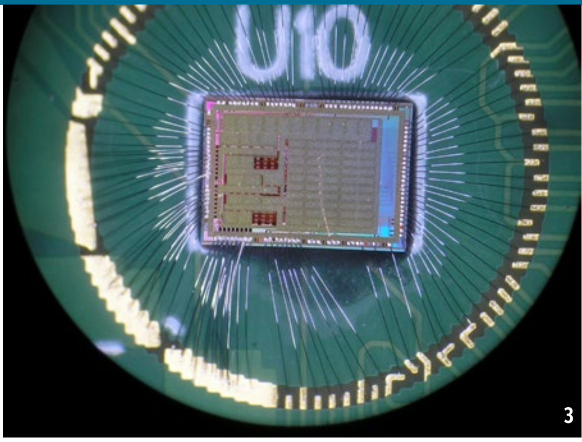
Additionally, in the center of the IC the sixteen FET transistors have been placed, dedicated to measurements with high frequency probes. Detailed measurements of these devices should determine the general performance of the ams aC18 process as a technology for THz detectors development.

Why Europractice?

Institute of Electron Technology is a longstanding member of Europractice, with many ICs designed and fabricated during the last several years. The Europractice MPW service offers an excellent opportunity for the prospective access to many mature technologies. Europractice staff always provides superb assistance and knowledgeable feedback, which is a huge support for our design and prototyping processes.

Acknowledgement

This work has been partially supported by the Polish National Centre of Research and Development (NCBR) under project LIDER/020/319/L-5/13/NCBR/2014.



An integrated LED driver using a Hybrid Switched Capacitor Converter with reduced inductor size

Eindhoven University of Technology, Mixed-signal Microelectronics Group, The Netherlands

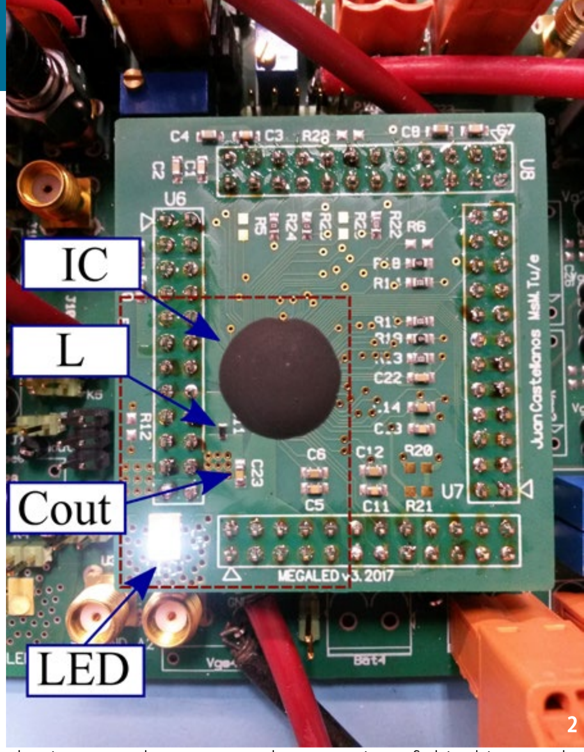
Contact: Juan Castellanos, Pieter Harpe, Eugenio Cantatore
E-mail: j.castellanos@tue.nl; p.j.a.harpe@tue.nl; e.cantatore@tue.nl
Technology: ams 0.18µ HV CMOS H18 6M
Die size: 4166 x 2930 um

Description

Solid-State LED lighting has emerged as a solution for high efficiency, long lifetime, compact form factors, color mixing and smart lighting applications (such as internet of things - IoT). Nevertheless, the operation of LEDs demands LED drivers, which use bulky inductors and several external components. Therefore, power efficiency, total size, form factor and functionalities are compromised. Silicon integration of LED drivers enables compact form factors and smart functionalities at low cost. However, it is a challenge to preserve high power efficiency and current dimming capabilities when the driver is scaled to IC dimensions and the inductor value is reduced.

Results

Inspired by this problem, the Mixed-signal Microelectronics Group at the TU/e developed within the NWO-TTW project MEGALED, supported by Philips, a highly efficient and compact LED driver using a Hybrid Switched-Capacitor Converter. This converter merges Switched-Capacitor (SC) and inductive converters in one topology. It operates at the resonance frequency between the capacitor in the SC converter and the inductor. Also, additional operation states are added to dim continuously the LED load in a full range. Using this converter, it was possible to reduce the energy losses of the SC converter, and to enable efficient continuous current dimming using small inductor sizes. Additional circuitry, such as current sensors, zero-current detectors, a self-resonant timer and a control loop were



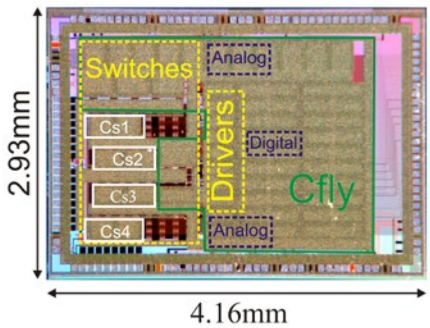
also integrated to support the operation of this driver at the best efficiency point. The switching frequency is automatically adjusted by the self-resonant timer to match the resonance frequency, thus tracking manufacturing variations in the LED, inductor tolerances or parasitics.

The LED driver uses a single 6.4mm^2 footprint SMD inductor of 150nH without using external flying capacitors. It can supply current to a 0.7A LED load with a peak-efficiency of 92.2%. The chip was recently published at ESSCIRC 2017.

Fig. 1:
Detailed image of the fabricated self-resonant H-SSC LED driver chip

Fig. 2:
PCB of the self- resonant H-SCC LED driver chip

Fig. 3:
Bonded die of the self-resonant H-SSC LED driver chip on the PCB



Why Europractice?

Europractice offers a wide range of design tools and a wide range of IC technologies, both at a very affordable price. As a university, this enables us to develop and fabricate test chips, which would otherwise not be possible. On top of that, Europractice offers excellent technical support and flexibility, which is a MUST for successful tape-outs. Thank you very much!

Reference

[1] J.C. Castellanos, M. Turhan, M.A.M. Hendrix, A. van Roermund, E. Cantatore, "A 92.2% peak-efficiency self-resonant hybrid switched-capacitor LED driver in 0.18µm CMOS" in ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference, pp. 344-347.

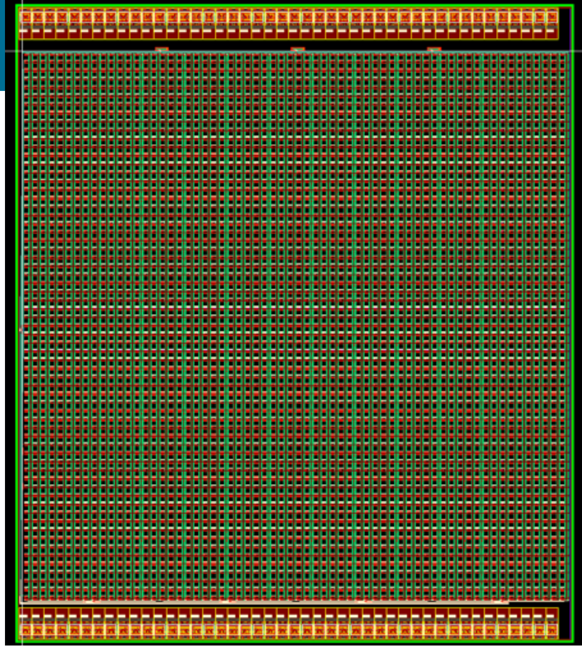


Fig. 1: Layout of the 64x64 array of SPADs

64x64 planar array of CMOS Single Photon Avalanche Diode for fluorescence imaging

University of Glasgow, Microsystem Technology Group, United Kingdom
In collaboration with University of Edinburgh, United Kingdom

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E-mail: c.accarino.1@research.gla.ac.uk; Mohammed.Al-Rawhani@glasgow.ac.uk; Srinjoy.Mitra@ed.ac.uk; David.Cumming.2@glasgow.ac.uk
Technology: AMS 0.18 µm HV CMOS aH18 50V/20V/5V/1.8V/ 6M/MIM
Die size: 4.6 mm x 4.05 mm

Description

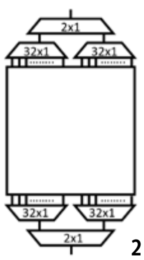
Single Photon Avalanche Diodes (SPADs) are becoming increasingly important for use in biomedical imaging thanks to their high sensitivity and fast response; Fluorescence, lifetime fluorescence, Raman spectroscopy and PET detector are typical SPADs application. The designed chip is suited to fluorescence imaging in a reduced illumination condition. Previous work enabled us to demonstrate a high performance pixel on a standard high voltage CMOS process. The design was engineered to optimize the photon detection probability (PDP) ratio between the number of detected photons and the total number of photons illuminating the active area of the detector, whilst minimizing the base noise level known as Dark Count Rate (DCR). The design of the SPAD relied on semiconductor simulations, using Sentaurus TCAD, to optimize the electric field and achieve the desired specifications. Figure 1 shows a layout of the chip, designed in 0.18 µm High Voltage CMOS technology, which is an array of 64x64 pixels consisting of a SPAD detector and the readout electronics with an 8-bit ripple counter and a global shutter to optimize image acquisition. Addressing is achieved using 4 decoders of 5-bit each; 2 horizontal ones (left and right) and 2 vertical ones (top and bottom). The count data are streamed out through a system of multiplexers placed at the top and bottom of the array respectively. The upper 32 rows, and the lower 32 rows as the system is symmetric, are streamed out through 2 multiplexers in cascade with a third one as shown in Figure 2: the first two blocks, which can be sequentially activated, select one 8-bit output from the available 32 columns (either left or right) and the cascaded multiplexer enables one side of the array at the time. In-pixel electronics is designed to minimize both the propagation delay and the pixel pitch while ensuring a sufficient storage memory for SPAD events. Figure 3 and 4 show a part of the array and a detail of few pixels respectively.

Results

The developed test SPAD showed a breakdown voltage of 16.8 V with a median DCR lower than 1 kHz/µm2 with a PDP greater than 50%. Early testing of the 64x64 array of SPADs matched the breakdown voltage of the test SPAD with comparable DCR, using a shutter time window of 1 ms.

Why Europractice?

We have successfully used Europractice service before and their support and availability were very accurate and helpful every time. Furthermore, they provide access to state of the art foundry service and foundry support at a discounted price which is extremely helpful especially for university research. We also benefitted from Europractice courses, Introduction to Technology CAD (TCAD), Introduction to Analogue and Mixed Signal IC Design and Introduction to Quartus Prime FPGA course are some of the course we attended, which we found thoroughly well organized, rich of useful contents and very helpful to achieve our objectives.



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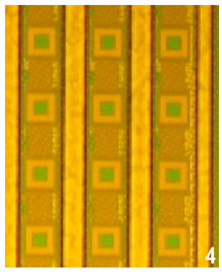
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Fig. 2: Schematic of the multiplexer system for readout
Fig. 3: Micrograph of part of the 64x64 array
Fig. 4: Detailed micrograph of the 64x64 array, illustrating the SPADs in green

Analog and Digital IP Blocks for Platforms of Sensors

Group of Metamaterials, Microwaves and Optics (GMeta), Dept of Electrical Engineering (SEL), University of São Paulo (USP), São Carlos - SP, Brazil

Contact: Prof. João Paulo Carmo, Rodrigo Henrique Gounella, and João Paulo Costa
E-mail: jcarmo@sc.usp.br
Technology: ON Semi 0.7μ C07M-A 2M/1P/PdiffC/HR
Die size: 2760μm x 2760μm

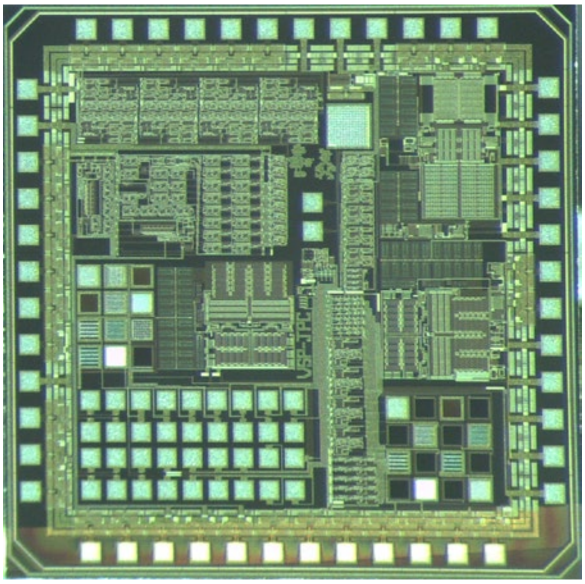

Fig.1: Photo of the fabricated microdevice.

Description/application of the microdevice

This microdevice comprises several analog and digital blocks. More specifically, it is composed by two biopotencial amplifiers with output drivers, one additional biopotencial amplifier without driver and reference voltages, 16 N+/p-sub photodiodes with diffraction structures on top and respective readout electronics, one optical transceiver for intra-corporal communications, one arbitrary/programmable PN sequence generator, one digital controllable PWM generator, one power driver, few test structures of photodetectors, one plasmonic photodiode, one radiofrequency modulator, and one test structures of a novel active-pixel. The biopotential amplifiers were designed for integration and implementation of the chip-in-the-tip electrode concept for use on optogenetics applications. The amplifier was designed to operate between 1Hz and 10kHz, to reject DC offsets generated at the interface between the electrodes and the tissue, with a medium-frequencies gain of 40dB (e.g., a gain of 100) and a power consumption of 36μW at 5V. Few photodiodes in the 4x4 array was fabricated with slits and metallic strips above to provide functionalization and frequency-selectivity for chemical and gas sensors based on optics. The optical transceiver was designed for intra-corporal wireless transmission at high data-rates. The arbitrary PN sequence generator was designed for application on platforms of sensors. The programmable PWM generator and the power driver were designed for integration of photodynamic therapy modules on intra-corporal devices. The plasmonic photodiode uses metallic straps and slits to use surface plasmons for chemical and gas sensors. The radiofrequency modulator was designed with the purpose to modify and/or modulate signals to provide excitation on sensors based on electrets and piezoelectrets. Finally, the unitary cell of a new type of active-pixel was designed with the intention to characterize the behavior of a new architecture of imagers in this technology.

Why Europractice?

The Europractice service offers affordable prototyping for research. However, in my point of view, it has the simpler procedures to access the technology and a easy to understand website, when compared to similar services outside Europe. It is very easy and straightforward to access without complications the NDAs and PDKs. The submission page is also very easy to work. The Europractice service is always open to questions and suggestions related to delivery and billing.

Acknowledgement

The fabrication of this microdevice was fully sponsored by the Brazilian National Council of Scientific Research (CNPq) under the grant 400110/2014-8.

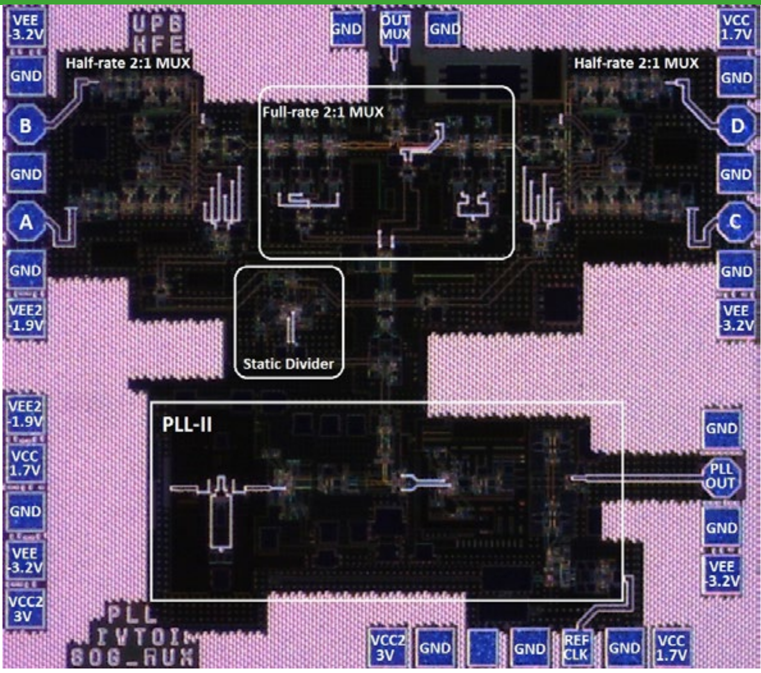

Fig. 1: Picture of the fabricated die in IHP SG13G2 BiCMOS HBT technology

4:1 Multiplexer Working up to 155 Gbps with On-chip PLL

Dept. High-Frequency Electronics, University Paderborn, 33095 Paderborn, Germany

Contact: Umair Ali, Andreas Thiede
E-mail: thiede@uni-paderborn.de
Technology: IHP 130 nm SiGe BiCMOS technology (SG13G2)
Die Size: 2.3 mm^2

Description/application of the microdevice

A 155 Gbps 4:1 multiplexer has been designed and fabricated in the IHP SG13G2 BiCMOS HBT technolgy. 4:1 multiplexing was achieved in two steps using three 2:1 MUXs. Each of the first stage 2:1 MUXs converts two 40 Gbps data streams into a single 80 Gbps data stream. The second stage 2:1 MUX takes 80 Gbps outputs of both half-rate multiplexers and converts them to a single 160 Gbps data stream. The select lines for both half- and full-rate MUXs are provided either by an on-chip clock source i.e. PLL or by an external clock source. Each of the half- and full- rate MUXs are based on the master-slave-slave and master-slave architectures.

The clock distribution network receives the clock signal either from the output of the on-chip PLL or from the external pad and brings it to the individual latches of each 2:1 MUX. The design of the clock distribution networks is targeted to keep the gain of each branch of the clock distribution network close to unity. Additionally, a tight phase synchronization is kept among the signals delivered by each branch at the inputs of latches and 2:1 selectors. The purpose of an active balun is to convert the single-ended clock to a differential clock signal with some gain. If a differential clock signal is readily available from the PLL then this block can be omitted. An input buffer isolates the balun from the core of the clock distribution network. The clock distribution network for the 4:1 MUX is simply an extended version of the network used for the 2:1 MUX.

The full characterization of the multiplexer samples became increasingly complicated and challenging at data rates beyond 100 Gbps. Several factors, such as limited operating bandwidth of the sampling oscilloscopes and limited data rates of the bit pattern generators, restrict the full characterization of the MUX. Consequently, we were forced to measure the ICs under certain limitations. For this purpose, we fabricated two versions of 4x1 MUX. In version 1, an external 0-80 GHz clock source is connected to the clock input of the MUX, whereas, in version 2 the clock signal is provided by an on-chip PLL. The characterization of version 1 was completed in two phases i.e. static input characterization and PRBS characterization. For static input characterization, we applied fixed DC voltage levels corresponding to 1s/0s at four data inputs A, B, C, and D. The 0-80 GHz clock signal at frequency fin was applied at the input clock using a signal generator. The output of the 4:1 MUX , i.e. the sequence ACBD, was measured using a state-of-the-art spectrum analyzer. The verification of the circuit was done for the following three cases of static inputs: For inputs A=B=1 and C=D=0, we expect a spectral line at fin. For inputs A=B=C=D, we expect no spectral lines at all. And for inputs A=C=1 and B=D=0, we expect a spectral line at fin/2. As spectrum analyzer with 80 GHz bandwidth, that was required for the proposed characterization scheme, we could use the newly developed spectrum analyzer MS2760 by Anritsu, measuring from 9 kHz up to 110 GHz with a single frequency sweep.
For PRBS characterization of the 4:1 MUX, we applied PRBS data at inputs A, B, C, and D. The clock signal was provided directly by the signal generator and the output was measured using 70 GHz digital sampling oscilloscope. The PRBS characterization of the 4:1 MUX was possible up to 80 Gbps output data rate due to equipment limitations. Once the operation of the MUX with external

clock was verified, a PLL, which was already verified to be working from 153.5 to 155 GHz, was added to the 4:1 MUX block. A 40 GHz clock source 'REF CLK' was used as a reference signal for the PLL. The PRBS input was not possible in this case due to limited bandwidth of the sampling oscilloscope. So, only static inputs were applied for all three cases. The expected outputs corresponding to three above cases for 4:1 MUX with on-chip PLL could be shown for a data rate of 153.5 Gbps.

Acknowledgement:

German Research Foundation (DFG) is sincerely acknowledged for funding the project through TH829/9. We are very thankful to Anritsu Deutschland GmbH for supporting the measurements by advanced access to the MS2760 Spectrum Analyzer. Finally we wish to thank IHP Frankfurt Oder for chip fabrication and the EuroPractice initiative for providing access to this technology and the respective design tools.

Why Europractice?

The department High-frequency Electronics of University Paderborn has been using EuroChip and EuroPractice initiatives since its foundation in 1999. We have worked with OMMICs GaAs HEMT, CT Microelectronics CMOS and IHPs HBT technologies in numerous research projects. We appreciate the EuroPractice services for providing access to leading edge IC technologies and CAD tools at reasonable prices. It is thus wonderfully suitable for academic institutions!

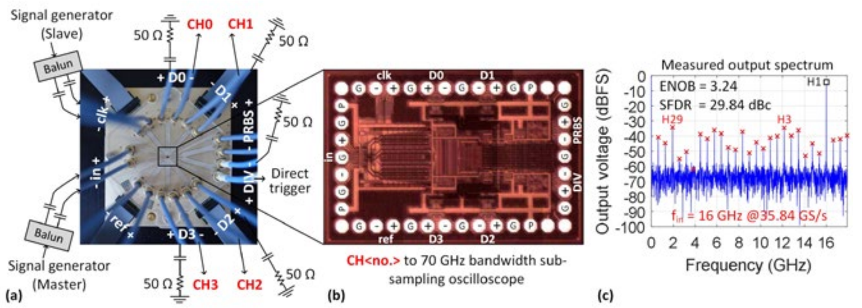

Fig. 1: (a) Validation test setup, (b) ADC die photograph and (c) measured output spectrum of digitized sine input.

A 35.84 GS/s 16 GHz ERBW 4 bit Single-Core Flash ADC

Institute of Electrical and Optical Communications Engineering (INT), University of Stuttgart, Germany

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Technology: IHP 130 nm SiGe BiCMOS technology (SG13G2)
Die size: 1.4 mm x 0.9 mm

Description

Via EUROPRACTICE, we did a tapeout of a mm-wave analog-to-digital converter (ADC) [1] in a 130 nm SiGe BiCMOS technology from IHP. The ADC is based on a 4 bit flash architecture and makes use of a traveling-wave signal distribution approach, where analog input and clock signal travel synchronously along two delay-matched transmission lines from comparator to comparator. Fig. 1 depicts the validation test setup (a), the die photograph (b) and the measured output spectrum (c) of the ADC. The converter is wire-bonded on a specially designed RF printed circuit board and is characterized with a four-channel 70 GHz sub-sampling oscilloscope. At a sampling rate of 35.84 GS/s, the ADC exhibits an effective bit resolution bandwidth (ERBW) of 16 GHz with an effective number of bits (ENOB) of 3.24 and spurious free dynamic range (SFDR) of 29.84 dBc. To our best knowledge, this is the first reported single-core ADC that enables full Nyquist sampling operation beyond 30 GS/s. The ADC can be utilized in 100 Gbit/s wireless communication infrastructures such as proposed in [2] to enable digital signal processing (DSP) of wideband baseband receive signals with low modulation order as well as in optical communication systems to enable DSP-based equalization of fiber-induced dispersion [3].

Why Europractice?

As a research institute specialized in the design of integrated electrical and optical circuits (e.g., ADC, DAC, photonic ICs, etc.), fast access to leading electronic automation tools and state-of-the-art semiconductor technologies is of utmost importance for us. At present, and over the past two decades, we rely on EUROPRACTICE for software licensing, design kit access and particularly IC fabrication in some of the most advanced semiconductor technologies. We deeply value the benefits of being part of the EUROPRACTICE program and are very thankful for the technical support provided by the EUROPRACTICE teams at STFC, IMEC and especially at Fraunhofer IIS.

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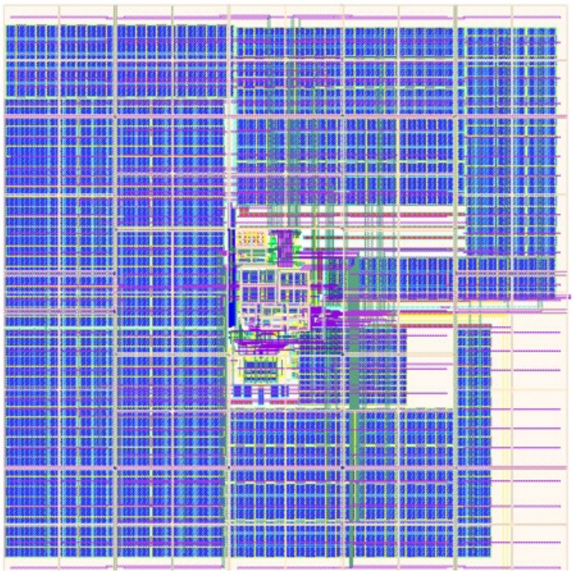

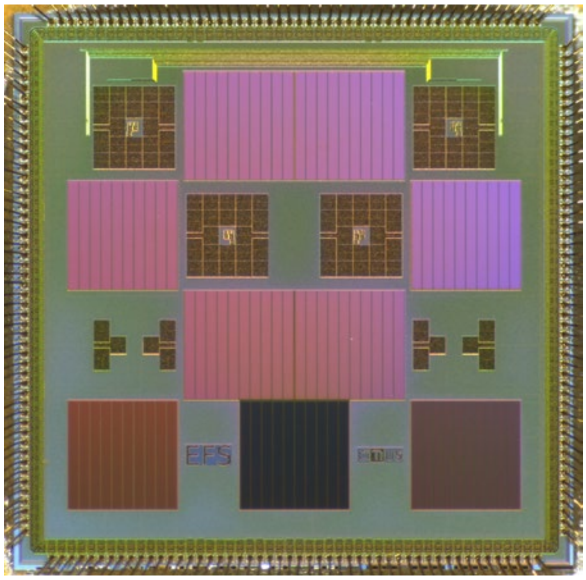

Micro-Energy Harvesting System including a PMU and a Solar Cell on the Same Substrate

Centro Singular de Investigación en Tecnoloxias da Información (CiTIUS), Universidade de Santiago de Compostela, Santiago de Compostela, Spain

Contact: Designer: Esteban Ferro, PhD student.
Supervisors: Dr. Paula López, Dr. Víctor M. Brea
Lab Head: Prof. Diego Cabello
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Technology: UMC L180 Mixed-Mode /RF
Die size: 5.0 mm x 5.0 mm

Description

Micro-energy harvesting is an attractive way to power systems which have a small form factor, such as implantable or wearable devices or Internet of Things (IoT) nodes. In the case of on-chip energy harvesting transducers, the scavenged power can be as low as a few nW, being a challenge to work with such low power levels without external control signals or start-up mechanisms. The voltage generated by the transducer can also be as low as 0.2 V, requiring efficient DC-DC converters. Boost DC-DC converters are highly attractive because of their high efficiency, but the requirement of an off-chip inductor restricts their domain of application. Switched capacitor DCDC converters (charge pumps) are appropriate because they can be fully integrated with a relatively small form factor.

Fig. 1: Layout of the designed circuit
Fig. 2: Photograph of the fabricated chip.

This tape out includes a Power Management Unit (PMU) powered by a 1 mm^2 on-chip solar cell (photodiode) to reach output voltages higher than 1.1 V. A continuous and two dimensional onchip Maximum Power Point Tracking (MPPT) to adjust the gain and the switching frequency of the main charge pump of the PMU leads to a cold start-up from a harvested power of nW without any external kick off or control signal.

Results

The on-chip solar cell and a PMU are made on the same substrate in standard UMC 0.18 μm CMOS technology. Different photodiode configurations combined with the PMU were fabricated. The photodiode with fingers of 1 μm pitch provides the best efficiency. The end-to-end efficiency is about 25% and 40% for low and high illumination, respectively. The proposed chip is able to start-up from nW of harvested power, including on-chip harvesting and MPPT capabilities on the same substrate.

Why Europractice?

The University of Santiago de Compostela has worked with Europractice in UMC 0.18 μm technology fabrication for many years. We have benefitted from their competitive prices, as well as from their expert advice and comprehensive guidance for using the design kits, libraries and design software, being crucial for a successful chip design and tape out

32-channel self-triggered ASIC for GEM detectors

National Research Nuclear University MEPhI, ASIC lab and Department of Electronics, Moscow, Russia

Contact: Eduard Atkin
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Technology: UMC L180 Mixed-Mode/RF
Die size: 5000 x 5000 µm

Application

During last few years a multichannel readout ASIC for GEM detectors with an asynchronous (self-triggered) architecture has been being developed at MEPHI. Nowadays the GEM detectors are commonly used in large-scale experiments at different accelerators. The presented ASIC is focused on GEM detectors, which are the key elements of the muon chamber (MUCH) of the CBM experiment at FAIR [1].

The ASIC was designed on the basis of results, received from two previous mini-ASICs, prototyped via Europractice, and their lab tests [2, 3]. These prerequisites have provided both characterization of main building blocks and study of analog channel structure. The current design is the first version of a full-scale 32-channel readout ASIC. As a result of the channel data processing there can be obtained both the signal amplitude and timestamp.

ASIC structure is shown in Fig.1. It contains 32 analog channels, 32 SAR ADCs, a digital back-end, slow control and synchronization part, high speed I/O circuits (SLVS transmitters/receivers) and PLL for on-chip high frequency generation. The ASIC also includes 2 test channels with analog drivers for monitoring internal signals and pads for probe station tests.

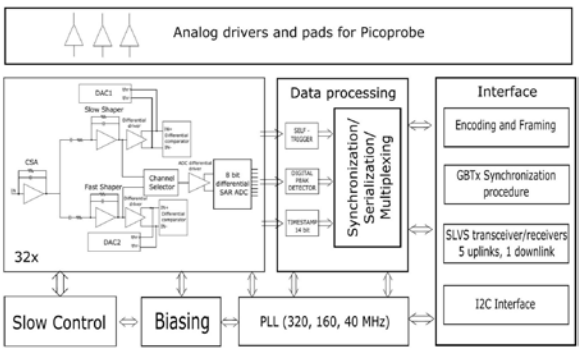

Fig.1: ASIC structure

Since the GEMs in MUCH will have different granularity, the requirements for the front-end electronics are different depending on its location. Thus, each analog channel consists of the preamplifier (CSA) followed by two chains: a slow channel optimized for S/N ratio in order to use it in the periphery, and a fast one, adapted to the hit rate of the inner detector part, where the occupancy is the highest. The fast channel is also supposed to be used for the timestamp determination. Both channels are realized with CR-RC shapers with different peaking times, 60 and 260 ns accordingly. The measured ENCs of the fast and slow channel shapers are no more than 2000 and 1500 el correspondingly at 50 pF detector capacitance. The channel is optimized to operate with the negative charge polarity. The preamplifier dynamic range is up to 100 fC. The channel occupancy is up to 1 MHz. The shaper outputs are connected to the drivers, which make a single-ended to differential signal conversion. Further, the signals are supplied to the differential comparator inputs. For setting the threshold of the comparators current 5-bit DACs are used. The DACs set the threshold up to 80 mV with INL 0.20 LSB and DNL 0.25 LSB. The signal from either slow or fast shaper (depends on the occupancy) is processed by an 8-bit SAR ADC with a 40 Mbps sampling rate and 1.5 mW power consumption. The ADC is followed by a digital peak detector. The peak detector has a function of the false peak find prevention due to the presence of noise spikes. The chip has fast and slow discriminators. The fast discriminator output is connected to a timestamp block. Both fast and slow discriminators can be used by the logic for hit overlap detection. When the event in the channel occurs, the fast discriminator fixes the time of a 14-bit counter in the Gray code.

The digital back-end of the ASIC generates data with information about amplitude of the signal, timestamp, overlap of the signals and address of the channel. The data transfer protocol is based on [4] for compatibility with other ASICs to be used in CBM experiment. The data are combined in a 29-bit packet. Each packet is converted by the interface part into a 40-bit word and transmitted to GBTx.

Results

The ASIC was implemented in a 0.18 µm UMC L180 Mixed-Mode/RF CMOS process and packaged into CQFP 208. The layout as shown in Fig. 2, while the evaluation board and, as an example, transfer characteristics of the CSA and shapers

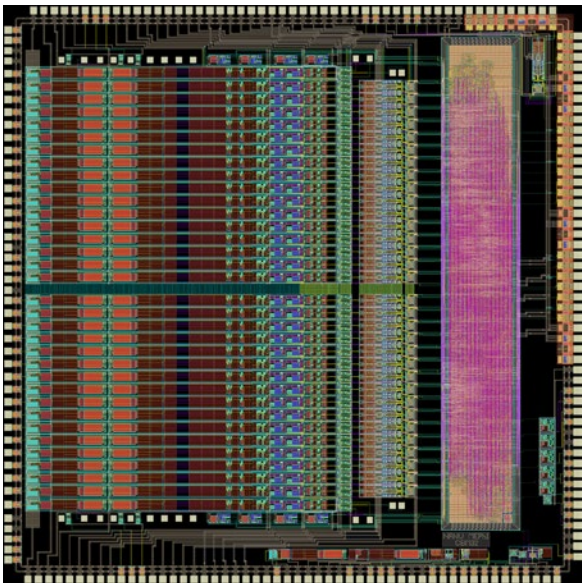

Fig.2: Layout

are shown in Fig. 3 and 4. The measurement results [5] confirmed the ASIC functionality.

Why Europractice?

Europractice provides a unique opportunity for our University to have a well scheduled access to a wide range of advanced technological processes. It is also important, that the approach is cost-effective. This allows making a simple choice of right technology for each R&D project, keeping in mind possibility of further engineering runs for a small volume reproduction of chips. An expert support on installation and usage of PDKs jointly with advanced EDA tools gives additional benefit to our designers.

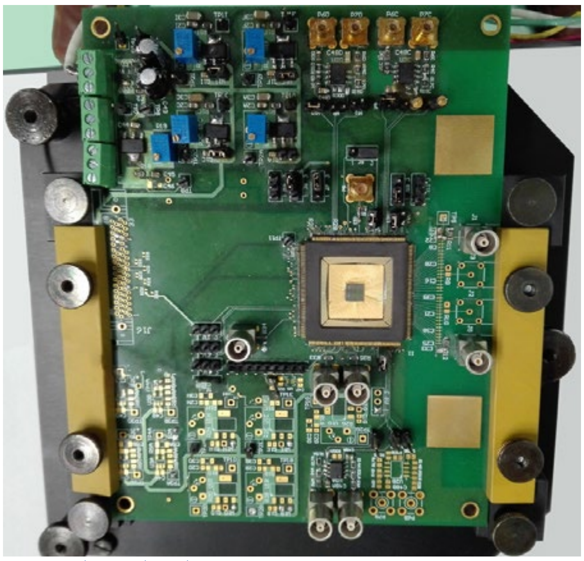

Fig. 3: Evaluation board

Acknowledgement

This work was supported by the Ministry of Education and Science of the Russian Federation in the frames of the Competitiveness Program of National Research Nuclear University MEPhI and grant no.14.A12.31.0002 in accordance with the RF government resolution no. 220.

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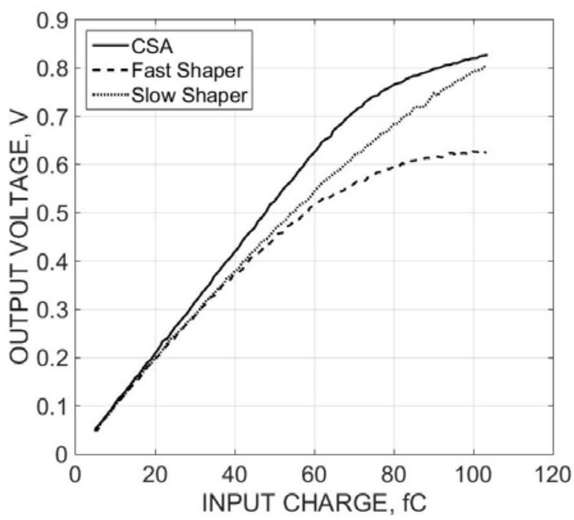

Fig. 4: Transfer characteristics of the CSA and shapers

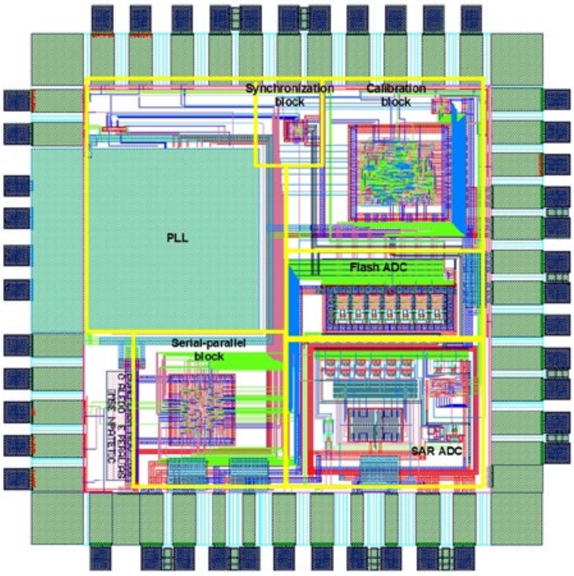

Fig. 1: Complete chip layout

Flash ADC with Digital Background Offset Self-Calibration Technique

Microelectronic Institute of Seville (IMSE-CNM-CSIC), University of Seville, Spain

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Technology: UMC 180nm MM/RF
Die size: 1525mm x 1525mm

Description

Analog-to-digital converters (ADCs) are one of the main building blocks in current electronic systems, especially in communication, signal processing and biomedical fields. The evolution of ADCs has been changing with the requested specifications of the devices technology.
Among the different types of ADCs, flash converter is the simplest and fastest architecture, achieving a great bandwidth (tens of GHz). Errors due to inaccuracy and element mismatches affect greatly to the ADC performance. Offset due to mismatch errors is the main issue in flash ADCs, which decreases the flash linearity. Therefore, using calibration techniques to reduce the offset is crucial in this kind of converters. There are many different offset calibration techniques applied to flash ADCs. Background calibration methods are really popular since they are accomplished simultaneously and continuously without ceasing the normal operation of the ADC. Also, digital offset calibration is quite often employed due to its reduced circuitry, cost and power consumption. These digital methods, based on adaptive processing algorithms, greatly reduce the cost of the circuit without attenuating its performance, even for rather complex digital algorithms.

The aim of the chip, presented here (Fig. 1), is to prove the obtaining of high accuracy in a low resolution, high-frequency flash ADC through background calibration. To achieve this, the idea of [1] has been implemented. It consists of a low-cost background digital technique for calibration the comparator offsets in flash ADCs. In our design, a low-resolution reference-less 3-bit flash ADC with a simple structure and reduced area has been considered. Instead of using a resistive ladder, transitions are implemented by a forcing mismatch system implemented in each comparator input front-end. To calibrate the offset of the flash ADC, a slower and more accurate auxiliary ADC (with at least 2 more bits than flash) is used. The chosen auxiliary ADC is a 6bit SAR type.
Calibration process is assisted by a digital adaptive algorithm which is implemented in a third block (calibration block). Its outputs act on input forcing mismatch system of each comparator of the flash, correcting their offsets. In addition, the die contains a PLL, a synchronization block that helps synchronizing both ADCs sampling clocks, and a serial-to-parallel circuit to inject programmability in all blocks. For example, in all comparators of flash ADC it is possible to inject 16 different offset values in the range of ±2 LSB.
The integrated circuit was fabricated in the context of project “n-PATETIC” [2].

Results

The die was wrapped in a QFN32 package and tested in a home-made four-plane FR4 PCB. Measured results prove the correct designed calibration strategy as well as the reliability of the technology. Measurements done when ADCs work simultaneously show that the 3-bit flash ADC achieves an ENOB of 2.8 bits up to 250 Msps in its default state (no offsets injected) and the 6bit SAR ADC reaches an ENOB of 5.2 bits up to 5 Msps (Fig. 2). This good performance of SAR ADC is enough to guarantee the offset calibration process. Offset calibration method has been tested with successful results, thanks to the full control of the injected offset in each comparator (Fig. 3). This rather good performance of this offset calibration method improves flash accuracy and speed, by relaxing the architecture complexity design. Also, both power dissipation and area are lessened due to the simpler architecture.

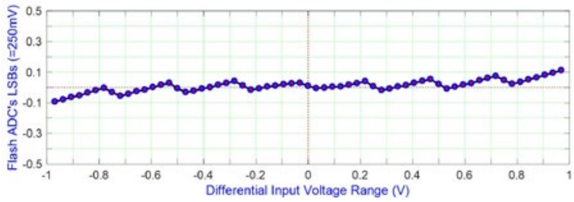

Fig. 2: 6bit SAR ADC linearity performance (Sampling 1 Msps): Transition errors respect to 2.0-Vpp 6bit ideal ADC in LSB units of the 2.0V 3bit Flash ADC under calibration

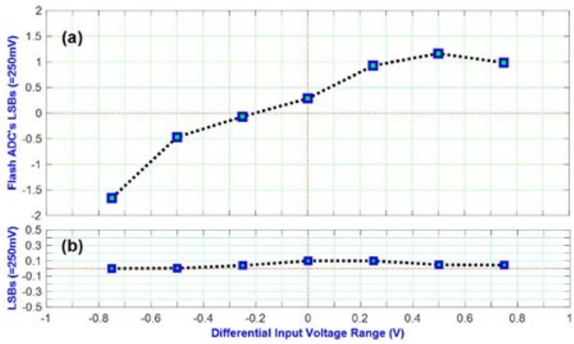

Fig. 3: 3bit Flash ADC linearity performance (Sampling=150 Msps): a) Example case of injected transition errors before calibration process in LSB units, b) Typical transition errors after stabilization of background calibration process.

Why Europractice?

Europractice has been widely used in our Institute and University during many years as part of the integration, bonding and packaging processes. Europractice provides not only an effective and fast service, but also an excellent qualified technical support team, which is essential for a successful IC design and tape out. Also, the great variety of fabrication technologies and the mini@sics program, which allows fabricating small area dies at affordable prices, make Europractice service a great choice.

References

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Ultra-low power wireless interface for implantable medical devices

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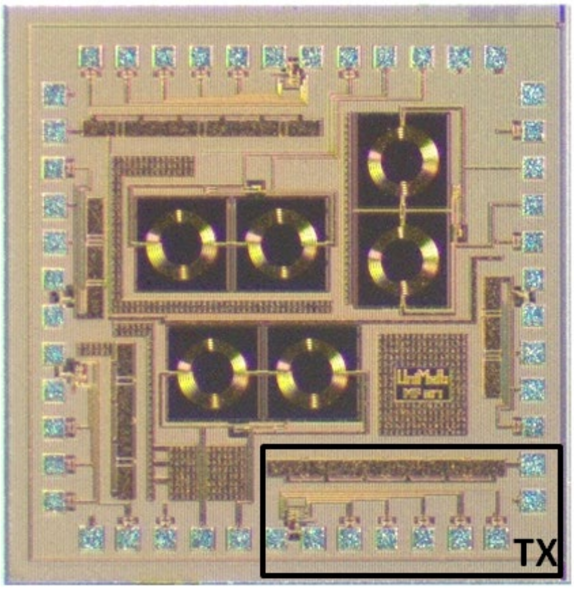
Technology: UMC L180 Mixed-Mode /RF
Die size: 1525 µm x 1525 µm

Description

Over the past decades, wireless implantable micro-devices have been considered as potentially efficient and cost-effective tools for monitoring of physiological parameters as well as stimulation of biological tissue. Energy scavenging has recently attracted attention as an interesting option for powering simple, low-power micro-devices. However, the power that they can generate is very limited. To be able to power a system using energy scavengers, the power consumption of the system should be reduced significantly. In any implantable biomedical devices, the wireless communication unit is considered to be the most power-hungry component. Hence, a lower power wireless interface is desired in such systems. This project focused on design, development, and fabrication of a state-of-the-art, ultra-low-power transmitter for biomedical implants. The transmitter operates at 2.4 GHz frequency band. To realize such a low power transmitter, the circuit was designed and fabricated using UMC 180 nm CMOS technology through the Europractice mini@sic program. Power reduction techniques were taken into consideration to reduce both active and leakage power of the system. To increase the radiation efficiency of the transmitter, a mm-size, silver-diamond loop antenna was fabricated. The antenna was designed to be employed directly in the oscillation tank of the transmitter circuitry. Synthetic diamond grown via chemical vapour deposition (CVD) was used as a substrate to house a silver active braze alloy (ABA) antenna due to its biocompatibility, sterilizability, mechanical strength, and longevity. CVD diamond is easily shaped by laser so it can be used not only for enclosing the antenna but also for encapsulation of the whole micro-device.



Fig; !. Photogrqph of the fqbricqted circuit

Results

The transmitter was fabricated in UMC 180 nm CMOS process and occupied an area of 0.2 mm². The overall size of the die was 1.5 × 1.5 mm² including some other RF circuits (Fig. 1). The power consumption of the transmitter at 2.47 GHz while transmitting data at the data rate of 10Mbps was less than 100 uW, and phase noise of less than -110 dBc/Hz at 1 MHz offset was measured. Also, compared to the PCB antenna, higher radiation efficiency was achieved by using the silver-diamond antenna. The tests have not yet been completed and are still ongoing.

Why Europractice?

mini@sic Europractice MPW program offers designers and researchers the opportunity to prototype their ideas and designs at an affordable price. Europractice staff provide excellent technical support throughout the different stages of the tape-out. They also offer a packaging service, which is very convenient.

nSYNC, a new readout chip for the future upgrade of Muon Detector LHCb experiment at CERN

INFN Sezione di Cagliari, Italy

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Technology: UMC 130nm L130 Logic

Die size: 4.4 x 3.8 mm²

Description of the circuit and results

nSYNC is a VLSI integrated circuit developed in UMC 130 nm technology. It is a building block of the readout system for the upgraded LHCb Muon detector.

The chip has 48 input channels from which it will receive the data from the front-end electronics sited on the detector.

Each input channel is equipped with its own TDC to measure the incoming signal phase with respect to the 40MHz master clock.

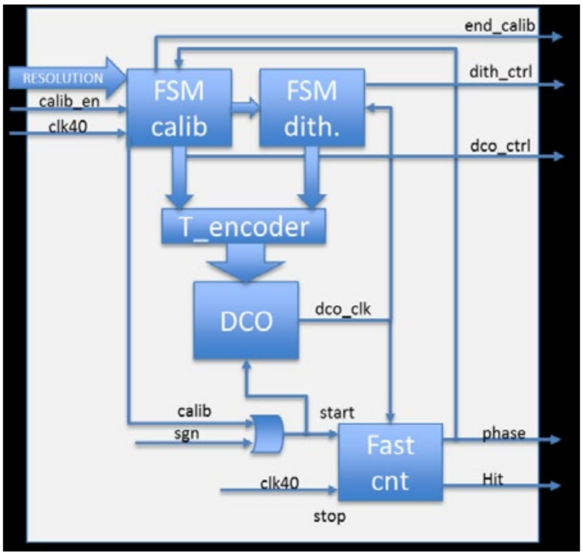


Fig. 1: Block diagram of a time-to-digital converter (TDC)

Table 1: Specifications of the designed time-to-digital converter (TDC)

	TDC
Technology	UMC 130 nm
Size	90 x 171 mm² (0.0154 mm²)
Resolution Step Range	8 – 32
Max Res. Achievable	About 750 ns
Reference clock	40 MHz
Voltage	1.2 V
Working Power Cons.	Average 500 mW
Rest Power Cons	5 mW

The main core of the TDC is a fully digital DCO (named Giordano-DCO) developed for ALLDIGITALL INFN experiment and that is patented. The DCO is calibrated in order to have each slice equal to the DCO output period. The frequency match is improved by means of a dithering system. The phase measurement is activated by the incoming signal that switches the DCO on. The DCO clock drives a fast counter, which "counts" the number of DCO clock periods. When the rise-edge master clock arrives, the fast counter (and so the DCO) is stopped, the measurement is completed and can be stored in an output buffer. The choice to keep the TDC silent (not running) between two consecutive measurements is based mainly on power consumption consideration. Indeed, in order to reduce the power consumption per channel, it is important to reduce the switching power when not needed.
TDC layout has a size of $90x171mm^2$. The width of 90 mm is equal to the minimum pitch guaranteed by the Europractice standard assembly and the power rails are designed in a way the TDC can be placed side by side just in front of the corresponding input pad.

At the TDC output we have two information @ 40MHz: a flag giving the simple binary Hit/NoHit info and a 5 bits-wide word with the measured phase. These information go through a pipeline with programmable length in order to align different channels with different arriving time. The TDC information will be used internally to build a histogram of the incoming signal phase in order to perform the so-called fine-time synchronization that is crucial to achieve the required muon system efficiency. The histograms will be read back through the ECS interface (I2C).
The aligned data coming output from the TDC's are tagged with a unique 12-bit BXid identifier.
The new complex-data is managed to create the extended frame with Header+HitMap+all-TDCdata.
The TDCdata are then Zero Suppressed in order to fit the output frame 112 bit wide, which is finally transmitted at 320MHz.
The TDC block was prototyped using the mini@sic runs offered by Europractice. Extensive test were performed on this fundamental block, showing good results inside the specification.
The nSYNC was prototyped with a MPW run and tested in all its aspect. In particular the 48 integrated TDCs were tested, showing uniform results in agreement with the prototype ones.

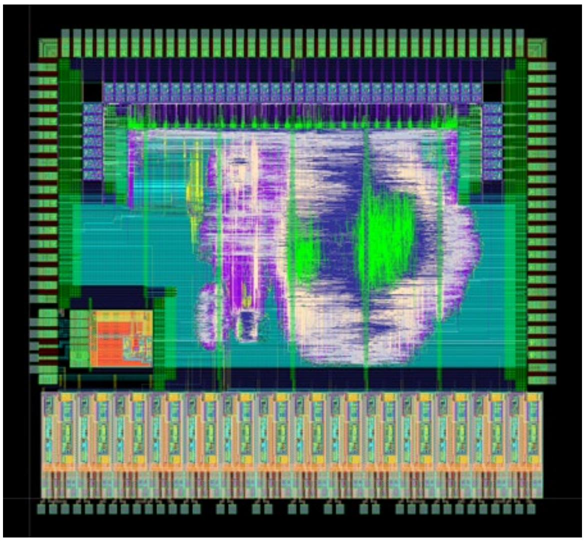


Figure 3: Illustration of the designed circuitry

After all these tests, the nSYNC was tested mounted on the final board and a full chain test was performed to verify all its capability to fulfil the system requirements. The next steps will be a small volume production to equip the LHCb Muon Detector at CERN, upgrading the readout capability to face the new phase of the experiment.

Why Europractice?

We participate at the EUROPRACTICE consortium from the 1990's, with tens of chips produced in different technologies. As part of our research it is important to have easy access to state of the art technologies. Our project are always R&D projects, with design at the level of prototype most of the time. When our needs grow in number we are always at the level of a small volume production. The EUROPRACTICE IC service is fundamental to give us the possibility to explore these technologies and to realize our custom electronics for our experiments. Custom designed microelectronics components designed in advanced technologies are vital parts of today's complex scientific instruments. The services provided by EUROPRACTICE are allowing a large community of physicists and engineers working for these projects to use these technologies for the construction of such instruments with a centralized high quality support. In particular, during our experience using UMC technologies, we always received an incredible support from the EUROPRACTICE engineers, in every design aspect and phase. The help received is invaluable and the results obtained would be very much hard to reach without their constant support.

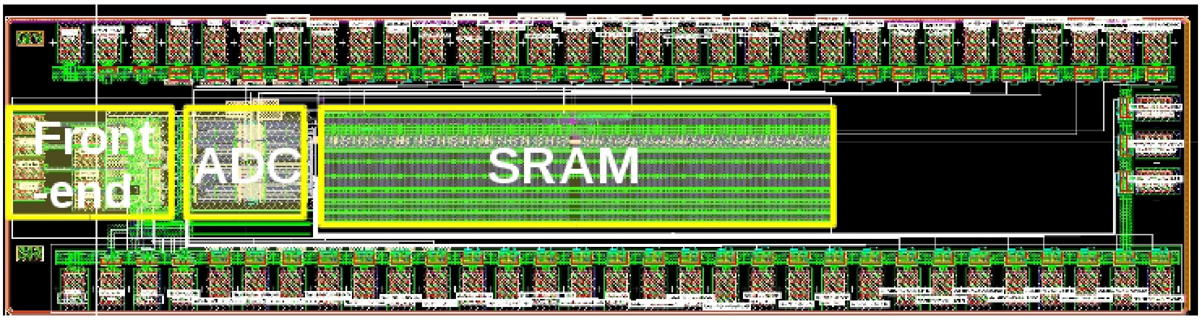


Fig. 1: Layout of the test chip, containing 1 circuit block: 8 CSAs + 2 CDS buffers +2 ADCs.

A readout ASIC for Gotthard-II X-ray detector applied at the European X-ray Free Electron Laser

Paul Scherrer Institute, Detectors Group, Synchroton Radiation and Nanotechnology Division, Villigen-PSI, Switzerland

Contact: Xintian Shi, Roberto Dinapoli, Davide Mezza, Aldo Mozzanica, Bernd Schmitt, Jiaguo Zhang
Email: xintian.shi@psi.ch
Technology: UMC L110AE 110 nm CMOS
Die size: 6500 µm x 5500 µm

Introduction

The European X-ray Free-Electron Laser (XFEL) is a research facility of superlatives: It generates ultrashort X-ray flashes – 27000 times per second and with a brilliance that is a billion times higher than that of the best conventional X-ray radiation sources. Using the X-ray flashes of the European XFEL, scientists will be able to map the atomic details of viruses, decipher the molecular composition of cells, take 3-D images of the nanoworld, film chemical reactions, and study processes such as those occurring deep inside planets.
The Gotthard-II is a 1-D microstrip detector specifically developed for the European XFEL. The peculiar time structure of the European XFEL beam, 10 Hz bunch trains with 2700 4.5 MHz bunches each, requires the chip to be able to achieve a maximum frame rate of 4.5 MHz, while its very high brilliance translates in a challenging requirement for the dynamic range, which has to be up to 104 photons. Single photon resolution is required in case of low photon flux (<70-80 12.4 keV photons/pixel) as well as a negligible noise, over the whole dynamic range, with respect to the fluctuations generated by the Poisson distribution of the incoming photons. Gotthard-II is going to be the only detector capable of measuring all the bunches in a train.

Description of the design

Each readout ASIC contains 128 charge sensitive preamplifiers (CSA), 32 correlated-double-sampling (CDS) buffers, 32 12-bit 18MS/s SAR ADCs and 16 SRAMs with a size of 2720 x 112 bits each. During the bunch train operation, the charge generated by the photon pulses in the sensor is collected by the CSA and converted into voltage signals every 220ns. The CSA has 3 automatically adaptive gain stages to achieve high dynamic range and retain single photon resolution in the highest gain stage. The CDS buffer converts the single-ended output signals of the CSA into fully differential signals and feeds them into the ADC. The digital outputs of the ADC and the gain bits of the CSA are stored in the SRAM. During the 99.4 ms gap between the bunch trains, the 2700 images stored in the SRAM are read out of the chip. Due to performance and physical layout considerations, the whole chip consists of 16 blocks. Each block contains 8 CSAs, 2 CDS buffers, 2 ADCs and 1 SRAM. Several prototype chips have been designed and tested. The dedicated engineering run is planned for the middle of 2018.

Results

For the front-end circuit (CSA + CDS), the measured equivalent input noise charge is about 300 e- rms @ 4.5 MHz frame rate. The measured dynamic range is higher than 104 x 12.4 keV photons. For the ADC, the measured effective number of bit (ENOB) is about 9.8 bits @ 18 MS/s and the power consumption is less than 1mW. The last prototype was submitted in November 2017 with some fixes to improve the ENOB of the ADC and the noise of the front-end.

Why Europractice?

PSI has worked with Europractice more than 15 years. We really appreciate the affordable access to CAD tools and different technologies using Europractice MPW runs, as well as the high quality service and support provided by Europractice.

Towards a more secure RISC-V design

ETH Zurich, Integrated Systems Laboratory (IIS), Switzerland
TU-Graz, Institute of Applied Information Processing and Communications (IAIK), Austria

Contact: David Schaffenrath, Frank K. Gurkaynak, Mario Werner, Stefan Mangard
E-mail: kgf@iis.ee.ethz.ch, stefan.mangard@iaik.tugraz.at
Technology: UMC L65N Logic/MM/RF - LL
Die size: 2626 µm x 2626 µm

Description of the project

Security is becoming one of the main issues of computing these days. Recently released attacks show that modern processors are susceptable to all sorts of attacks. At ETH Zürich in collaboration with the University of Bologna, we have been working on open source silicon-proven implementations of the RISC-V architecture (http://riscv.org) by Berkeley using a permissive Solderpad license (http://solderpad.org/licenses) derived from the Apache v2.0 license explicitly to support open source hardware. Working on an open source hardware has additional benefits for the security community as it allows a more thorough examination of the internals of the implementations allowing potential weaknesses to be identified more easily leading to ultimately more secure systems.

We have been collaborating with the Institute of Applied Information Processing and Communications (IAIK) of TU Graz over the past 10 years in finding ways to improve the security of digital systems. In this project we have concentrated on improving the security of our own RISC-V based processors by two separate measures. First adding the necessary modifications to the hardware to allow it to run the SEL4 operating system and secondly adding hardware countermeasures against fault attacks in the control path of the processor. In a fault attack, the adversary tries to interrupt the normal flow of the program. This can be used to bypass security checks and/or execute arbitrary code on the machine.

In this design, we add an additional pipeline stage to the processor that decrypts the instruction fetched by the processor based on its internal state. The program is compiled in a way that only the correct order of execution would allow a meaningful execution, any interruption in this flow would result in an exception within 3 clock cycles.

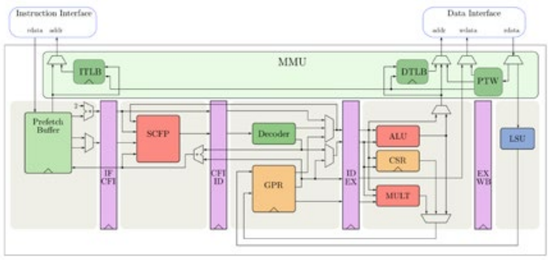


Fig. 1: Pipeline stage: the core with fault attack tolerance

Results

We have developed a test chip called Patronus that contains three different 32-bit RISC-V cores optimized for low area footprint, one of which contains the control flow integrity solution (CFI) that should make it increasingly difficult for attackers to launch fault attacks. The additional CFI stage has an area overhead of only 25 kGEs and the whole system is able to run at 160MHz clock at worst case corners (1.02V, 125C) in the UMC65nm process.

The design also contains several SHA-3 accelerators added with different side channel mitigation techniques and enough memory (384kBytes) to allow SEL4 to be loaded into the on-chip memory.

Fig. 2: Color picture of the PATRONUS chip taken through a Leica microscope

Why Europractice?

As ETH Zurich we have enjoyed a long and fruitful relationship with Europractice IC service resulting in over 150 chips in the last 10 years. We are particularly proud of our student projects that allow Master students to take part in semester theses where they can work on their own ASIC designs in parallel to our VLSI lecture series. The lectures and the associated exercises allow give the students the necessary background and experience to work on their own chips. David Schaffenrath that designed Patronus as part of his master thesis came as an exchange student from TU-Graz and took part in this lecture series as well.

Such master projects are made possible by the longstanding and fruitful relationship we have established with Europractice IC service as well as the CAD tools obtained through the Europractice design tools and configurable platforms. Members of the Europractice IC service have been instrumental in establishing the design flow and helped us find customized solutions for our student project requirements.

CHIPMUNK: A Systolically Scalable 0.9 mm², 3.08 Gop/s/mW @ 1.2 mW Accelerator for Near-Sensor Recurrent Neural Network Inference

ETH Zurich, Integrated Systems Laboratory (IIS), Switzerland

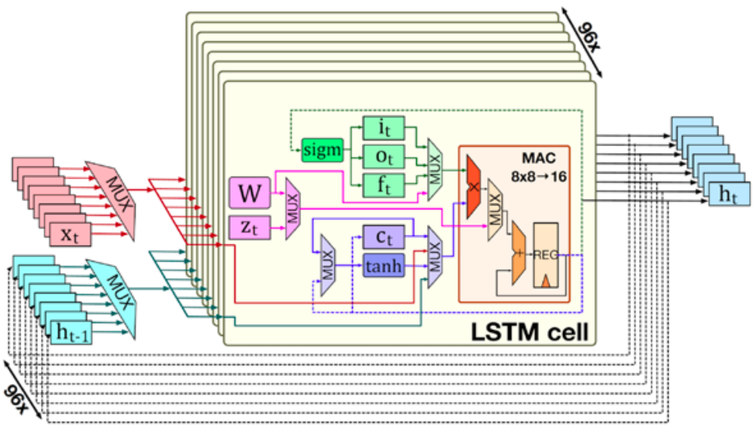
Contact: Francesco Conti, Lukas Cavigelli, Gianna Paulin, Igor Susmelj, Luca Benini
E-mail: fconti@iis.ee.ethz.ch, lbenini@iis.ee.ethz.ch
Technology: UMC L65N Logic/MM/RF - LL
Die size: 1252 µm x 1252 µm

Description of the project

In this work, we present a twofold contribution towards the deployment of Recurrent Neural Network (RNN)-based algorithms in devices such as smartphones, smartwatches and wearables.
First, we designed CHIPMUNK, a small and low-energy hardware accelerator engine targeted at real-time speech recognition and capable to operate autonomously on moderate size Long Short-Term Memory (LSTM) networks. The necessary computing steps are based on the same set of basic operations:
i) matrix-vector products,
ii) element-wise vector products, and
iii) element-wise non-linear activations.

The internal datapath allows to execute these three basic operations as visible in the figure below. The LSTM state parameters are in registers while the vast amount of data are stored on-chip in SRAM banks.
Second, we conceived a scalable computing architecture, apt to operate on bigger LSTM models as well. As the main limitation to the deployment of big RNNs in embedded scenarios stems from their memory boundedness, we designed the CHIPMUNK engines so that they can be replicated in a systolic array, cooperating on a single bigger LSTM network. This methodology allows the acceleration of large-scale RNNs, which can be made fast enough to operate in real-time under realistically tight time, memory and battery constraints without requiring complex, power hungry and expensive high bandwidth main memory interfaces.

Fig. 1: Block diagram of the main computation block in Chipmunk



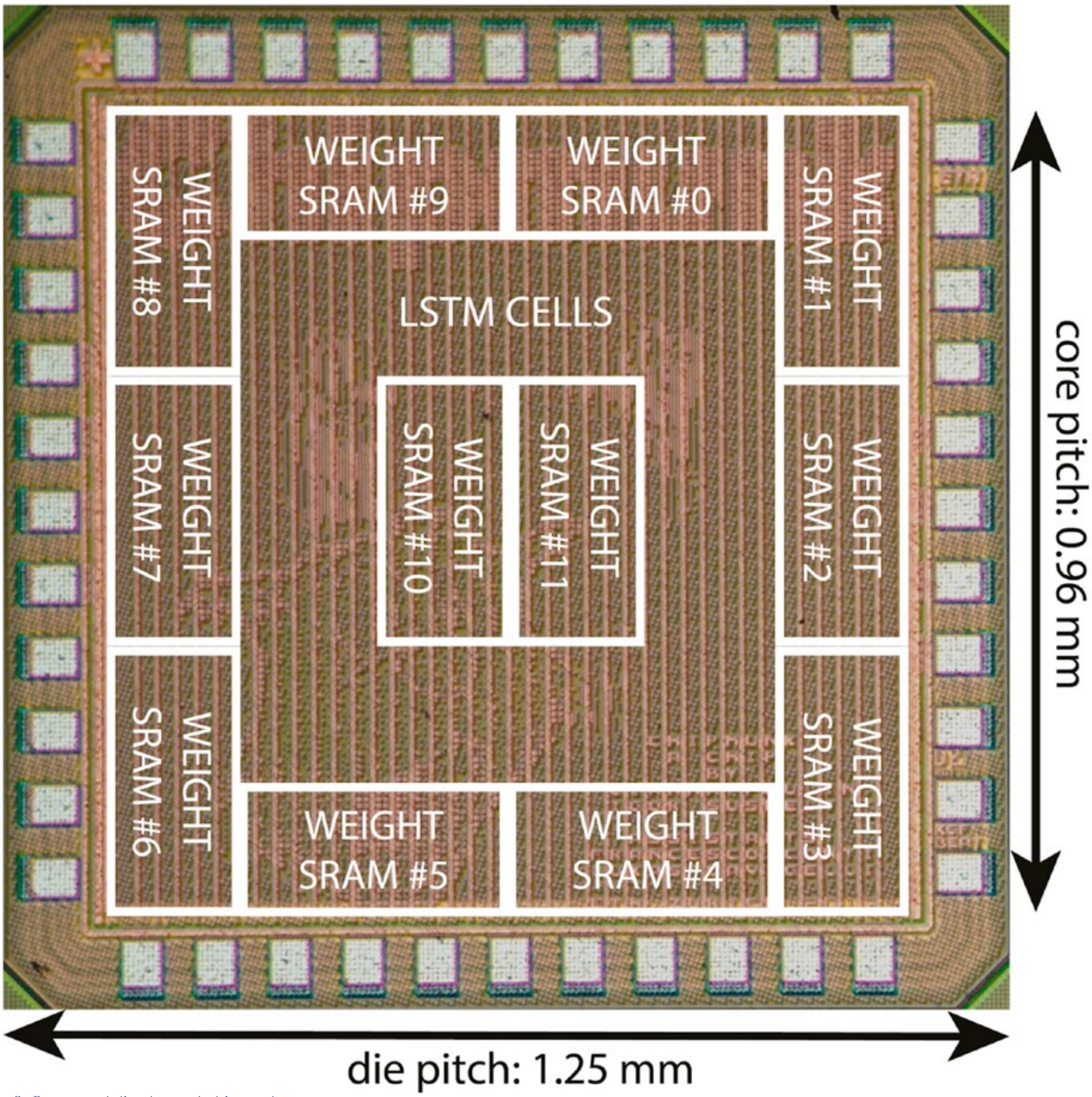


Fig. 2: Annotated die photo of chipmunk

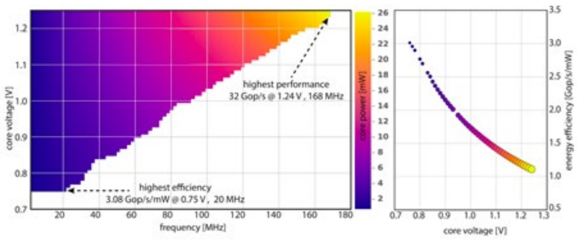


Fig. 3: Measurement results from chipmunk

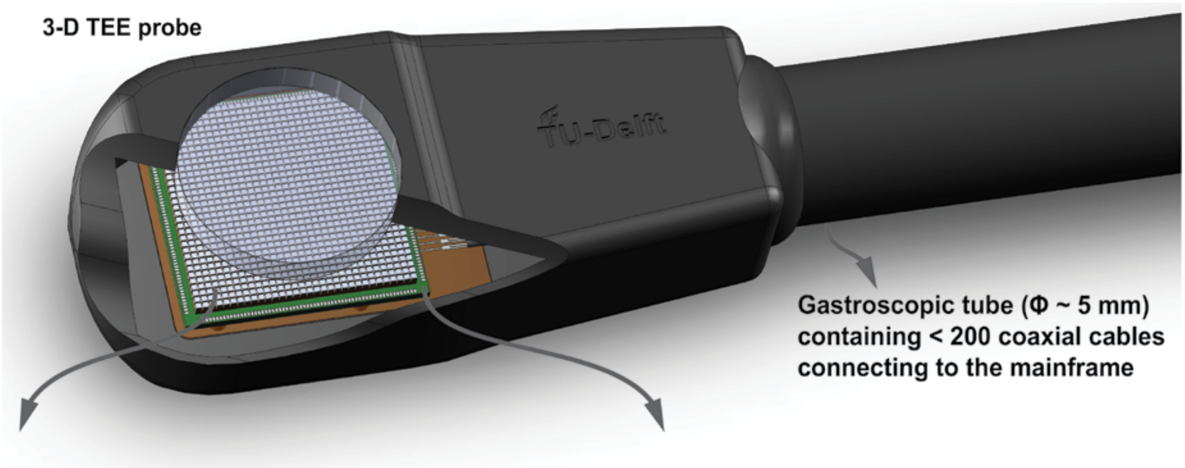
Results

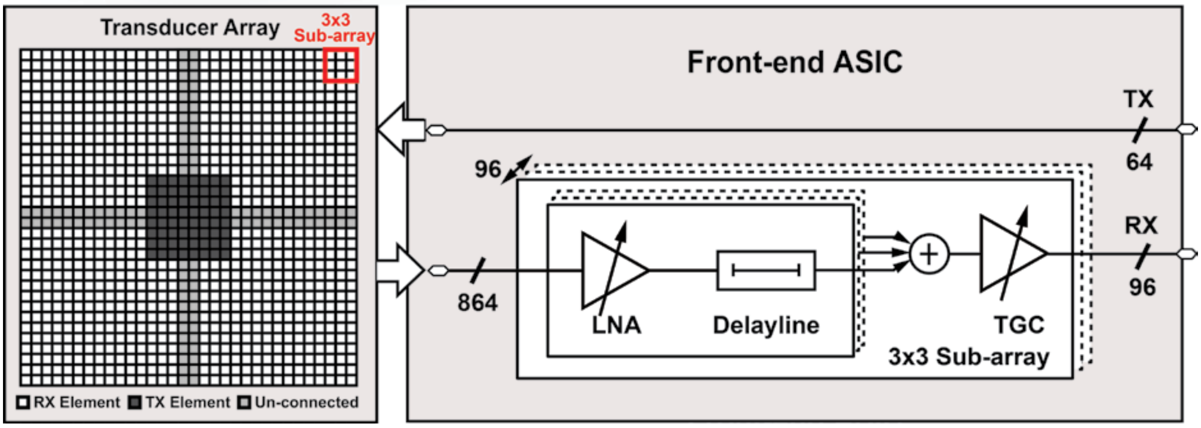
We present silicon results from a prototype chip containing a CHIPMUNK engine as seen in the figure, which has been fabricated in UMC 65 nm technology within 2017 through Europractice; measurement results show that the chip can achieve up to 3.8 Gop/s at maximum efficiency operating point (@0.75 V), consuming only 1.24 mW.

Why Europractice?

As ETH Zurich we have enjoyed a long and fruitful relationship with Europractice IC service resulting in over 150 chips in the last 10 years. We are particularly proud of our student projects that allow Master students to take part in semester theses where they can work on their own ASIC designs in parallel to our VLSI lecture series. The lectures and the associated exercises allow give the students the necessary background and experience to work on their own chips. Individual projects are supervised by Post Doctoral researchers and Ph.D. candidates working at the Integrated Systems Laboratory. Gianna and Igor designed the Chipmunk design as part of such a semester thesis and were able to measure the performance of their chip on our own Advantest SoCV93000 tester, allowing them to be part of state of the art research at an early part of their career.

Such semester projects are made possible by the longstanding and fruitful relationship we have established with Europractice IC service as well as the CAD tools obtained through the Europractice design tools and configurable platforms. Members of the Europractice IC service have been instrumental in establishing the design flow and helped us find customized solutions for our student project requirements.





A Front-End ASIC With Receive Sub-array Beamforming Integrated With a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography

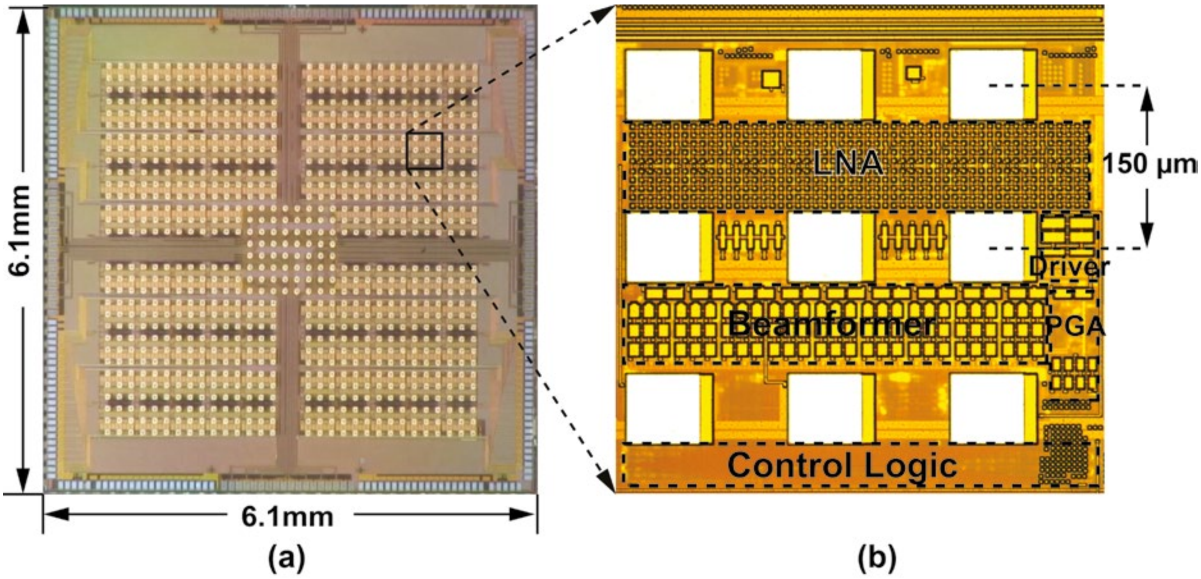
Electronic Instrumentation Laboratory(EI), Department of Microelectronics, Delft University of Technology, The Netherlands

Contact: Zhao Chen, Michiel Pertijs
Email: Z.Chen-3@tudelft.nl; M.A.P.Pertijs@tudelft.nl
Technology: TSMC 0.18u CMOS MS/RF
Chip size: 6.1mm x 6.1mm

Description

Volumetric visualization of the human heart is essential for the accurate diagnosis of cardiovascular diseases and the guidance of interventional cardiac procedures. Echocardiography, which images the heart using ultrasound, has become an indispensable modality in cardiology because it is safe, relatively inexpensive, and capable of providing real-time images. Transesophageal echocardiography (TEE) utilizes an ultrasound transducer mounted on the tip of a gastroscopic tube to make ultrasonic images of the heart from the esophagus[1]. For real-time 3-D imaging, a 2-D array of 1000+ independent transducer elements is needed, presenting an interconnection challenge due to the limited number of cables that fit in the tube. Integrating the transducer array with a front-end ASIC that locally processes the signals is an efficient way to reduce the channel count[2]. Moreover, the strict constraints on the size and power dissipation of the probe tip also make the ASIC design very challenging.

The designed ASIC in this work is optimized in both system architecture and circuit-level implementation to meet the stringent requirements of 3-D TEE probes. It is directly integrated with an array of 32 × 32 piezoelectric transducer elements (Fig. 1), which are split into a transmit (TX) and a receive (RX) array to facilitate the power and area optimization of the ASIC [3]. An 8 × 8 central sub-array is wired out to transmit channels in the external imaging system using metal trace in the ASIC. All other 864 elements connect directly to 96 sub-array receiver circuits, each of which contains a switched-capacitor based beamformer, to realize a 9-fold cable reduction. Besides, an ultralow-power low-noise amplifier (LNA) architecture [4], which incorporates an inverter-based operational trans-conductance amplifier (OTA) with a bias scheme tailored for ultrasound imaging, is proposed to increase the power efficiency of the RX circuitry, while keeping the area compact[1].



Previous page:
Fig. 1: (Top) Photograph of the ultrasound transducer mounted on the tip of a gastroscopic tube; (bottom-left) zoom-in of the ultrasound transducer array; and (bottom-right) block diagram of the front-end ASIC of the designed circuit.

This page:
Fig. 2: (a) Photograph of the fabricated chip; (b) zoom-in of one sub-array receiver in the circuitry.

Results

The ASIC has been realized in a 0.18-µm low-voltage CMOS process with a total area of 6.1×6.1 mm^2, as shown in Fig. 2(a). Fig. 2(b) presents a zoomed-in view of one sub-array receiver that is matched to a 3 × 3 group of transducer elements with a pitch of 150 µm. The fabricated prototype with integrated PZT matrix transducer has been fully evaluated electrically and acoustically. While receiving, the ASIC consumes only 230 mW, which is less than half of the power budget for a 3-D TEE probe. The 0.27mW RX power per element is also the lowest comparing to the prior art.

Why Europractice?

As Electronic Instrumentation Lab, TUDelft, we have been working with Europractice for chip fabrication for many years. Europractice offers very frequent and affordable access to the TSMC 0.18-µm low-voltage CMOS process and the TSMC 0.18-µm BCD process, in which our ultrasound-related chips are fabricated, via its MPW and mini@sic services, thus making the planning of our chip fabrication more flexible. Moreover, we can get quick and useful feedback on our any technical questions related to the process from the Europractice IC service team. We have enjoyed the benefit from the great support service in the past collaboration with Europractice .

Reference

[1]. C. Chen, et al., "A front-end ASIC with receive sub-array beamforming integrated with a 32 × 32 PZT matrix transducer for 3-D transesophageal echocardiography",IEEE Journal of Solid-State Circuits, vol. 52, no. 4, pp. 994-1006, Apr. 2017.

[2]. C. Chen, et al., "A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32×32 PZT Matrix Transducer for 3-D Transesophageal Echocardioaraphv", IEEE Symp. VLSI Circuits, pp. 38-39, June 2016.

[3]. Z. Yu et al., "Front-end receiver electronics for a matrix transducer for 3-D transesophageal echocardiography," IEEE Trans. Ultrason., Ferroelect., Freq. Control, vol. 59, no. 7, pp. 1500–1512, Jul. 2012.

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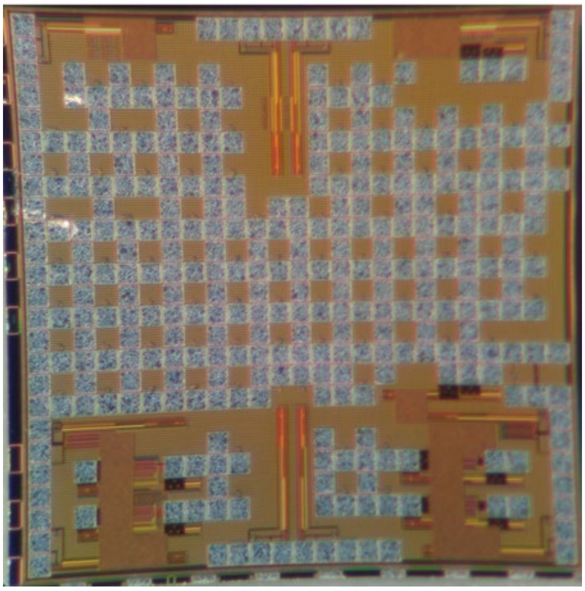


Fig. 1: Photograph of the fabricated chip

Radiation-Hardening bulk CMOS Digital Library Cells

UFRGS – Universidade Federal Rio Grande do Sul

Contact: Student: PhD candidate Pablo Vaz;
Supervisor: Dr-Ing. Gilson Wirth
E-mail: gilson.wirth@ufrgs.br
Technology: TSMC 0.18u CMOS Logic or MS/RF(mini@sic)
Die size: 1660 µm x 1660 µm

Description

The incidence of ionizing radiation may result in undesirable effects in the ICs, such as upsets and even permanent damage to the device's materials. Therefore, applications exposed to a radioactive environment may behave unpredictably, reducing reliability and expected lifetime.

My Ph.D. research project, entitled "Radiation-Hardening bulk CMOS standard cell library design flow based on Enclosed Layout Transistor", proposes a methodology to develop a Radiation-Hardening by Design (RHBD) digital cell libraries in bulk CMOS technology, using real-world constraints.

Therefore, the main focus of this ASIC proposal is to validate this methodology through practical performance measurements under ionizing radiation. As a case study, a group of cells, selected to provide the practical measurements, to characterize the basic building blocks of the RHBD library cells for TSMC 0.18um have been laid-out.

In this group of cells there are single n-pMOS two-edged (Standard) and enclosed-gate (Radiation Hardened) devices, series and parallel devices' configurations, ring oscillators, digital cells, and some calibration structures.

Results

The measurements performed in typical conditions (before incidence of ionizing radiation) have shown that the core elements of proposed RadHard library, i.e., hardened transistors, works as predicted. The DC characteristics validates the effective W/L aspect ratio calculation for enclosed geometries as well as the proposed PN ratio have been shown as an effective solution to size radiation hardened digital cells.

The next step might be the radiation test in which the circuits will be exposed to high levels of ionizing radiation during their operation.

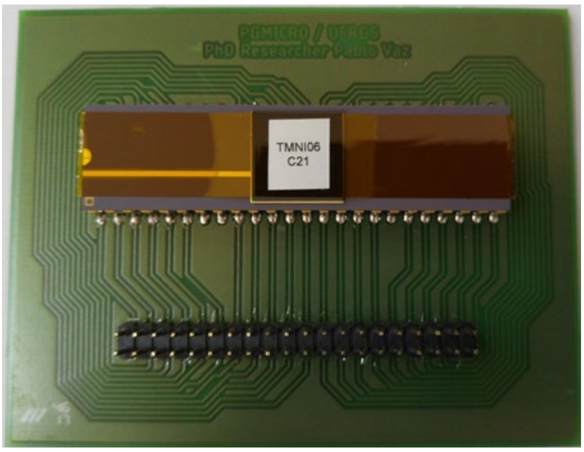
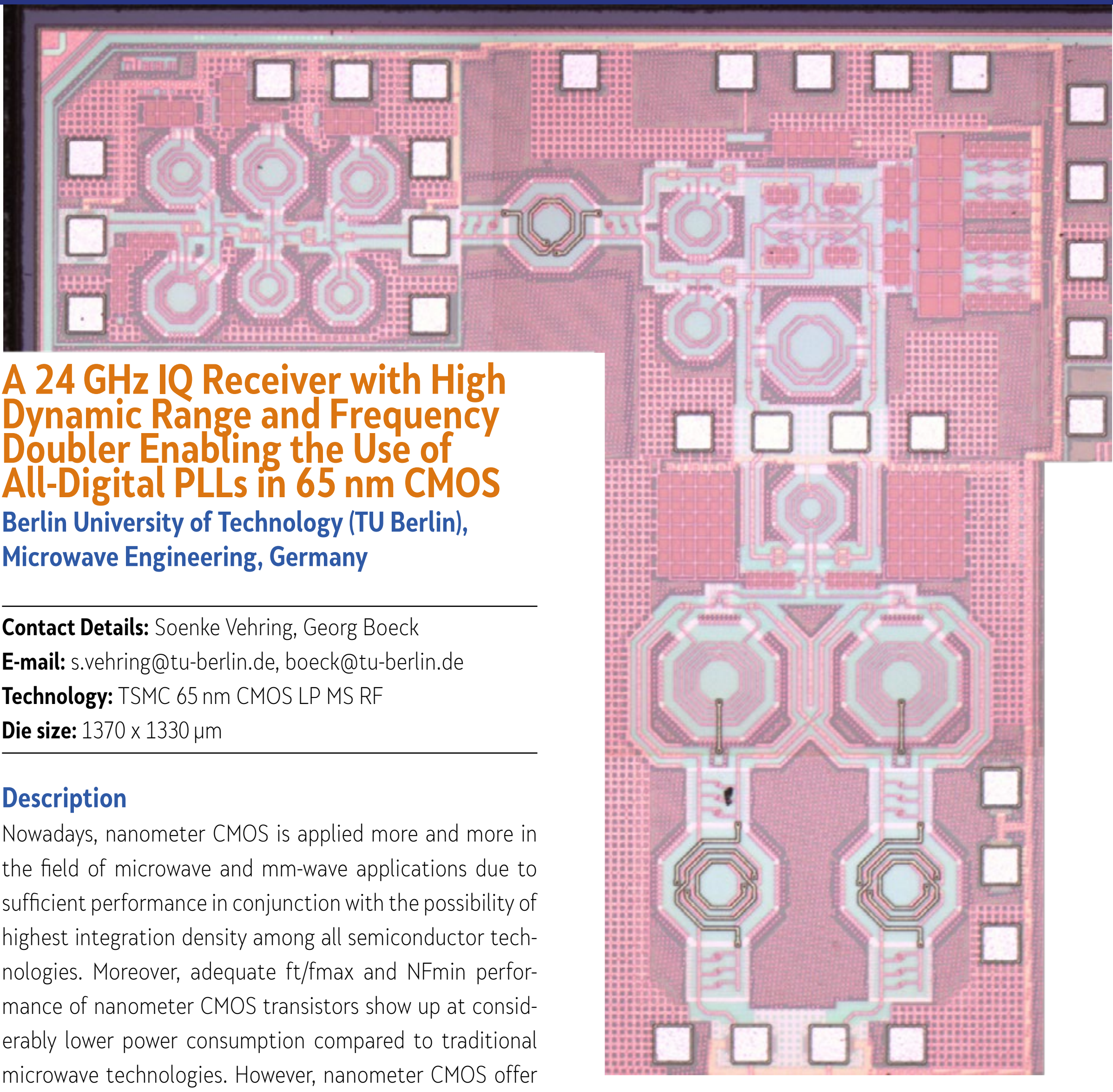


Fig. 2: Photo of the chip in the final package

Why Europractice?

Europractice gives the possibility to access foundry services of a modern semiconductor process (180nm) would not have otherwise a necessary case study to validate the PhD thesis. We have an excellent technical support during design phase, submission and even at packaging process.



A 24 GHz IQ Receiver with High Dynamic Range and Frequency Doubler Enabling the Use of All-Digital PLLs in 65 nm CMOS

Berlin University of Technology (TU Berlin), Microwave Engineering, Germany

Contact Details: Soenke Vehring, Georg Boeck
E-mail: s.vehring@tu-berlin.de, boeck@tu-berlin.de
Technology: TSMC 65 nm CMOS LP MS RF
Die size: 1370 x 1330 µm

Description

Nowadays, nanometer CMOS is applied more and more in the field of microwave and mm-wave applications due to sufficient performance in conjunction with the possibility of highest integration density among all semiconductor technologies. Moreover, adequate ft/fmax and NFmin performance of nanometer CMOS transistors show up at considerably lower power consumption compared to traditional microwave technologies. However, nanometer CMOS offer only low supply voltages of around 1.2 V in the 65 nm node which limits the achievable linearity of microwave receivers. Modern system designs try to serve for a wide range of applications in order to create high demand and enable the mass-production. Under mass-production conditions CMOS is incomparably cheap.

In this project a 24 GHz IQ receiver with high dynamic range is developed. The receiver can be used in case of long and short distances. Therefore, the receiver offers high gain (~26 dB) and low NF (~5 dB DSB) while offering high IP1dB (~-17 dBm) at moderate power consumption of only 50 mW. In order to achieve these results, a three stage common-source LNA with high gain and linearity followed by a IQ demodulator based on resistive mixers have been implemented. For lower overall system costs the use of an all-digital PLL (ADPLL) is intended. The ADPLL avoids tuning voltages and filters compared to its analog counterpart. High performance ADPLLs are hard to build at high fundamental frequency due the limited Q-factors of the switchable LC-tanks. Therefore, a fully balanced 12-to-24 GHz frequency doubler with 5 dBm output power has been added. High output power is necessary in order to fully saturate the mixers at their LO port. Between all circuit blocks additional probing pads are implemented for comprehensive test purposes as shown in Fig. 1.

Fig. 1: Photograph of the fabricated receiver.

Why Europractice?

The Europractice MPW service offers access to state-of-the-art CMOS processes at affordable prices. Furthermore, we experience proficient support through the Europractice team during tape-out phase.

Acknowledgement

This work was funded by the German Federal Ministry of Education and Research (BMBF) in the project 'NaLoSysPro' under contract no. 16ES0161.

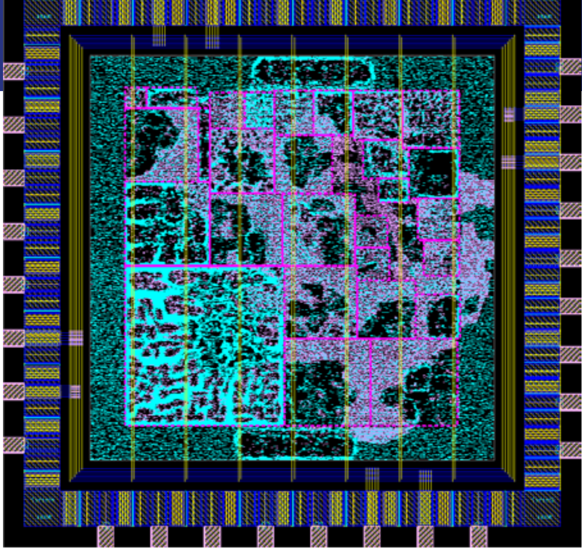


Fig. 1: Layout of the designed circuit

Side-Channel and Fault Injection Evaluation Chip

Chair for Embedded Security, Faculty of Electrical Engineering and Information Technology, Ruhr-Universität Bochum

Contact: Designer: Thorben Moos, PhD student; Supervisor: Priv.-Doz. Dr. Amir Moradi
E-mail: Thorben.Moos@rub.de
Technology: TSMC 65nm CMOS LP MS/RF
Die size: 2000 x 2000 µm

Motivation

It is a well known fact that hardware implementations of cryptographic primitives are in danger of being compromised by adversaries who have physical access to the circuitry. By carefully observing and analyzing the physical emissions that any operating circuit inevitably produces adversaries can learn sensitive information like internal key material of the cryptographic functions. Additionally due to the constant and non-observable physical exposure of the devices to potential adversaries even more invasive attacks like fault injections become possible. Over the years many different countermeasures have been published to decorrelate the measurable physical emissions from the intermediate values of cryptographic algorithms and to detect and resist injected faults. However, due to increasingly altered physical characteristics of CMOS devices in advanced technologies, partially induced by the fast downscaling (like e.g. increased leakage and coupling effects), it needs to be carefully investigated whether these new conditions do not invalidate the underlying assumptions of countermeasures or even introduce new side-channels or weaknesses.

Description

To investigate whether assumptions which are frequently made in state-of-the-art countermeasures against physical attacks do still apply in advanced CMOS technologies (like the 65nm node) we participated in the EUROPRACTICE FIRST ADVANCED USER stimulation action and got a sophisticated test chip fabricated. The overall framework, which can be controlled by two 4-bit input buses (address and data) as well as one 4-bit output bus (data), embeds 27 different cipher cores for our analysis purposes. Each of these cores implements one of the following block ciphers, either with or without state-of-the-art countermeasures applied and in a certain degree of parallelization (unrolled, round-based, serial): PRESENT, PRINCE, Midori, SKINNY, LED, AES. Some of these ciphers are specifically optimized to fulfill a certain design goal (e.g. low-energy, low-latency, ultra-lightweight, high-throughput), which allows us to draw comparisons over the whole range of block cipher applications. During placement we have arranged all cores in clearly delimited geometrical areas around the center of the chip to be able to precisely measure the electromagnetic emanation of individual cipher cores by an EM probe, without damaging the bond wires of the packaged chip. Apart from an external clock supply via a regular I/O cell, each core can also be driven by an internal clock which is generated based on a simple ring oscillator circuit. Additionally two types of pseudorandom number generators (PRNGs), one based on an LFSR the other one inspired by a Keccak threshold implementation, are implemented to satisfy the demand for initial and fresh randomness that state-of-the-art hardware masking schemes have. The input to the masked implementations can either be given in a shared form to the framework or, alternatively, the masks can be generated and applied on-the-fly during the input procedure. The same goes for the unmasking of the output of any masked core. All of the described design decisions have been made to be able to reliably evaluate the cipher cores in different application scenarios. Our final goal is to extract information about the effects that technology changes can have on the physical security of cryptographic hardware and to develop new solutions that stay secure even under these altered conditions.

Experience with EUROPRACTICE FIRST ADVANCED USER stimulation action

This was our first project with EUROPRACTICE and the experience we made was extremely positive. The EUROPRACTICE TSMC team was at all times available for our questions, responded quickly and was patient and helpful with our beginners problems. We believe that EUROPRACTICE offers an unique opportunity for universities and research institutes to get their circuits prototyped in advanced technologies of the leading foundries and we plan to design and tape-out further test circuits in even smaller technology nodes.

A Nonlinear Transfer Function Based Receiver for Wideband Interference Suppression

Eindhoven University of Technology, Mixed-signal Microelectronics, The Netherlands

Contact: Dr.ir. Hao Gao, Prof. dr.ir. Peter Baltus
E-mail:h.gao@tue.nl, P.G.M.Baltus@tue.nl
Technology: TSMC 40nm LP 1P8M5X2Z
Die size: 1920x1920µm

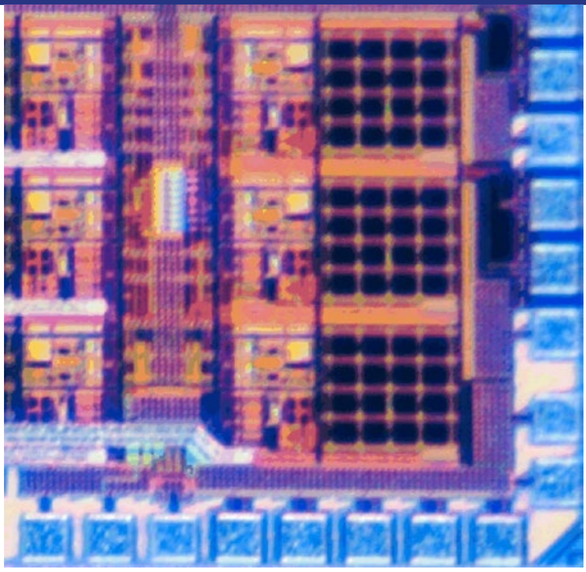


Fig.1: Micrograph of the fabricated chip

Description

Wireless communication is developed to provide faster speed with reliability under the increasing amount of daily usage. In a mobile handset device, several wireless communication standards are supported, such as 2G/3G/4G, Bluetooth, Wifi, etc. In general, there are two solutions for the coexistence of multiple standards operation. One is the narrowband solution and another is the wideband solution. In the narrowband solution, multiple narrow-band receiver front-ends and off-chip surface-acoustic-wave (SAW) filters are required. In the wideband solution, a single wideband receiver covers the spectrum of interest, such as software-defined radios (SDR) and reconfigurable receivers. However, the wideband operation introduces wideband interference problems. The interference comes from the simultaneous operation of multiple radios. The transmitted signal generates interference through the poor isolation between transmitter and receiver in the same device. Also, the transmitted signal generates interference for other devices if they have active receivers operating at the same time.

Wideband receivers for multi-standards operation can simplify the system and lower the cost. In a wideband receiver, the tolerance of large interference signal within the operating band is important. Traditional frequency domain filtering suffers from a lack of filtering capability for in-band interference signals. This project describes a receiver system exploiting nonlinear transfer function. Based on the nonlinear method, the receiver is able to provide frequency-independent filtering for large blockers and linear amplification for weak desired signals. The amount of suppression depends on the amplitude discrimination between the envelope of the large and small signal. The operation of the nonlinear receiver is based on the information of the interferer envelope amplitude.

A feedforward path is designed to extract the envelope information of the interferer and a feedback path is added to keep track of the environmental changes. With frequency independent filtering, the nonlinear receiver system achieves both good in-band and out-of-band linearity, thus enabling wideband multi-mode operation.

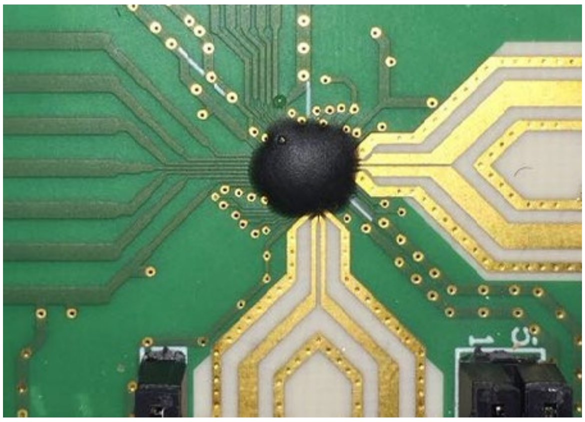


Fig.2: Final test chip on an evaluation board

Why Europractice?

Europractice's design kit services and organized MPW, mini@sic runs are crucial for a research with affordable access to state-of-art technology. The Europractice staff provides excellent service and information in each stage of the chip design process. Thanks for the support!

Acknowledgement

The authors acknowledge imec/Europractice IC service team for their high-quality support, the projects CORTIF, 3CCAR for the financial support.

Characterization of an Associative Memory Chip in 28 nm CMOS Technology

University of Milano and INFN Milano, Via Celoria 16, Milano, Italy (in collaboration with many other universities)

Main contact: Alberto Stabile (Universita degli Studi di Milano and INFN Milano)
Collaborators: Alberto Annovi, Giacomo Fedi, Fabrizio Palla (INFN Pisa)
Giovanni Calderini, Francesco Crescioli, Maroua Garci (LP-NHE Paris)
Stefano Capra, Luca Frontini, Valentino Liberali (Universita degli Studi di Milano and INFN Milano)
Bruno Checcucci (INFN Perugia)
Francesco De Canio (INFN Pavia)
Calliope-Louisa Sotiropoulou (Universita degli Studi di Pisa)
Gianluca Traversi (Universita degli Studi di Bergamo and INFN Pavia)
Christos Gentsos (Aristotle University of Thessaloniki)
Sebastien Viret (IPNL Lyon)
Takashi Kubota, Jafar Shojaii (University of Melbourne)
E-mail: alberto.stabile@unimi.it
Technology: TSMC N28 HPL
Die size: 1520 µm x 1520 µm

Introduction

A common challenge in the last decades is the fast and accurate handling of Big-Data. Specific cases of study are the High Energy Physics (HEP) experiments. In 2010 We started our research activity with the aim of designing an innovative device capable of accurately reconstruct the particle tracks. The Fast TracKer (FTK) is a dedicated electronics system being integrated in the ATLAS experiment [1] at the Large Hadron Collider (LHC) [2] at CERN for real-time reconstruction of all particle tracks with transverse momentum above a sufficient threshold produced in the proton-proton collisions [3]. The FTK system strongly enhances the capability of the online event selection system of the ATLAS experiment enabling the full exploitation of the physics capability of the LHC. The core of these Big-Data systems for the current FTK and of the future Hardware Tracker for the Trigger (HTT) [4] is a dedicated VLSI processor: the Associative Memory (AM) chip that provides highly-parallelized and fast pattern recognition.

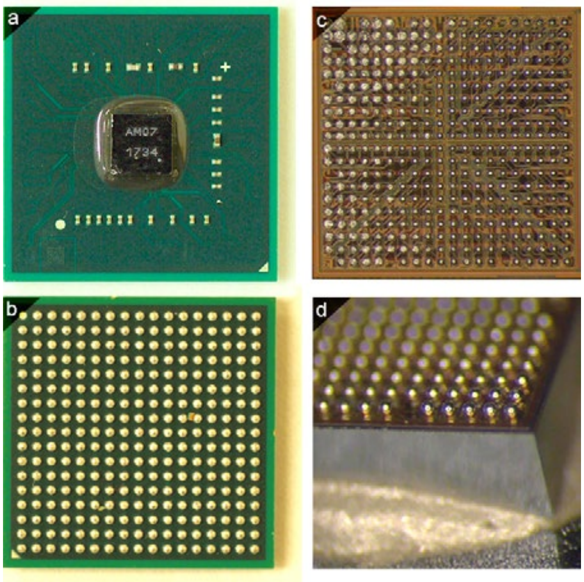


Fig. 1. Photograph of AM07: a) top face: die mounted on the ad-hoc BGA package ; b) bottom face: balls of the ad-hoc BGA package; c) top face: die bumps and RDL layer; d) bumps details.

The many prototypes designed, realized and tested, led to the realization of the first large volume chip in 2015: the AM06 chip [5]. The AM06 chip was manufactured in TSMC 65nm CMOS technology. In the next years, centre-of-mass energy and intensity of the proton-proton collisions of the LHC will be significantly upgraded. This strongly requires a next generation AMs with faster processing, lower power consumption and higher memory cell area density. The solution taken in 2015 includes the use of the advanced 28nm CMOS technology. In addition, an interesting feature of the chip presented in the paper is the capability to be compatible with the elaboration of data for other disciplines: AM07 will be used in the development of an integrated system for pattern recognition in the context of the image and DNA sequences analysis. The aim of AM07 is to guarantee the working functionality of two innovative designed memory cell technologies [6] at the clock frequency of 200 MHz to pioneer the design of the future AMs for the ATLAS and CMS experiments at the LHC, and all other DNA and image analysis applications that need to strongly improve pattern recognition performance.

Architecture of the designed circuit

AM07 counts 20 x 20 bumps and 17 x 17 balls. The die is flipped and mounted on the dedicate package substrate that re-route the signal and power from/to balls/bumps as shown in Figs. 1. The chip size is 1:520 µm x 1:520 µm pre-shrink that, at fabrication stage, will be 90% for each dimension.

The AM07 is organized in arrays of associative memory cells integrating two innovative custom design: DOXORAM and KOXORAM [6] based on the previous XORAM [7]. The measured power consumption of DOXORAM and KOXORAM are 30% and 75% less than AM06, respectively, and the silicon area decreased by a factor of (about) 4 with respect to the AM06 chip.

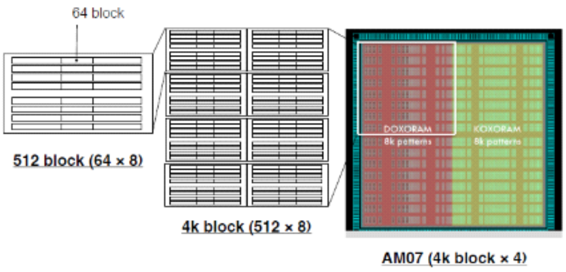


Fig. 2. Arrangement of the 16 kpatterns cell array.

Fig. 2 shows the hierarchy of memory banks: a word is composed by 18 bits; a pattern contains 8 words, and a bank of 16 kpatterns are organized in four 4k blocks (two DOXORAM blocks and two KOXORAM blocks). A 4k block consists of eight 512 blocks, each of which is made up of eight 64-word blocks. The array of the 64-word blocks is organized in 64 rows x 18 bits. The Bit-Lines (BLs) and the Search-Lines (SLs) are 18 bit double buses which connect a column of the memory array.

A. Comparison mode

SLs are used for finding correspondences of input data with pre-stored data. If a match is found in a block of 18 cells (a word block), the associated Set-Reset latch (SR) is flagged to '1', and the match pattern in a row is stored in a segment of eight flip-flops (8FF). For each word block, the Quorum logic counts the number of FF flagged to '1' and, if it exceeds a programmable threshold, the address of the row and the match pattern are read out. All these operations are performed in parallel.

B. Write mode

BLs are used to write cells (in the 'write mode'). Each pattern is connected by a Write-Line (WL). The on and off command of WLs is biased by external signals through demultiplexers.

C. Input data propagation

The input data are connected in parallel to each 4k block via the Double Data Rate (DDR) module. Data are propagated in parallel on the BLs and the SLs among the "12-blocks". The propagation could be stopped by means of an external control signal (STATE). The input data propagation could be also disabled in the DDR module. The AM07 chip can operate in the DDR data transfer mode. When the DDR mode is turned on, the input buses are sampled at the both edges of the input clock. Odd buses are propagated on the negative edges, and vice versa.

D. Clock domains and signal registering

Two external clocks are used: CLKI, for the input buses synchronization and CLKO for the output buses synchronization.

The full-custom memory arrays are clock-less and they are the interface between CLKI and CLKO. All inputs, controls and outputs signals are registered by means of Delay Flip Flops (DFFs) at the I/O interface. With the aim to smooth the VDD current peaks, one half of the input data are propagated among the chip on the positive edge of the CLKI, and one half on the negative edge.

Design flow and simulations

A mixed approach has been used: the memory arrays and analog IPs are designed with full-custom approach; the more complex (in terms of logic) modules are designed with Electronic Design Automation (EDA) tools.

Analog simulations with corner analysis have been used to validate the full-custom block. Cadence Tempus software has been used for static timing analysis, UVM and ncsim for backannotate digital simulations and Cadence Voltus for IR drop analysis.

Simulations with Tempus have been performed in three worst cases:

1. slow-slow library models, 0°C, 0.9V, working frequency: 150MHz;
2. fast-fast library models, 0°C, 1.1V, working frequency: 300MHz;
3. typical library models, 27/85°C, 1V, working frequency: 300MHz.

Fig. 3 shows the histograms of slack time, in which good timing margins are demonstrated. For all cases and simulations, results confirm that no negative slack time exists.

Voltus simulator has been used to performed IR drop analysis on the power wires. Standard cells containing Decoupling CAPacitors (DCAP) have been placed to reduce the IR drops. The estimated internal capacitance is 23 nF. The maximum IR drop is 64mV.

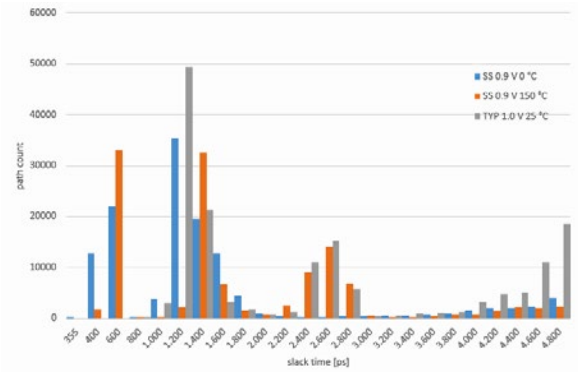


Fig. 3. Histograms of the slack time from a static timing analysis with Tempus in the three respective cases.

Characterization results

The chip has been characterized by means of a dedicated PCB (EDA-03625) mounting two Enclustra Mercury KX1, a low-jitter clock Generator (Si5380), a ZIF connector for the AM07, two Ethernet connector, a JTAG connector and some SMAs for fast lanes. Fig.4 shows the photography of characterization setup.

AM07 is characterized with different electric voltage conditions (Tab. I). Current consumption measurements have been done for the core part and I/O part, and are presented in the form of Shmoo plots.

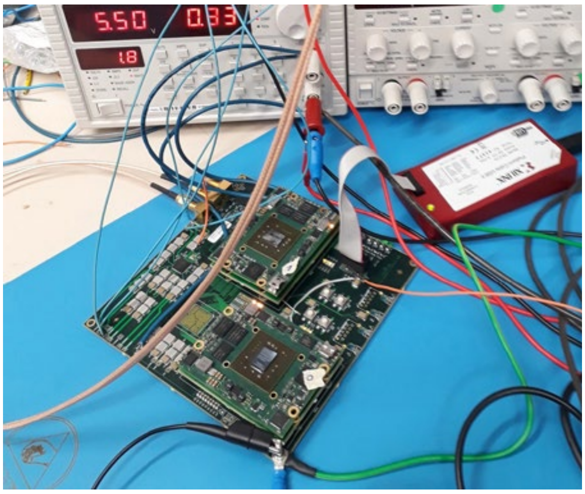


Fig. 4. Photography of the characterization setup at CERN.

I/O core supply [V] \ Core supply [V]	0.65	0.75	0.85	0.95	1.00	1.05	1.10
2.0	fail	fail	105	184	245	245	245
1.9	fail	fail	105	184	245	245	245
1.8	fail	fail	105	184	245	245	245
1.7	fail	fail	105	184	245	245	245
1.6	fail	fail	105	184	245	245	245
1.5	fail	fail	105	184	245	245	245
1.4	fail	fail	105	184	245	245	245

Table 1: SHMOO plot of functionality – values are the working frequency limit in mega hertz

Conclusion

The AM07 is a new Associative Memory chip designed in the 28nm TSMC HPL technology. The simulation and characterization results demonstrate that the chip is fully functional at 200 MHz. Respect to the AM06 chip, the power consumption of AM07 has been reduced by a factor 3 and the area occupation by a factor 2.9. We also report that the automatically designed blocks do not scale as the Moore's law. For this reason, in the future we will re-design the Quorum circuit with a full-custom approach. The power consumption and bandwidth capabilities of the entire chip will be also improved in the next chip.

Why Europractice?

AMchip team gratefully acknowledges Europractice for the support. We choose IMEC because is the unique channel in Europe to access the TSMC 28nm technology with reasonable prices for the research institutes.

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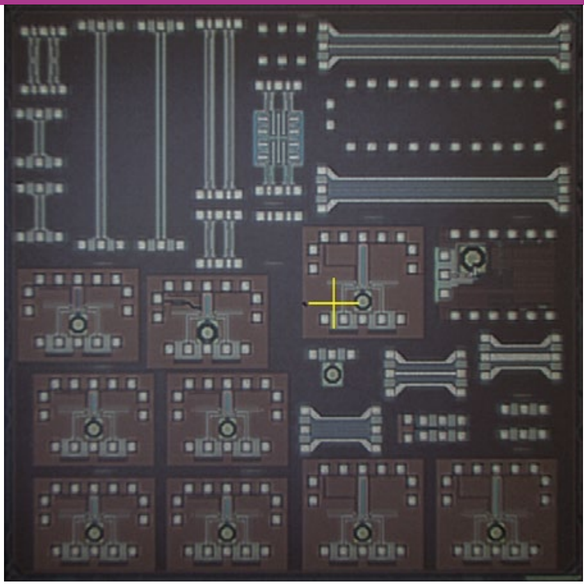

Fig. 1: Microscope picture taken from the Chartreuse chip fabricated in GLOBALFOUNDRIES 22FDX

CHARTREUSE chip – mm-wave Voltage Controlled Oscillator

Fraunhofer EMFT

Contact: David BORGGREVE
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Technology: GLOBALFOUNDRIES 22 nm FDSOI
Die size: 2600 x 2200 µm

Introduction

Low-power-electronic-circuits challenges are big for wireless telecommunication in Internet of Things (IoT) and Smart-X applications. The power consumption is critical for standalone systems, such as sensor monitoring and point-to-point communication. The 22-nm Fully Depleted Silicon On Isulator (FDSOI) technology from GLOBALFOUNDRIES aims to meet the requirements of emerging mobile, IoT and mm-wave RF applications. The back-gate-bias connection can improve the speed and the low power or the low leakage characteristics of the transistors. However, to date, the performance at mm-waves with this process is largely unknown.

Description

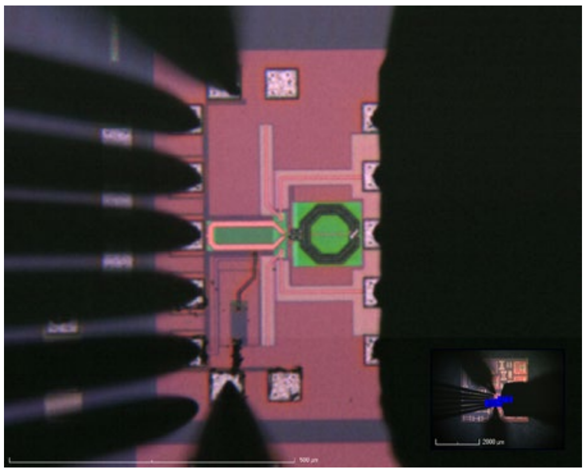
In the scope of the European Project WAYTOGO FAST, we develop the performance of one of the building blocks of an RF transceiver, the voltage controlled oscillator (VCO) at mm-wave frequencies with this FDSOI process. Sustainable oscillation at 80 GHz is possible with the help of an LC-tank and an nMOS cross-coupled pair. High-Q transmission lines are used to replace the on-chip inductor that has a low quality factor at the targeted operating frequency, suggesting an additional key improvement on the design. Higher quality factor means lower losses and hence smaller cross-coupled pair and lower power consumption.

The CHARTREUSE chip, which has been taped out with EUROPRACTICE on the 22FDX technology node from GLOBALFOUNDRIES, includes several variation of the VCOs and standalone active and passive elements. The passive elements, which are the transmission lines structures, provide useful information on the Back-End-Of-Line characteristics of the process and the active elements such as single transistor or varactor. These standalone elements characterizations are then compared with the simulations for PDK models verifications. The VCO exhibits a measured oscillation frequency at 68 GHz with an output power of approximatively 15 dBm, a phase noise of -72 dBc/Hz at 1 MHz offset and a power consumption of 5.3 mW. The main feature of the FDSOI technology is the use of the back-gate biasing, and for the VCO design, it lowers the total power consumption to a state-of-the-art value.

Why Europractice?

Europractice is a successful asset for the interface with GLOBALFOUNDRIES with the advanced 22nm FDSOI CMOS technology. As a research institute, Fraunhofer EMFT is able to use the expertise of Europractice for the customer support of the libraries installation, devices models, tools versions, and GDS delivery.

Fig. 2: Picture of the voltage controlled oscillator (VCO) under test.



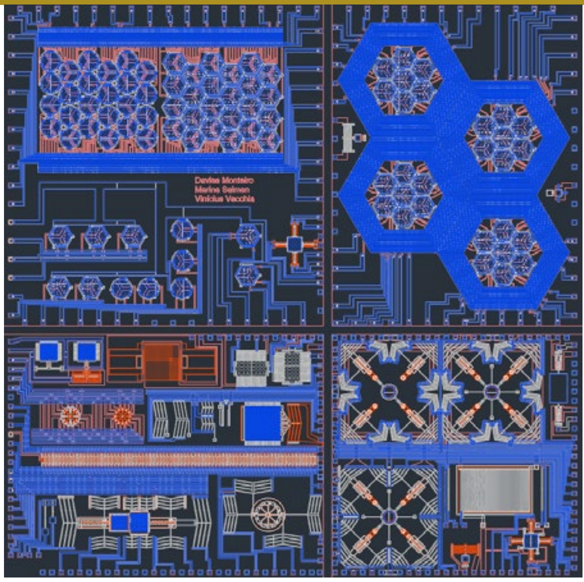


Figure 1 - Layout of the fabricated chip

Multiple stages of MEMS and MOEMS device developments using polyMUMPs

Federal University of Minas Gerais (UFMG), OptMAlab - Department of Electrical Engineering, Belo Horizonte, Brazil

Contact: Designers: Vinícius Vecchia, Marina Salmen
Supervisor: Prof. Dr. Davies William de Lima Monteiro
E-mail: davies@ufmg.br
Technology: MEMSCAP PolyMUMPs
Die size: 10 mm^2

Introduction

In this project several and MEMS MOEMS devices have been fabricated. Some are reproductions of well-known designs to serve as benchmarking. Another set of devices are modified versions of the latter aiming at an increase in performance. Yet a third set of structures are novel. The main reason for using PolyMUMPS was to shorten the time-to-prototype development and focus on the design aspects of the devices. Figure 1 shows the layout of the complete chip, that was subdiced into 4 smaller chips. Some of the devices implemented are accelerometers, flow sensors, tilting mirrors, diffraction gratings and several other types of actuators.

Description

Figure 2 shows a modified structure derived from a formerly tested structure [1]. It consists of an array of tilting hexagonal micromirrors, suspended by the residual force between the poly-Si layer and the metal layer on each one of the three arms. Tilting is accomplished by applying an electrical potential between the bottom electrodes and the top mirror surface. Several layouts have been fabricated, each with a different peripheral shape and metal distribution on their supporting arms.

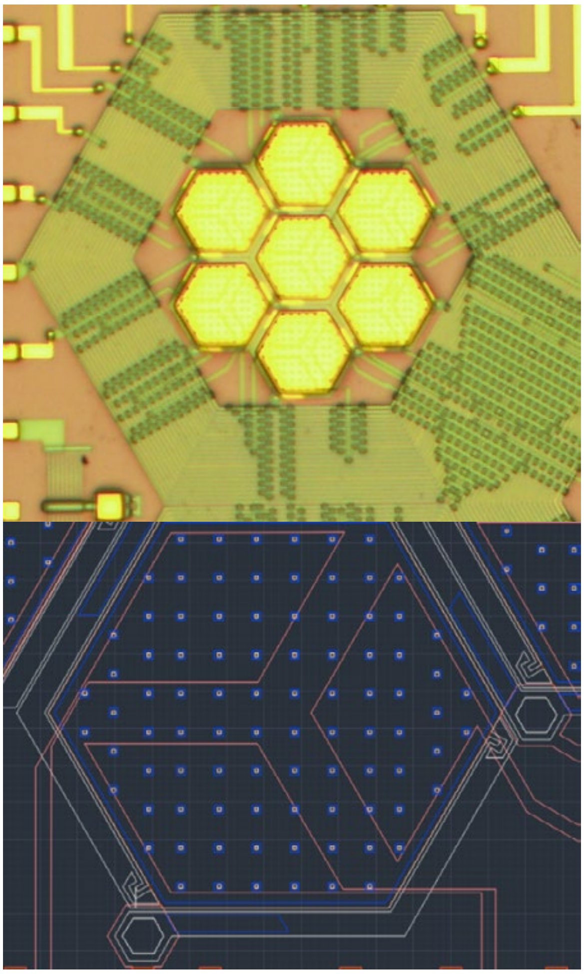


Figure 2 – Photography of the array consisting of seven tilting micromirrors (top). Layout view of a single tilting micromirror, showing the three diamond shaped electrodes (bottom).

Figure 3 depicts one of the novel designs implemented. This device consists of two juxtaposing square arrays of long metal coated fingers that can be stacked and aligned in or out of phase in relation to each other, thus implementing a variable diffraction grating.

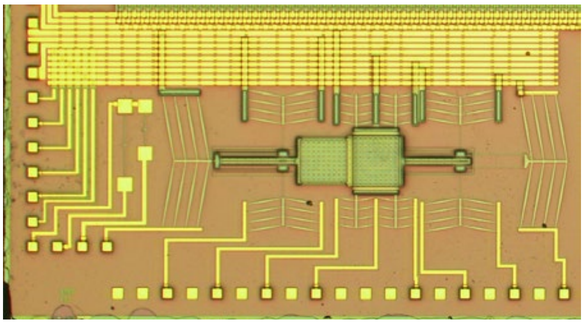


Figure 3- Overall view of the diffraction grating

As the PolyMUMPS process allows only metal to be deposited on the top movable poly-Si layer, both arrays must be fabricated using the same layer and some assembling is required to first operate the device and stack the metal layers. This assembly is done by driving the Chevron actuators connected to the linear rack [2]. Additional Chevron actuators are required to serve as a clutch mechanism. This device stands out among most of the MEMS diffraction grating already described in the literature by having the possibility to tune the gap between two adjacent fingers from 3 µm to, theoretically, zero [3]. The implemented device has approximately 300x300 µm of optical usable area.

Why Europractice?

Europractice enables professors, students and academic staff to easily prototype integrated circuits and MEMS devices in a short period of time. Also, Europractice staff offers excellent technical support regarding technology PDK and general guidance regarding the design of the devices.

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PiezoMUMPS devices for sensing, actuation and energy harvesting

Federal University of Minas Gerais (UFMG), OptMAlab - Department of Electrical Engineering

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E-mail: davies@ufmg.br; facdo@hotmail.com
Support: FAPEMIG, CNPq and CAPES
Technology: MEMSCAP PiezoMUMPs
Die size: 11.15 x 11.15 mm

Introduction

A piezoelectric MEMS chip containing several different structures comprising of sensors, filters, resonators and energy harvesters was designed at OptMAlab of the Federal Univeristy of Minas Gerais (UFMG). The chip has been successfully fabricated and is currently under test.

Chip description

The full chip with 11.15 x11.15 mm^2 (but having only the central 9 x 9 mm available for la yout) was LASER sub-diced into four different sub-dies. The chip contains a total of 42 different structures, most of them falling into one of the following categories: cantilever, bridge, surface acoustic wave device (SAW), ring resonator, membrane and double anchored spiral. The chip layout is shown in figure 1 and figure 2 shows a picture of the fabricated chip.

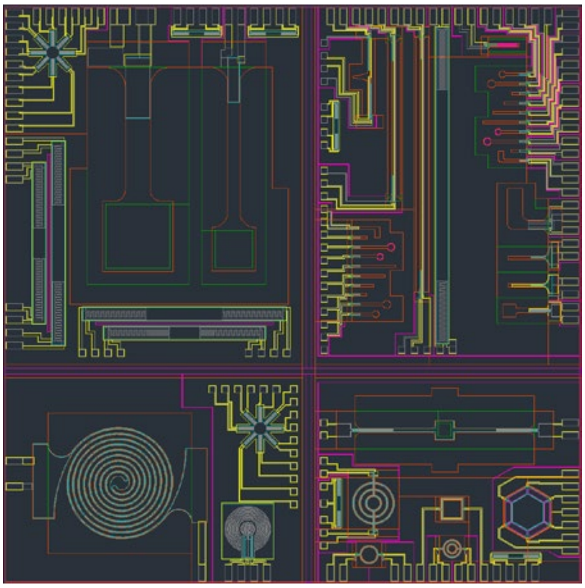


Fig. 1. Full chip layout.

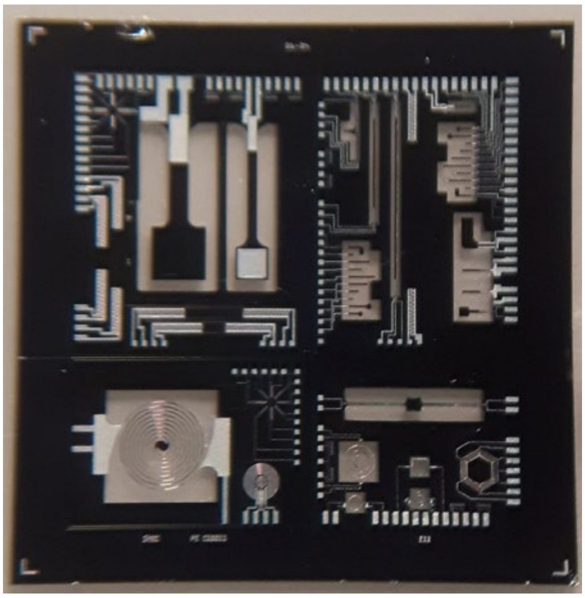


Fig. 2. Full chip photograph.

Chip functionality and Results

There were several applications envisioned for the proposed structures and several types of cantilevers, with resonant frequencies ranging from 160 Hz up to hundreds of kHz were fabricated. The SAW devices can be used for high-Q band-pass filter featuring frequency up to 1 GHz. An innovative ring resonator structure was developed, with inner rings that resonate in different frequencies that could be used as multi-band pass filters. The double anchored spiral was simulated with finite element analysis software and the results showed a low frequency resonance and a high sensitivity, having a potential application for ambient vibration sensing. Most of the bridge structures can also be magnetically actuated, by passing an alternating current and using an external magnetic field, having also piezoelectric sensing capabilities and the potential for measuring fluid parameters. A more in-depth study was made for the two largest cantilevers that have a tip mass for increased sensitivity to ambient vibrations and lower resonant frequency. Those structures can be used for vibrational energy harvesting and a few experiments were conducted showing promising results for this application. The bigger cantilever was mechanically excited by a loud speaker, in the measured resonance frequency of 162 Hz and the vibration intensity was measured with an accelerometer, being slightly under 1 g. A variable resistive load was connected to the cantilever and the generated voltage/power was measured as a function of load. Figure 3 shows the obtained results.

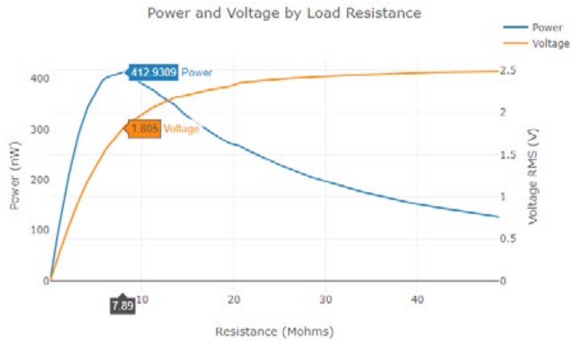


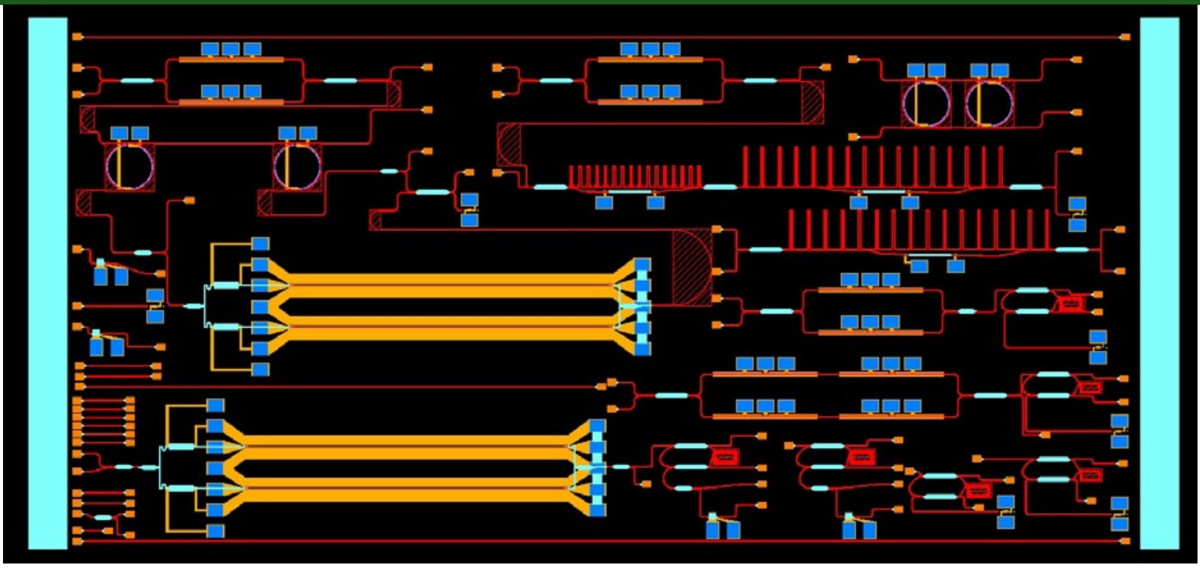
Fig. 3. Measured voltage and power as a function of resistive load.

Why Europractice?

It enables the easy prototyping of MEMS devices in a short period of time, with ready and competent technical support regarding the technology design kits, interface with the manufacturers and useful tips during the design phase.

Acknowledgements

The authors would like to thank FAPEMIG, CNPq and CAPES for their support.



Silicon photonic integrated circuit for energy-efficient millimeter-wave generation

Department of Engineering, Aarhus University, Denmark

Contact: Martijn Heck
E-mail: mheck@eng.au.dk
Technology: ISIPP50G – IMEC Si-Photonics (Active platform)
Die size: 5.15 mm x 2.5 mm

Fig. 1. Layout view of the submitted design in the ISIPP50G technology

Description

Signal generation at higher frequencies, e.g., millimeter-waves for future 5G wireless communication systems, becomes increasingly energy-inefficient for increasing frequency, when electronic solutions are used. Moreover, we are seeing a fiber-wireless convergence, which will favor the transport and processing of such millimeter-wave signals on an optical carrier. This field is called microwave photonics.

Traditionally, photonic systems tended to be bulky, made out of discrete components. Photonic integration offers a path to reduce the footprint, cost and energy consumption of such systems dramatically. Photonic integration is currently widely used commercially for telecommunications and data communications, using material platforms like indium phosphide and silicon. Its use for microwave photonic applications, such as millimeter-wave generation, is currently a topic of very active research.

The ISIPP50G process of imec was used to design and realize a silicon photonic integrated circuit for millimeter-wave generation. In this approach, an external laser is coupled into the circuit and then modulated. The modulator is driven by and external microwave oscillator, at a relatively low frequency, to ensure maximum energy-efficiency of the application.

When the laser light gets modulated, a comb of optical frequencies is created, separated by a frequency spacing equal to the driving oscillator frequency. On the silicon photonic circuit, optical filters then select two of these comb lines, with an integer multiple spacing of the driving frequency. These comb lines are then combined into a single waveguide, creating a beat signal on top of the optical carrier. This light is coupled into an on-chip photodiode, which detects this beat signal and creates an equivalent photocurrent. This can then, e.g., be coupled to an antenna.

In summary, the silicon photonic integrated circuit can multiply microwave input frequencies with a discrete, even factor. In effect it acts like a frequency doubler, quadrupler, etc. Initial feasibility studies show that an integrated microwave photonic approach can be more energy-efficient than a pure electronic approach. Experimental results are ongoing.

Why Europractice?

The photonic integrated circuits group at Aarhus University takes a fabless approach. We rely on foundries to fabricate our designs. This means we can focus on the circuit design, rather than the physical design. In our opinion, that is the only path forward to push photonic integration to higher integration levels, and to applications that will truly benefit the society.

The ISIPP50G process offers the high-bandwidth components that allow us to work on applications in the millimeter-wave range, for future 5G communication systems.

Acknowledgements

We acknowledge support from the Danish Det Frie Forskningsråd under grant number DFF – 4005-00246.

EUROPRACTICE MEMBERSHIP

The funding requested from the EC is far from sufficient to offer the EUROPRACTICE high quality service to >600 European universities and research institutes. Membership Fees pay for extra staff supporting this requested stimulation activity for academic institutions (not fully paid by the EU). The annual Membership Fee is collected by STFC on behalf of the EUROPRACTICE project partners.

European universities and research institutes can choose from 3 different levels of membership:

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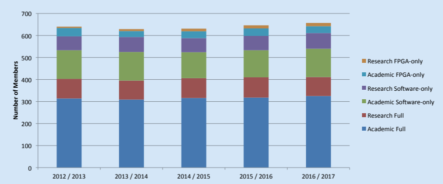
The academic user base is averaging around 625 institutes in ~42 countries of Europe, Middle East, Africa and Russia .



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A47630	Belarusian State University of Informatics and Radioelectronics
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Cyprus

A07090	University of Cyprus

Czech Republic

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A40070	Vysoke uceni technicke v Brne
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R49000	Ustav teorie informace a automatizace AV CR

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A14670	Cairo University
A15090	The German University in Cairo
A15160	The American University in Cairo
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A16020	Zewail City of Science & Technology

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Finland

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A13260	École Nationale Supérieure de Mécanique et des Microtechniques
A13800	Université de Lorraine
A14410	École des Hautes Etudes d'Ingénieur
A14440	Laboratoire de Physique Corpusculaire de Caen
A15600	Université Pierre et Marie Curie - Institut de la Vision
A35020	Université Pierre et Marie Curie - L2E
A35290	Université de Montpellier 2
A35370	École Nationale Supérieure de l'Electronique et de ses Applications
A35800	Institut Supérieur d'Electronique et du Numérique
A36061	Centre Interuniversitaire de Microélecronique et de Nanotechnologies
A36311	Institut National des Sciences Appliquées de Lyon
A36312	École Supérieure de Chimie Physique Électronique de Lyon
A36410	Atelier Interuniversitaire de Microélecronique
A37470	Université de Strasbourg
A37590	Aix Marseille Université
A37670	Laboratoire de Physique Nucléaire et de Hautes Energies
A37710	IMT Atlantique Bretagne-Pays de la Loire
A37950	Université Claude Bernard Lyon 1
A37980	Université Joseph Fourier
A39060	Laboratoire d'Annecy-le-Vieux de physique des particules
A39400	Université Clermont Auvergne
R00210	Laboratoire d'Analyse et d'Architectures des Systèmes
R14140	Laboratoire des sciences de l'ingénieur, de l'informatique et de l'imagerie
R15140	XLIM Université de Limoges
R20490	European Synchrotron Radiation Facility
R20810	Station de Radioastronomie de Nançay, Observatoire de Paris
R20980	Laboratoire des Plasmas et de Conversion d'Energie
R21010	Laboratoire de Physique et Chimie de l'Environnement et de l'Espace
R21020	Synchrotron SOLEIL
R21030	Institut Matériaux Microélectronique Nanosciences de Provence
R21140	Institut Laue-Langevin
R21170	Laboratoire de l'Accélérateur Linéaire
R21270	Commissariat à l'énergie atomique et aux énergies alternatives - IRFU
R21290	Spintronique et Technologie des Composants
R21380	Laboratoire de Physique des Plasmas
R21410	Laboratoire Leprince-Ringuet
R21420	Office National d'Études et de Recherches Aérospatiales - Châtillon
R21560	Office National d'Études et de Recherches Aérospatiales - Toulouse
R21960	Institut de recherche en astrophysique et planétologie
R22060	Institut d'Astrophysique Spatiale
R22130	Observatoire de Paris - LESIA
R22190	Laboratoire des Sciences de L'Information et des Sciences
R22210	Centre de Microélectronique OMEGA
R22220	Commissariat à l'énergie atomique et aux énergies alternatives - LETI DACLE
R22240	Le Laboratoire PROcédés, Matériaux et Énergie Solaire
R22280	Institut de Recherche sur les Composants logiciels et matériels pour l'Information et la Communication Avancée
R22310	Grand Accélérateur National d'Ions Lourds
R22360	Institut de Recherche et Technologie Antoine de Saint Expupéry
R22380	Laboratoire de Génie Electrique et Electronique de Paris
R37850	Laboratoire de l'Accélérateur Linéaire
R38290	Laboratoire de l'Intégration du Matérieu au Système

Germany

A00110	Johannes Gutenberg Universität Mainz
A00240	Fachhochschule Köln
A00510	Hochschule Konstanz für Technik, Wirtschaft und Gestaltung
A00670	Hochschule Bremen
A00850	Justus Liebig-Universität Gießen
A12140	Technische Universität München - Fakultät für Physik (Garching)
A12270	Hochschule Albstadt-Sigmaringen
A12410	Fachhochschule Schmalkalden
A12440	Hochschule Pforzheim
A12540	Brandenburgische Technische Universität Cottbus
A12840	Bergische Universität Wuppertal
A13060	Albert-Ludwigs-Universität Freiburg - IMTEK
A13610	Fachhochschule Aachen

A13650	Technische Universität Darmstadt - Institut für Halbleitertechnik und Nanoelektronik (IHT)
A13660	Universität Bremen - Informatik
A13680	Hochschule Aschaffenburg
A13880	Hochschule für Technik und Wirtschaft des Saarlandes
A13890	Technische Universität Berlin - Institut für Technische Informatik und Mikroelektronik (TIME)
A14130	Fachhochschule Brandenburg
A14310	Universität Kassel - Fachbereich Elektrotechnik/Informatik
A14740	Universität Kassel
A14920	Universität Konstanz
A15030	Universität Bielefeld
A15230	Hochschule für Angewandte Wissenschaften Hamburg
A15330	Carl von Ossietzky Universität Oldenburg - Energie und Halbleiterforschung (EHF)
A15410	Technische Hochschule Mittelhessen - Friedberg
A15500	Hochschule RheinMain
A15840	Hochschule Rosenheim
A15930	Fachhochschule Südwestfalen
A15950	Beuth Hochschule für Technik Berlin
A16030	Rheinisch-Westfälische Technische Hochschule Aachen - Lehrstuhl für Integrierte Photonik (IPH)
A16040	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Stromrichtertechnik und Elektrische Antriebe (ISEA)
A16060	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Theoretische Elektrotechnik (ITHE)
A16090	Westfälische Hochschule
A16100	Hochschule fuer Technik und Wirtschaft Berlin (HTW Berlin)
A16310	Technische Universität Bergakademie Freiberg
A16320	RWTH Aachen, Physikalisches Institut B
A35320	Technische Universität Hamburg-Harburg
A35400	Hochschule Ulm
A35420	Georg-Simon-Ohm Hochschule Nürnberg
A35430	Karlsruher Institut für Technologie
A35450	Technische Universität Darmstadt - Integrierte Elektronische Systeme (IES)
A35500	Eberhard Karls Universität Tübingen
A35590	Johannes-Wolfgang-Goethe-Universität Frankfurt am Main
A35600	Technische Universität Braunschweig
A35620	Universität Bremen - Institut für Theoretische Elektrotechnik und Mikroelektronik
A35640	Rheinisch-Westfälische Technische Hochschule Aachen - Institute for Communication Technologies and Embedded Systems (ICE)
A35710	Hochschule Augsburg
A35810	Technische Universität Kaiserslautern
A35830	Universität Hamburg
A35990	Universität Duisburg-Essen
A36070	Carl von Ossietzky Universität Oldenburg - Informatik
A36440	Universität des Saarlandes
A37090	Technische Universität Dortmund
A37240	Hochschule Furtwangen
A37290	Leibniz Universität Hannover
A37310	Technische Universität Berlin
A37380	Friedrich-Alexander-Universität Erlangen-Nürnberg
A37390	Technische Universität München - Fakultät für Elektrotechnik und Informationstechnik München
A37440	Universität der Bundeswehr München
A37450	Hochschule Esslingen
A37500	Universität Paderborn
A37510	Hochschule für Angewandte Wissenschaften München
A37530	Humboldt-Universität zu Berlin
A37540	Universität Ulm
A37760	Technische Universität Dresden
A37800	Hochschule Offenburg

A37810	Rheinisch-Westfälische Technische Hochschule Aachen - Fakultät für Elektrotechnik und Informationstechnik
A37880	Hochschule Aalen
A37920	Hochschule Ravensburg-Weingarten
A37930	Hochschule Mannheim
A38010	Hochschule Heilbronn
A38030	Hochschule Darmstadt
A38080	Ruhr-Universität Bochum
A38090	Otto-von-Guericke-Universität Magdeburg
A38220	Universität Siegen
A38240	Technische Universität Ilmenau
A38340	Technische Universität Chemnitz
A38390	Ruprecht-Karls-Universität Heidelberg - Mannheim
A38550	Ostfalia Hochschule für angewandte Wissenschaften
A38650	Fachhochschule Dortmund
A38890	Rheinische Friedrich-Wilhelms-Universität Bonn
A38940	Ernst-Abbe-Fachhochschule Jena
A39000	Technische Hochschule Mittelhessen - Gießen
A39110	Universität Stuttgart
A39220	Universität Rostock
A39250	Ruprecht-Karls-Universität Heidelberg - Heidelberg
A39260	Albert-Ludwigs-Universität Freiburg
A39320	Jade Hochschule
A39330	Hochschule Reutlingen
A39340	Martin-Luther-Universität Halle-Wittenberg
A39460	Christian-Albrechts-Universität zu Kiel
A39580	Hochschule Osnabrück
A39660	Friedrich-Schiller-Universität Jena
A39770	Universität zu Lübeck
R00150	Max-Planck-Institut für Physik
R20300	Institut für Mikroelektronik- und Mechatronik - Systeme gemeinnützige GmbH
R20330	Deutsches Elektronen-Synchrotron
R20460	Institut für Mobil- und Satellitenfunktechnik GmbH
R20510	IHP GmbH - Leibniz-Institut für innovative Mikroelektronik
R20720	Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und -Systeme
R20880	GSI Helmholtzzentrum für Schwerionenforschung GmbH
R20890	Fraunhofer-Institut für Siliziumtechnologie
R20900	Fraunhofer-Institut für Biomedizinische Technik
R20920	Fraunhofer-Institut für Integrierte Schaltungen - Erlangen
R20930	Fraunhofer-Institut für Integrierte Schaltungen - Dreden
R21050	Max-Planck-Institut für Chemie
R21060	Forschungszentrum Jülich
R21090	Fraunhofer Heinrich-Hertz-Institut
R21120	Max-Planck-Institut für extraterrestrische Physik
R21150	Physikalisch-Technische Bundesanstalt - Braunschweig
R21220	Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie
R21260	Hochschule für Technik und Wirtschaft Dresden
R21310	Fraunhofer-Institut für Photonische Mikrosysteme
R21320	Fraunhofer-Institut für Solare Energiesysteme
R21510	Deutsches Zentrum für Luft- und Raumfahrt - Berlin
R21530	Deutsches Zentrum für Luft- und Raumfahrt - Bremen
R21540	Max-Planck-Institut für biophysikalische Chemie
R21580	Deutsches Zentrum für Luft- und Raumfahrt IIP - Berlin
R21610	Helmholtz-Zentrum Berlin für Materialien und Energie
R21620	Fraunhofer-Einrichtung für Angewandte und Integrierte Sicherheit
R21630	Fraunhofer-Institut für Zerstörungsfreie Prüfverfahren
R21650	Fraunhofer-Institut für Hochfrequenzphysik und Radartechnik
R21660	Fraunhofer-Einrichtung für Systeme der Kommunikationstechnik
R21770	Konrad-Zuse-Zentrum für Informationstechnik Berlin
R21780	Deutsches Zentrum für Luft- und Raumfahrt - Wessling

R21790	NaMLab gGmbH
R21860	DLR-Institut für Vernetzte Energiesysteme e.V.
R21900	Max-Planck-Institut für Radioastronomie
R21970	PNSensor gGmbH
R22020	European XFEL
R22080	Fraunhofer COMEDD
R22110	Physikalisch-Technische Bundesanstalt - Berlin
R22150	Fraunhofer Institute SIT
R22160	Halbleiterlabor der Max Planck Gesellschaft
R22260	Helmholtz-Zentrum Geesthact
R22290	Fraunhofer-Einrichtung für Mikrosysteme und Festkörper-Technologien EMFT
R22300	Max-Planck-Institut für Informatik
R22340	Optotransmitter-Umweltschutz-Technologie e.V
R22370	CIS Forschungsinstitut fuer Mikrosensorik GmbH
R22420	Paul-Drude-Institut für Festkörperelektronik
R22440	Hahn-Schickard-Gesellschaft fuer Angewandte Forschung e.V.

Ghana

A14770	Kwame Nkrumah University of Science & Technology

Greece

A00530	University of Ioannina
A12451	Technological Educational Institute of Crete
A13550	University of Thessaly
A13690	Technological Educational Institute Stereas Elladas
A14150	Athens University of Economics and Business
A14340	University of the Peloponnese
A14700	University of Piraeus
A15110	Technological Educational Institute of Western Macedonia
A35140	National Technical University of Athens
A35960	University of Patras - Electrical and Computer Engineering
A37550	National and Kapodistrian University of Athens
A37680	University of Patras
A39280	Aristotle University of Thessaloniki
A39490	Technical University of Crete
R20790	Demokritos, National Center for Scientific Research
R21080	Foundation for Research and Technology Hellas

Hungary

A40010	Budapesti Muszaki és Gazdaságtudományi Egyetem
A47540	Pázmány Péter Katolikus Egyetem
R22230	Magyar Tudományos Akadémia ATOMKI

Ireland

A01190	Cork Institute of Technology
A13410	Institute of Technology, Carlow
A15730	University College Dublin
A35300	University College Cork
A36490	Trinity College Dublin
A36510	University of Limerick
A39310	Institute of Technology, Tallaght
R21720	Tyndall National Institute
R22400	Dublin Institute for Advanced Studies

Israel

A13330	Technion - Israel Institute of Technology
A13910	Ben-Gurion University of the Negev
A13920	Bar-Ilan University
A14070	Ort Braude College of Engineering
A14380	Tel-Aviv University
A14540	Kinneret College on the Sea of Galilee
A14690	Holon Institute of Technology
A15190	Jerusalem College of Technology

Italy

A00120	Università Politecnica delle Marche
A00520	Università degli Studi di Modena e Reggio Emilia - Modena
A00560	Università degli Studi di Siena
A00680	Università della Calabria
A00740	Università degli Studi di Perugia
A12000	Università di Bologna - DEIS
A12370	Università degli Studi di Napoli Federico II - DIETI
A12390	Università degli Studi di Brescia
A12430	Università degli Studi Mediterranea di Reggio Calabria
A12530	Università degli Studi di Verona
A12640	Università degli Studi di Milano
A12770	Università del Salento
A12990	Università degli Studi di Bergamo
A13280	Università degli Studi di Udine
A14020	Università degli studi di Napoli Federico II - Dipartimento di Fisica
A14220	Università degli Studi di Trento
A14800	Università degli Studi di Milano-Bicocca
A14820	Università degli Studi di Salerno
A14860	Università degli Studi di Modena e Reggio Emilia - Reggio Emilia
A15070	Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna
A15750	Università Degli Studi di Cassino e del Lazio Meridionale
A15900	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Cesena)
A16130	Università degli Studi Roma Tre
A35210	Università degli Studi di Parma
A35530	Politecnico di Torino
A35660	Università di Pisa
A35690	Politecnico di Milano
A35910	Università degli Studi di Genova
A36380	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Bologna)
A37280	Università degli Studi di Pavia
A37460	Università degli Studi di Catania
A37520	Università degli Studi di Ferrara
A38380	Politecnico di Bari
A38620	Università degli Studi di Torino
A38840	Università degli Studi di Roma "La Sapienza"
A39200	Università degli Studi di Padova
A39410	Università degli Studi dell'Aquila
A39550	Università degli Studi di Firenze
A39570	Università degli Studi di Cagliari
R00140	Fondazione Bruno Kessler
R00270	Istituto Nazionale di Fisica Nucleare, Sezione di Genova
R00300	Istituto Nazionale di Fisica Nucleare, Sezione di Pisa
R20310	Istituto Nazionale di Fisica Nucleare, Sezione di Roma
R20320	Istituto Nazionale di Fisica Nucleare, Sezione di Roma II
R20400	Istituto Nazionale di Fisica Nucleare, Sezione di Bologna
R20420	Istituto Nazionale di Fisica Nucleare, Sezione di Trieste
R20440	Istituto Nazionale di Fisica Nucleare, Sezione di Torino
R20450	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali di Frascati
R20470	Istituto Nazionale di Fisica Nucleare, Sezione di Padova
R20550	Elettra-Sincrotrone Trieste
R20560	Istituto Nazionale di Fisica Nucleare, Sezione di Roma III
R20580	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali di Legnaro
R20630	Istituto Nazionale di Fisica Nucleare, Sezione di Milano
R20670	Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari
R20710	Istituto Nazionale di Fisica Nucleare, Sezione di Bari
R20990	Istituto Nazionale di Fisica Nucleare, Sezione di Ferrara
R21100	Istituto Nazionale di Fisica Nucleare, Sezione di Napoli

R21160	Istituto Nazionale di Astrofisica, Osservatorio Astrofisico di Arcetri
R21190	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali del Gran Sasso
R21300	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi
R21450	Istituto Nazionale di Fisica Nucleare, Sezione di Pavia
R21570	Istituto Nazionale di Astrofisica, Istituto di Radioastronomia
R21600	Istituto Italiano di Technologia
R21800	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi Roma
R21940	The Abdus Salam International Centre for Theoretical Physics
R22010	Istituto Nazionale di Astrofisica Osservatorio Astronomico di Cagliari
R22040	Istituto Nazionale di Astrofisica - IASF, Milano
R22070	Instituto per lo Studio dei Materiali Nanostrutturati
R22120	Istituto Nazionale di Astrofisica - Istituto di Radioastronomia - Radiotelescopi di Medicina
R22200	Radio Analog Micro Electronics srl
R22390	Instituto Nazionale di Fisica Nucleare Sezione di Perugia
R22410	Instituto Nazionale di Fisica Nucleare Sezione di Catania
R22450	European Gravitational Observatory

Jordan

A15990	Princess Sumaya University for Technology
A16080	Yarmouk University
A16140	Jordan University of Science & Technology

Kazakhstan

A48080	Nazarbayev University

Lebanon

A15720	Lebanese American University
A47650	American University of Beirut

Lithuania

A40230	Kauno Technologijos Universitetas
A47980	Vilniaus Universitetas
A48050	Vilniaus Gedimino Technikos Universitetas

Luxembourg

A15780	Université du Luxembourg

Malta

A38720	University of Malta

Norway

A12750	Høgskolen i Sørøst-Norge
A13580	Norges teknisk-naturvitenskapelige universitet - Institutt for datateknologi og informatikk
A37360	Universitetet i Oslo
A37560	Norges Teknisk Naturvitenskapelige Universitet - Institutt for elektroniske systemer
A37820	Universitetet i Bergen
R21460	SINTEF Stiftelsen for industriell og teknisk forskning

Palestine

A16240	Birzeit University

Poland

A40100	Uniwersytet Zielonogórski
A40120	Politechnika Warszawska
A40130	Politechnika Lódzka - Mikroelektroniki I Technik Informatycznych (DMCS)
A40140	Akademia Górniczo-Hutnicza im. Stanislawa Staszica
A40150	Instytut Fizyki Jadrowej im. Henryka Niewodniczanskiego
A40160	Politechnika Wroclawska
A40530	Politechnika Slaska
A47300	Politechnika Gdanska
A47400	Politechnika Poznanska - Inzynierii Komputerowej
A47580	Wojskowej Akademii Technicznej
A47670	Politechnika Poznanska - Radiokomunikacji
A47740	Politechnika Lódzka - Pólprzewodnikowych I Optoelektronicznych
A47940	Politechnika Lubelska
R40030	Instytut Technologii Elektronowej
R49030	Instytut Podstawowych Problemów Techniki PAN (IPPT-PAN)
R49050	Bioinfobank Institute
R49080	Centrum Badan Kosmicznych PAN
R49100	Norodowe Centrum Badan Jadrowych

Portugal

A12310	Universidade Nova de Lisboa
A12550	Universidade do Minho
A13710	Instituto Superior de Engenharia de Lisboa
A35540	Universidade do Porto
A35670	Universidade de Aveiro
A35970	Instituto Superior Técnico
A37230	Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento
R14120	Instituto de Telecomunicações - Lisboa
R21710	Laboratório de Instrumentação e Física Experimental de Partículas
R21750	International Iberian Nanotechnology Laboratory
R21890	Instituto de Telecomunicações - Aveiro
R22170	Instituto de Sistemas Robótica (ISR-UC)

Romania

A15520	Universitatea Politehnica din Bucuresti
A16070	Universitatea Transilvania Brasov
A48070	Universitatea Tehnica din Cluj-Napoca
R49010	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Nuclear Hadrons
R49060	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Particle Physics

Russia

A40240	Vladimir State Technical University named after Alexander and Nikolay Stoletovs
A47330	St. Petersburg State Polytechnical University
A47520	National Research University of Electronic Technology (MIET)
A47790	St. Petersburg State University of Aerospace Instrumentation
A47810	Lomonosov Moscow State University
A47850	Moscow Institute of Physics & Technology (MIPT) - Wireless Technologies
A47990	St. Petersburg Electrotechnical University 'LETI'
A48030	Omsk State Technical University
A48040	Moscow Institute of Physics & Technology (MIPT) - Control Systems
A48110	Far Eastern State Transport University
A60020	State University-Education-Science-Production Complex
A60030	Tomsk State University
A60040	Tomsk State University of Control Systems and Radioelectronics
A60060	Mordovian State University named after N.P.Ogarev
A60080	Novosibirsk State Technical University
A60100	Moscow State Institute of Electronics and Mathematics (Technical University)
A60110	National Research Nuclear University MEPHI
A60140	MV Lomonosov Moscow State University
A60150	Moscow Institute of Physics & Technology (MIPT) - Cybernetics
A60160	Bauman Moscow State Technical University - Kaluga

A60170	Moscow State Technical University of Radioengineering, Electronics and Automation
A60190	Bauman Moscow State Technical University - Moscow
A60200	Rzhanov Institute of Semiconductors Physics
A60220	Voronezh State Academy of Forestry Engineering
A60230	Samara National Research University (Samara University)
A60240	National University of Science & Technology 'MISiS'
R21930	Scientific Manufacturing Complex "Technological Centre" MIET (SMCTC)
R47900	Budker Institute of Nuclear Physics
R49070	Space Research Institute (IKI)

Serbia

A47510	Univerzitet u Nišu
A47600	Univerzitet u Novom Sadu
A48010	Univerzitet u Beogradu

Slovakia

A40050	Slovenská technická univerzita v Bratislave
A47930	Technická univerzita v Kosiciach

Slovenia

A40280	Univerza v Ljubljani
A47690	Institut "Jožef Stefan"
A47820	Univerza v Mariboru

South Africa

A14560	University of Pretoria

Spain

A12320	Universidad Politécnica de Cartagena
A12470	Universidad Rey Juan Carlos
A12590	Universidad de Castilla - La Mancha
A13150	Universitat de València
A13340	Universidad de Alcalá
A13860	Universidad de Salamanca
A14720	Universidad de La Laguna
A15100	Universitat Politècnica de Catalunya - Manresa
A15370	Universidad de Deusto
A16290	Universitat Pompeu Fabra
A35130	Universidad Politécnica de Madrid - Departamento de Ingeniería Electrónica
A35190	Universitat Politècnica de València
A35870	Universidad de Sevilla - Instituto de Microelectrónica de Sevilla (IMSE-CNM)
A35891	Universidad de Cantabria
A36250	Universitat Autònoma de Barcelona
A36390	Universidad de Las Palmas de Gran Canaria - Instituto Universitario de Microelectrónica Aplicada (IUMA)
A37060	Universidad de Zaragoza - Dpto.Ingenieria Electronica y Comunicaciones
A37080	Universidad de Santiago de Compostela
A37330	Universidad Complutense de Madrid
A37580	Universidad de Malaga
A37690	Universidad del Pais Vasco
A38330	Universidad de Vigo
A38360	Universitat de les Illes Balears
A38580	Universidad de Sevilla - Ingenieria Electronica
A38590	Universidad de Granada
A38600	Universidad de Navarra
A38660	Universitat de Barcelona
A38780	Universidad de Las Palmas de Gran Canaria - Departamento de Informàtica y Sistemas
A38790	Universidad de Zaragoza - Facultad de Ciencias
A38820	Universidad Politécnica de Madrid - Centro de Electrónica Industrial
A39080	Universidad de Extremadura
A39100	Universidad Pública de Navarra
A39150	Universitat Politècnica de Catalunya - Departamento de Ingeniería Electrónica (Campus Nord)
A39180	Universitat Rovira i Virgili
A39300	Escola Universitàta Salesiana de Sarrià
A39390	Universitat Autónoma de Madrid
A39540	Universidad Carlos III de Madrid
R00060	CNM - Instituto de Microelectrónica de Barcelona
R20700	Ikerlan
R20850	Centre Tecnològic de Telecomunicacions de Catalunya
R21230	Instituto de Fisica Corpuscular
R21520	Institut de Ciències de L'Espai
R21550	Institut de Ciènces Fotòniques
R21740	Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
R21910	Centro de Acústica Aplicada y Evaluación No Destructiva
R22100	Centro Nacional de Supercomputación, Barcelona

Sweden

A00260	Luleå tekniska universitet
A13720	Uppsala universitet
A37350	Linköpings universitet
A37370	Lunds universitet
A38180	Kungliga Tekniska högskola
A38670	Chalmers Tekniska högskola
A39840	Mittuniversitetet
R20690	Acreo Swedish ICT AB
R20910	Totalförsvarets forskningsinstitut FOI
R21990	European Spallation Source
R22050	Institutet för Rymdfysik
R22140	European Spallation Source ESS AB

Switzerland

A05000	Scuola Universitaria Professionale della Svizzera Italiana
A12730	École Polytechnique Fédérale de Lausanne - Laboratoire de Physique des Hautes Energies
A12920	Universität Zürich
A13090	Università della Svizzera Italiana
A13630	Université de Genève
A13780	Hochschule Luzern
A14780	École d'Ingénieurs et d'Architectes de Fribourg
A14930	Haute École Spécialisée de Suisse Occidentale
A15050	Haute Ecole d'Ingénierie et de gestion du canton de Vaud
A15480	Universität Basel
A15530	Universität Bern
A36110	École Polytechnique Fédérale de Lausanne - Microelectronics Systems
A37340	École Polytechnique Fédérale de Lausanne - Neuchâtel
A38100	Hochschule für Technik Rapperswil
A38310	Eidgenössische Technische Hochschule Zürich
A38410	Berner Fachhochschule
A38800	Eidgenössische Technische Hochschule Zürich - Basel
A39760	Haute école du paysage d'ingénierie et d'architecture de Genève
A39820	Fachhochschule Nordwestschweiz
R20350	Organisation Européenne pour la Recherche Nucléaire
R20680	Centre Suisse d'Electronique et Microtechnique - Neuchâtel
R20800	Paul Scherrer Institut
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich
R22180	Eidgenössische Materialprüfungs- und Forschungsanstalt

The Netherlands

A00170	Universiteit Twente - CAES
A12010	Vrije Universiteit Amsterdam
A12650	Radboud Universiteit Nijmegen
A14510	Rijksuniversiteit Groningen

A15420	Erasmus Universitair Medisch Centrum Rotterdam
A15620	Stenden Hogeschool
A15960	Universiteit van Amsterdam
A35491	Universiteit Twente - Electrical Engineering
A35701	Technische Universiteit Delft
A38050	Technische Universiteit Eindhoven
R00280	Nikhef
R20370	TNO-FEL
R20430	European Space Agency - ESTEC Microelectronics
R20520	ASTRON Netherlands Foundation for Research in Astronomy
R20540	European Space Agency - ESTEC Payload Technology
R21200	Stichting imec Nederland
R21250	SRON Netherlands Institute for Space Research
R21820	Stichting INCAS3

Tunisia

A12930	École Nationale d'ingénieurs de Sfax
A15300	École Nationale d'ingénieurs de Tunis

Turkey

A13010	Sabanci Üniversitesi
A13530	TC Kocaeli Üniversitesi
A14250	Yeditepe Üniversitesi
A14730	TOBB Ekonomi ve Teknoloji Üniversitesi
A15210	Akdeniz Üniversitesi
A15260	T.C. Okan Üniversitesi
A15280	Orta Dogu Teknik Üniversitesi Kuzey Kibris Kampusu
A15610	Istanbul Sehir Üniversitesi
A15680	Yildirim Beyazit Üniversitesi
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A16280	Adana Bilim ve Teknoloji Üniversitesi
A37960	Istanbul Teknik Üniversitesi
A38270	Ihsan Dogramaci Bilkent Üniversitesi
A38440	Orta Dogu Teknik Üniversitesi
A39170	Bogaziçi Üniversitesi
R20360	Türkiye Bilimsel ve Teknik Arastirma Kurumu Uzay Teknolojileri Arastırma Enstitüsü
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UK

A12260	University of Dundee
A12480	University of Bath
A12860	Glasgow Caledonian University
A13480	Imperial College London
A13510	Royal Holloway University of London
A13520	University College London
A13620	University of Manchester Jodrell Bank Observatory
A14030	Staffordshire University
A14580	University of Lincoln
A14760	University of Leicester
A14980	Queen Mary College of London
A15390	The Open University
A15450	Cardiff University
A15790	City University London
A15850	Nottingham Trent University
A15910	University of Lancaster
A16000	Coventry University
A16050	Cranfield University
A16300	Kings College London
A35030	Sheffield Hallam University
A35053	University of Bolton
A35080	University of Manchester
A35160	Heriot-Watt University
A35180	University of Nottingham
A35250	University of Westminster
A35330	Newcastle University
A35410	University of Hull
A35440	University of Essex
A35470	University of Sheffield
A35520	University of Northumbria at Newcastle
A35630	University of Kent
A35780	University of Cambridge
A35920	University of Bradford
A36000	University of Bristol
A36090	University of Ulster
A36120	University of Strathclyde
A36280	Brunel University
A36341	University of Liverpool
A36342	Liverpool John Moores University
A37300	University of Birmingham
A37320	University of Oxford
A37400	University of Huddersfield
A37420	University of Edinburgh
A37430	University of the West of England
A37490	Queen's University of Belfast
A37570	University of Surrey
A37600	University of Hertfordshire
A37610	University of Southampton
A37630	University of Warwick
A37660	Swansea Metropolitan University
A37730	University of Leeds
A37780	University of South Wales
A37840	University of Durham
A37870	Swansea University
A37900	Manchester Metropolitan University
A38040	Oxford Brookes University
A38450	Loughborough University
A38810	University of York
A39440	University of Glasgow
A39450	Aston University
A39650	University of Salford
R00050	STFC Rutherford Appleton Laboratory
R20600	STFC Daresbury Laboratory
R20950	Diamond Light Source
R22030	STFC UK Astronomy Technology Centre
R22090	Culham Centre for Fusion Energy

Ukraine

A47610	National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute"

United Arab Emirates

A15860	Heriot-Watt University - Dubai
A16120	Abu Dhabi University

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