ACTIVITY REPORT

2018-2019

EUROPRACTICE

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EUROPRACTICE

THE ACCESS POINT FOR INDUSTRY AND ACADEMIA TO ELECTRONIC COMPONENTS AND SYSTEMS

EUROPRACTICE was launched by the European Commission in 1989 to help companies improve their competitive position in world markets by adopting ASIC, Multi-Chip Module or Microsystems solutions in their products. The program helps to reduce the perceived risks and costs associated with these technologies by offering potential users a range of services, including initial advice and ongoing support, reduced entry costs and a clear route to chip manufacture and product supply.

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by offering more than 600 European universities and research institutes affordable access to the latest IC (Integrated Circuits) design tools and technologies. This is reflected in the training provided by universities from which the best IC design engineers emerge, essential for the SMEs innovation in new IC products.

The ultimate goal of EUROPRACTICE is to enhance European industrial competitiveness in the global marketplace. The EUROPRACTICE services are open to industrial companies (especially SMEs), research institutes and academic users.

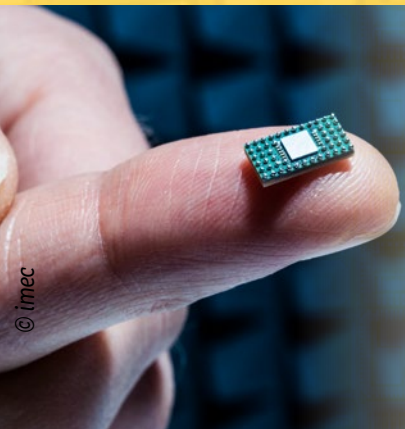
SERVICES OFFERED TO EUROPEAN SMES AND ACADEMIC INSTITUTIONS:

The mission statement of EUROPRACTICE is to provide the European industry and academia with a platform to develop smart integrated systems, from advanced prototype design to volume production. The latter is achieved by providing affordable and easier access to a wide range of state-of-the-art industry-grade fabrication technologies and design tools complemented with training and support to the customer in all critical steps which are needed.

- Affordable access to industry-standard and state-of-the-art design (CAD) tools
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- Low-cost prototyping in various technologies (both ASIC and More than Moore) via MPW runs
- Access to advanced packaging and smart system integration
- Training courses in advanced design flows and on various technologies

IC SERVICES OFFERED TO THE GLOBAL INDUSTRY:

EUROPRACTICE also offers industry worldwide access to microelectronic and microsystem design services, MPW prototyping, small volume production, packaging and test operations. Note, this does not include access to design tools.
Industry from all over the world have rapidly discovered the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who do not always need the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise. This you can get all from EUROPRACTICE IC service, a service that is already established for 20 years in the market.



THE EUROPRACTICE SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:

- imec (Belgium)
- Fraunhofer-Institut für Integrierte Schaltungen (Fraunhofer IIS) (Germany)
- STFC Rutherford Appleton Laboratory (United Kingdom)
- CMP (France)
- Tyndall National Institute (Ireland)

FOREWORD

Dear customers, colleagues and friends,

We hope you will enjoy reading the new EUROPRACTICE Activity Report 2018-2019, which reviews the past year 2018 but in addition looks forward to 2019.

2018 was a fantastic year for many reasons. The main highlight has been that EUROPRACTICE was selected and granted European funding. This new funding secures the EUROPRACTICE services to European universities, research institutes and industry until the end of 2021. In the new H2020 project, named the ***Next EUROPRACTICE eXtended Technologies and Services*** (NEXTS), two new partners CMP and Tyndall complement and extend the EUROPRACTICE offering.

2018 was also a busy year with a new record-number of designs taped out through our EUROPRACTICE service. We realized a total of ***624 design submissions*** in a wide range of technologies with 70% of the designs submitted by European universities and research institutes.

The majority of design submissions (~60%) has been in older technologies (from 0.7µm up to 110nm), which demonstrates the continuing need of technology access to those older nodes. On the other hand, EUROPRACTICE continues to stimulate its users to move to more advanced and specialty technologies (such as silicon photonics). In the recent years, EUROPRACTICE has launched multiple ***first-user Stimulation Actions*** (supported by EU funding). After initial ASIC design competitions to stimulate European universities to design a first IC in standard 0.18µm technology or to start a first IC in an advanced technology (in 90, 65 or 55nm) this was continued with new competitions to stimulate fabrication of Si-Photonics and MEMS designs. Some of those selected and fabricated first-user designs are reported as a specific user story in this report.

In ***2019***, the extended EUROPRACTICE consortium will enhance its services provided to European academia, extend the service to SMEs, encourage new users from non-traditional sectors, add new technologies to serve new markets, diversify the service towards smart system integration, and support the training of future generations of engineers that will be required for the growing digital economy in Europe. Ultimately, EUROPRACTICE will act as a true one-stop shop for technologies enabling fully integrated systems and providing direct routes for industrial up-scaling of those systems and consequently it will contribute to the creation of new jobs and to sustain those jobs in Europe, especially in the areas of design and fabrication of microelectronic components and systems.

To help ensure that Europe remains competitive in the electronics sector, it is absolutely necessary that European industry and innovative start-ups have enough high-quality well-trained engineers graduating from university. Thanks to the continuously evolving EUROPRACTICE service, more than 600 European universities, research institutes and over 300 small and medium-sized companies are provided with a vital infrastructure. EUROPRACTICE has grown to become an indispensable part of the European research and training landscape and part of the solution to helping Europe remain competitive.

We thank the European Commission (DG Connect) for their support. The EC funding has ensured that we hold our commitment to continue the EUROPRACTICE service and to offer our European members easy and affordable access to state-of-the-art design tools and to IC technologies.

Last but not least we thank all of you, our customers, universities and research institutes; our technology and design tool suppliers; for supporting our services and we wish you all a successful 2019.

Looking forward to another productive and fantastic year.

Romano Hoofman (EUROPRACTICE project manager)
On behalf of the entire EUROPRACTICE team at imec, STFC, FhG-IIS, CMP and Tyndall

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EUROPRACTICE SERVICES

THE ACCESS POINT FOR ELECTRONIC COMPONENTS AND SYSTEMS

EUROPRACTICE (1995-present) and its forerunner EUROCHIP (1989-1995) have supported the European academic sector with CAD tools and IC prototyping for almost 30 years, and SMEs have been supported with IC prototyping and small volume services for over 15 years. The provided services are widely recognized as world-leading.

Currently approximately 600 academia from the EU member States and "extended" Europe are supported by this EUROPRACTICE service funded by the European Commission. Eligible institutions are currently able to access CAD services and MPW services at discounted prototyping prices.

The European Commission has financially supported the provided services that offer the European universities, researchers appropriate access to CAD tools, advanced technologies, design kits, IP blocks and training to support their education, prototyping and small volume production.

In 2019, a new H2020 project has been launched, named the "Next EUROPRACTICE eXtended Technologies and Services" (NEXTS), in which two new partners CMP and Tyndall complement and extend the EUROPRACTICE offering. It will build upon the well-established, widely-used and successful EUROPRACTICE service and extend towards SMEs and System Integration.

The mission statement of the extended EUROPRACTICE consortium is to provide the industry and academia (in particular those in Europe) with a platform to develop smart integrated systems, from advanced prototype design to volume production. The latter will be achieved by providing affordable and easier access to a wide range of state-of-the-art industry-grade fabrication technologies and design tools complemented with training and support to the customer in all critical steps which are needed.

Ultimately, EUROPRACTICE acts as a true one-stop shop for technologies enabling fully integrated systems and providing direct routes for industrial up-scaling of those systems and consequently it will contribute to the creation of new jobs and to sustain those jobs in Europe, especially in the areas of design and fabrication of microelectronic components and systems.

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THE EUROPRACTICE BUSINESS MODEL

The EUROPRACTICE business model is based on a coordinated brokerage service for industry and academia looking for affordable and easier access to technologies in the domain of electronic smart systems – which builds on the many years' experience of its partners: imec, STFC, Fraunhofer IIS, CMP and Tyndall.

EUROPRACTICE provides its customers technology access through a vast network of technology suppliers, ranging from design tool vendors and foundries to packaging, assembly & test houses – who all provide state-of-the-art industry-grade technologies.

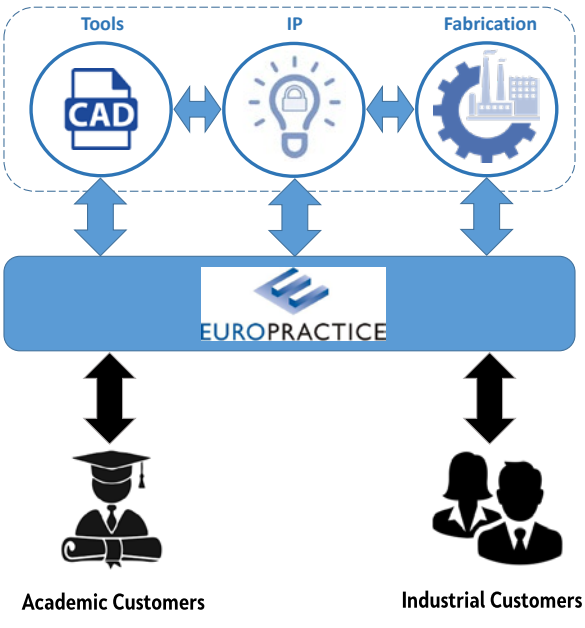


Fig. 1: Schematic representation of the entire NEXTS ecosystem, depicting a central role of the NEXTS service as prime interface between the technology suppliers (on top) and the customers (at the bottom).

The overall concept is that EUROPRACTICE acts as the prime interface between the users/customers and the technology providers (such as design tools and IP library vendors, foundries, assembly and test houses). Such a prime interface (or one-stop function) has advantages for both the supply and demand side of the value chain. The latter is schematically depicted in Figure 1, where the supply side is depicted on top, the demand side at the bottom and centrally EUROPRACTICE.

On the supply side, one can find centrally the current technology portfolio, where design tools are supplied by design tool vendors, technology IP by IP library vendors and fabrication services by various foundries. The technology portfolio is extended with emerging technologies typically offered by leading research institutes, and technologies which are brokered by other technology service providers (such as CMC in Canada for some MEMS options by Teledyne Dalsa).

Although EUROPRACTICE represents a large user base, it is considered as one user to the suppliers. Design tool vendors, IP-vendors and foundries have only to deal with EUROPRACTICE, and have their products and technologies promoted and securely distributed all over Europe. Thanks to this, it has been possible to negotiate (i) access and (ii) very favorable conditions for the EUROPRACTICE customers. This would not be possible when operating on a national level with only a very few users. Since the service is being offered on a pan-European level, the know-how and experience has only to be built up once.

AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated low cost prices with the major design tool vendors world-wide and also with IP and programmable device vendors. Consequently, European academic institutions can purchase EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics, ...) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service also provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

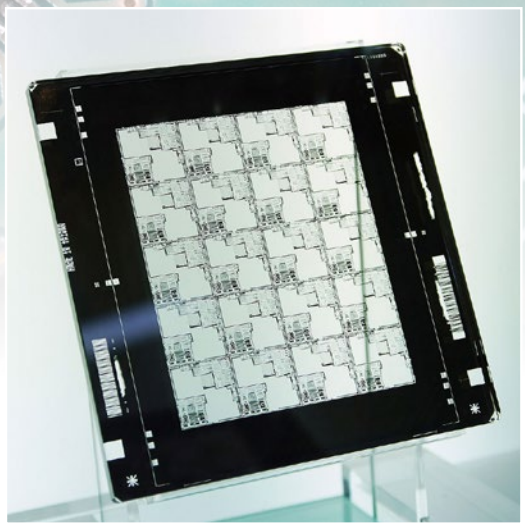
The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows them to participate in EC-funded projects, ranging from IP block and component design to complete system design.

Some mechanisms and terms and conditions have been negotiated which, subject to the approval of the specific design tool vendor to be obtained via STFC, allow:

- a design originally undertaken for non-commercial purposes to be exploited commercially
- non-commercial licenses installed at an experienced academic institute to be used by a start-up company, e.g. an academic spin-out, under the guidance of the academic institute to produce a commercial demonstrator to prove the viability and marketability of a novel end product. The design cannot be then sold or assigned without a further appropriate payment being made directly to the design tool vendor.

These and other similar mechanisms will be introduced to help lower the barrier to effective innovation by academic institutes and start-ups.

ACCESS TO PROTOTYPING FOR ASICS, MEMS AND PHOTONICS



In general, foundries are not willing to give access to their fabrication lines to academic institutes and small companies due to the high level of technical support required, unless a high-volume production is guaranteed – which is not the case for university prototype fabrication or SME small volume needs.

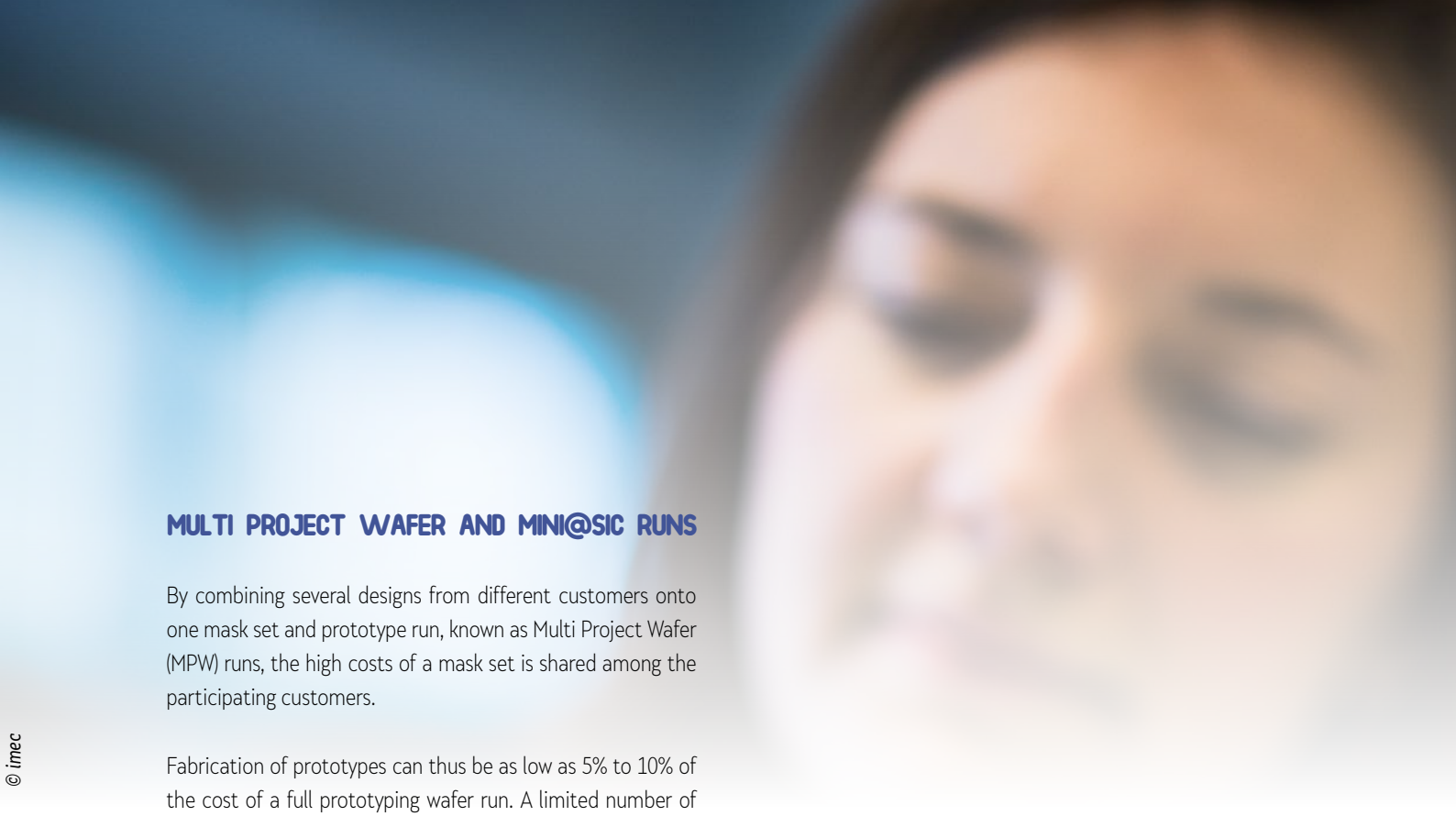
Over the last decades, leading IC-foundries have recognized that EUROPRACTICE is the ideal partner to offer low-cost prototyping services to smaller users and academia as EUROPRACTICE is the entity that offers both access and technical support.

The current technology portfolio includes a wide range of technologies from 3µm to 22nm, from digital logic, RF, mixed-signal to High Voltage and from SiGe, MEMS to Si-photonics. The service will be kept to a manageable size by endeavoring to obtain the maximum functionality from the minimum number of foundries or technologies.

Currently, 6 of the 8 ASIC foundries (namely OnSemi, ams, IHP, X-FAB ST Microelectronics and GLOBALFOUNDRIES) have manufacturing facilities in Europe and the Si-photonics fabrication takes place in IHP, imec and CEA-Leti (where the last two are leading European RTOs).

The cost of producing a new ASIC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. EUROPRACTICE has reduced the prototyping cost, especially for ASIC prototyping, by two techniques:

1. Multi Project Wafer Runs or
2. Multi Level Masks.



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MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto one mask set and prototype run, known as Multi Project Wafer (MPW) runs, the high costs of a mask set is shared among the participating customers.

Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full prototyping wafer run. A limited number of tested or untested ASIC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time". In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the teaching and research designs at the universities were much smaller than the minimum charged design size on regular MPW runs, the concept of **mini@sic** runs was introduced in 2003 – which was a solution to offer lower prototype fabrication cost.

The mini@sic principle is based on the methodology that 2 to 3 times per year on selected MPW runs a minimum area MPW block size will be bought, which is resold in smaller cheaper sub-blocks. This mini@sic MPW principle was extended over the years towards 90nm, 65nm, 40nm, 28nm CMOS, and now 22nm FDSOI to accommodate affordable prototype fabrication of small designs for the European universities and research institutes.

In 2018, EUROPRACTICE has also added a **MICROBLOCK** in the 28nm technology from TSMC. The Micro-block size is 1110 x 1110 microns (designed area – pre-shrink), which is available for ~10kEUR. Microblock designs can be placed on any of the 28nm-mini@sic runs. However, note that in case of only one microblock there is no commitment that the run will be launched.

MULTI LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi Level Mask (MLM). With this technique the available mask area (20 mm x 20 mm field) is typically divided in four quadrants (4L/R : four layer per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is thus reduced by a factor of four. By adapting the lithographical procedure it is possible to use one mask four times for the different layers by using the appropriate quadrants. Using this technique, the mask costs can be reduced by about 60%.

The advantages of using MLM single user runs are: (i) lower mask costs, (ii) can be started any date and not restricted to scheduled MPW runs, (iii) single user and (iv) customer receives minimal a few wafers, so a few hundreds of prototypes.

This technique is preferred over MPW runs when the chip area becomes large and when the customer wants to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.

This technique is only available for technologies from ON Semiconductor, IHP, TSMC, GLOBALFOUNDRIES and XFAB.

TECHNOLOGY PORTFOLIO

For 2019, EUROPRACTICE will continue to extend and update its technology portfolio. Currently, customers can have access to prototype and production fabrication in the following technologies:

- On Semi 0.7µ C07M-D
- On Semi 0.7µ C07M-A
- On Semi 0.35µ C035U
- On Semi 0.7µ C07M-I2T100 100V
- On Semi 0.35µ C035-I3T80U 80V
- On Semi 0.35µ C035-I3T50U 50V
- On Semi 0.35µ C035-I3T50U (E) 50V
- On Semi 0.35µ C035-I3T25U 3.3/25V
- ONC18MS 0.18µm
- ONC18MS-LL 0.18µm
- ONC18HPA 0.18µm
- ONC18-I4T 0.18µm 45/70V
- On Semi 0.5µ CMOS EEPROM C5F
- On Semi 0.5µ CMOS EEPROM C5N

- ams 0.35µ CMOS C35B4C3
- ams 0.35µ CMOS C35OPTO
- ams 0.35µ HV CMOS H35B4D3
- ams 0.35µ SiGe-BiCMOS S35
- BARC Diode for ams C35OPTO
- WLSCP for ams C35B4C3

- IHP SGB25V 0.25µ SiGe:C
- IHP SG25H3 0.25µ SiGe:C
- IHP SG25H5_EPIC (BiCMOS + photonics)
- IHP SG25 PIC (photonics)
- IHP SG13S 0.13µ SiGe:C
- IHP SG13C 0.13µ SiGe:C
- IHP SG13G2 0.13µ SiGe:C
- IHP BEOL SG13

- X-FAB XH035 0.35µ HV
- X-FAB XH018 0.18µ HV NVM E-Flash
- X-FAB XT018 0.18µ HV SOI
- X-FAB XS018 0.18µ OPTO
- X-FAB XP018 0.18 µ NVM
- X-FAB XR013 0.13µ RF-CMOS

- TSMC 0.18 CMOS Log/MS/RF (G)
- TSMC 0.18 CMOS HV BCD Gen2
- TSMC 0.13 CMOS Log/MS/RF (G,LP)
- TSMC 90nm CMOS Log/MS/RF (G,LP)
- TSMC 65nm CMOS Log/MS/RF (G,LP)
- TSMC 40nm CMOS Log/MS/RF (G,LP)
- TSMC 28nm CMOS Log HPL/HPC/HPC+
- TSMC 28nm CMOS RF HPL/HPC/HPC+

- ST 28nm CMOS28FDSOI
- ST 55nm BiCMOS055
- ST 65nm CMOS065
- ST 130nm BiCMOS9MW
- ST 130nm H9SOI-FEM
- ST 130nm HCMOS9GP
- ST 130nm HCMOS9A
- ST 0.16µ BCD8sP
- ST 0.16µ BCD8s-SOI

- UMC L180 Logic GII, MM/RF
- UMC L180 EFLASH Log GII
- UMC CIS18 – CONV diode
- UMC CIS18 – ULTRA diode
- UMC L130 Log/MM/RF
- UMC L110AE Log/MM/RF
- UMC L65N Log/MM/RF (SP)
- UMC L65N Log/MM/RF (LL)
- UMC 40N Log/MM – LP
- UMC 28N Log/MM – HPC

- GF 130nm BCDlite
- GF 130nm LP
- GF 55nm LPe/LPx-NVM/LPx-RF
- GF 40nm LP/LP-RF/RF-mmWave
- GF 28nm SLP/SLP-RF
- GF 22nm FDSOI

- imec Si-Photonics Passives+
- imec Si-Photonics ISIPP50G
- imec SiN-Photonics BioPIX 300
- imec SiN-Photonics BioPIX 150

- LETI Si-Photonics Si310-PHMP2M
- LETI MAD200 130nm NVM

- Teledyne Dalsa MIDIS

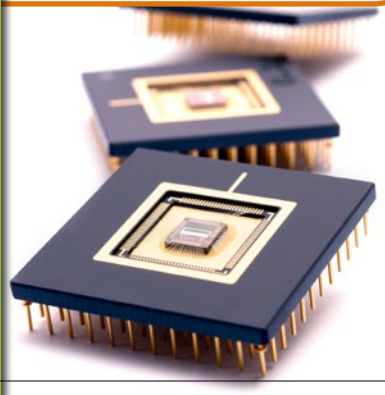
- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- MEMSCAP PIEZOMUMPS

PACKAGING AND ASSEMBLY

Standardly, EUROPRACTICE delivers unpackaged untested prototypes. However, EUROPRACTICE offers a low cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of packages are available ranging from DILs to PGAs and QFNs.

Side by side with world class partners and our long-term agreements, EUROPRACTICE boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.

In addition, photonics packaging is offered which is serviced by Tyndall. The photonics ecosystem continues to gather momentum attracting new users (both from academia and from industry) and increasing the technical scope of the photonics offering via EUROPRACTICE. Finally, various wafer-level packaging technologies will be offered through CEA-Leti and Fraunhofer IZM channels, ranging from 3D front side micro-bumping to 3D backside TSV, RDL and bumping.



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FROM PROTOTYPES TO VOLUME PRODUCTION

After successful ASIC prototyping, the EUROPRACTICE partners (in particular CMP, Fraunhofer IIS and imec) can also provide the customer access to the full production and qualification stage (from low to mid-high volumes).

PROTOTYPE FABRICATION

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. EUROPRACTICE will take care of the production for the first prototypes of the customer and organize the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program.
The devices can be tested on both wafer level as well on packaged devices. The goal is to reduce the test time and to test the ASIC for manufacturing problems using the ATPG and functional patterns.
EUROPRACTICE will support you during the development of single site test solution as well as with a multi-site test solution when high volume testing is required. Based on the test strategy followed diverse type of implementations can be realized.

DEBUG AND CHARACTERIZATION

Before going into production, a characterization test program will check if all the ASIC specifications are met according to the customer expectations. Threshold values are defined for each tested parameter. The software will test all different IP blocks and the results will be verified with the bench test results.
A characterization at Low (LT), Room (RT) and High (HT) temperature will be performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be strong against process variations, the product qualification can start. EUROPRACTICE can support you through the full qualification process using different kind of qualification flows ranging from Consumer, Industrial, Medical to Space according to the Military, Jedec and ESCC standards....
In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

YIELD IMPROVEMENT

EUROPRACTICE can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the characterization and qualification of the device on corner lots, EUROPRACTICE can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers will be analyzed to check for yield issues related to assembly or wafer production. EUROPRACTICE is using the well proven tool Examinator™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.

SUPPLY CHAIN MANAGEMENT

EUROPRACTICE is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.
Customer products are treated internally as projects and followed closely by the imec engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. EUROPRACTICE therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

The most relevant companies involved in our semiconductor supply chain are listed below:

- **Foundry partners:** TSMC, UMC, ON Semi, ams, IHP, XFAB, ST Microelectronics, GLOBALFOUNDRIES, MEMSCAP, Teledyne Dalsa, imec and CEA-LETI
- **Ceramic assembly partners:** HCM, Systrel, Optocap, Kyocera
- **Plastic assembly partners:** ASE, Kyocera, StatsChipPac
- **Wafer bumping partner:** Pactech, FCI, ASE
- **Si-photonics packaging:** Optocap, Tyndall (low-volume/non-standard), PIXAPP (medium-volume/standard)
- **Test partners:** Microtest, ASE, Delta, RoodMicrotec, Aptasic and Blue test
- **Failure analysis:** Maser Engineering, RoodMicrotec
- **Library partners:** Faraday, ARM, INVECAS, Cadence, Synopsys, Aragio, eMemory

TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

EUROPRACTICE training courses for European universities and Research Institutes are primarily aimed at academic staff and PhD students. Unlike training courses which address single topics or individual design tools, the EUROPRACTICE training courses address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow. Since the courses are based on the EUROPRACTICE EDA/CAD tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the EUROPRACTICE services/ infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants will be able to extensively practice the concepts described in lectures and have access to experts who are able to answer questions about the concepts, design tools or technology process discussed on the course. Where it is known that a design flow is well supported by multiple vendors and/or processes then multiple course variants will be offered that reflect the design tool / processes installed base.

New training courses will be added covering new design tools, new design flows, new nanoelectronic component technologies and smart system integration strategies. Courses will be offered at various "levels" ranging from introductory to advanced suitable for a wide range of attendees. Formal training courses will be augmented with a webinar series developed by EUROPRACTICE to ensure that training can be accessed easily by the widest possible audience.

During 2018 a total of 234 delegates (19 Lecturers, 91 Postgraduate students, 124 Researchers) attended 26 training courses organized by the EUROPRACTICE partners at 4 locations (as visualized on the map in the Figure above). The delegates came from 120 EUROPRACTICE Member Institutions in 25 countries.

Since EUROPRACTICE Training courses began in April 2014, a total of 886 delegates from 239 Member Institutes in 37 countries have attended 104 training courses making 3310 days of practical training.

OUTREACH AND COMMUNICATION

In order to stay in close contact with the customers and various stakeholders, EUROPRACTICE has presented and promoted their services through different channels for many years. A snapshot of those channels is listed below:

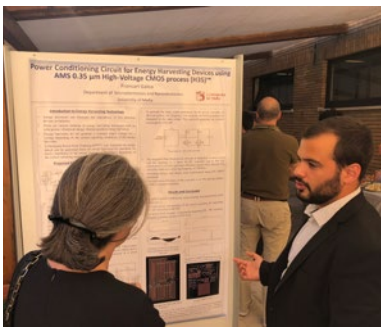
EUROPRACTICE WEBSITES

The current EUROPRACTICE service is operating 2 web pages in order to promote the service and to keep all (potential) users updated on new available tools and technologies.

- www.europractice.stfc.ac.uk : The design tool web site is hosted and maintained by STFC. This page contains all the latest information about the design tools, training courses and events.
- www.europractice-ic.com : The MPW prototyping / fabrication web site is hosted and maintained by IMEC and contains the latest news on MPW offering, schedule and pricings.

LEAFLETS, BOOKLETS AND FLYERS

Several leaflets and flyers are available and regularly updated. These contain detailed information on the technologies and services offered and on the associated timings and pricings. Next to the annual Activity Report, two separate booklets are produced (next to the; one describing the Design Tools and Programmable Platforms, the other describing the training courses. All of these are typically distributed during booths and exhibitions at multiple academic conferences and industrial fairs.



EXHIBITION BOOTHS AND PRESENCE AT CONFERENCES AND FAIRS

EUROPRACTICE is present at various scientific conferences and industrial trade shows/fairs in order to present its service to existing customers and to attract new customers. Typically, this is doing by means of an exhibition booth, table exhibit, poster and/or presentation. In 2019, EUROPRACTICE will be present at least at the following events:

ISSCC 2019	San Francisco, US	17-21 February
DATE 2019	Firenze, Italy	25-29 March
SSI 2019	Barcelona, Spain	10-11 April
DAC 2019	Las Vegas, US	2-6 June
Transducers 2019	Berlin, Germany	23-27 June
ESSDERC / ESSCIRC2019	Krakow, Poland	23-26 September
EFECS 2019	Helsinki, Finland	19-21 November

NATIONAL SEMINARS

In 2018, EUROPRACTICE started with the organization of national or regional seminars, where academic and industrial customers can meet and exchange learnings with each other and other stakeholders. Typically, the program is one-day. The morning session consists of plenary sessions in which EUROPRACTICE will share its current offering and its projected roadmap, but in addition highlights of user projects (preferably focusing on collaboration between academia and local industry). The afternoon session is more interactive consisting of an open-market place where users can present their results to each other by means of posters and demonstrators.

In 2018, three national seminars were organized, namely at UCM in Madrid, Spain, at INFN Roma Tor Vergata in Rome, Italy and at AGH in Krakow, Poland. For 2019, at least 4 national seminars are planned in Germany, UK, Benelux and Ireland.

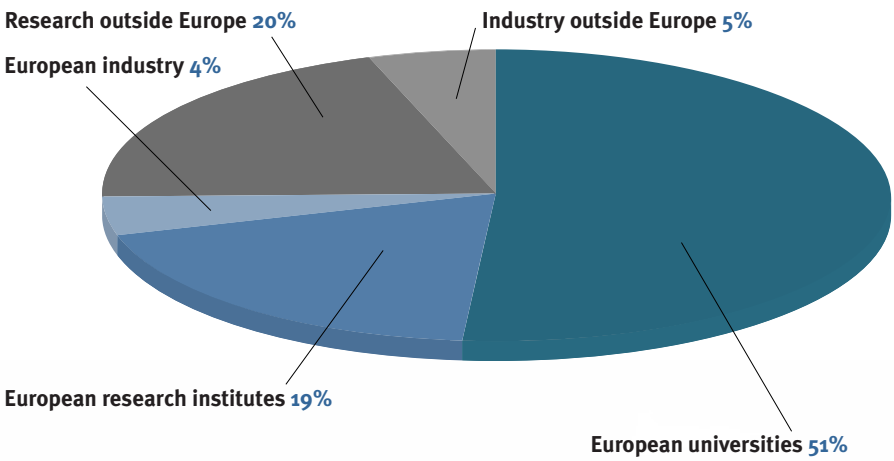
Pictures taken during the National Seminar in Rome, where universities from Italy and Malta were present.

FABRICATED DESIGNS IN 2018

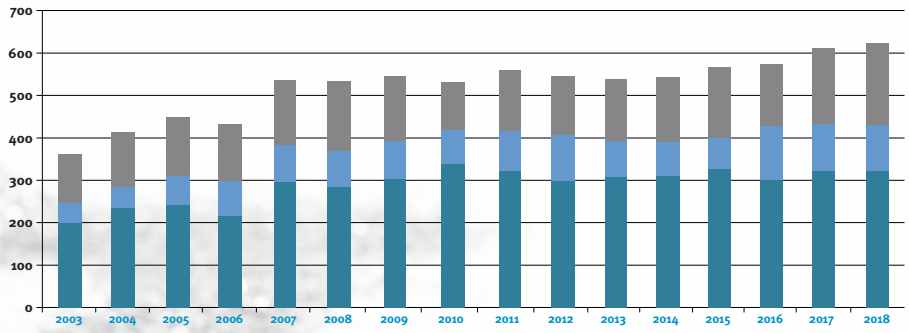
NUMBER OF PROTOTYPED CIRCUITS ON MPW RUNS

In 2018, a total of 624 submitted designs have been prototyped, again an increase compared to 2017, when already a record-high number of 614 submitted designs were noted. It has to be noted that the results of 2018 only the submitted designs to imec and Fraunhofer as service center are included (and not those to CMP).

70% of the designs are sent in by European universities and research institutes while the remaining 30% of the designs is accorded for by non-European universities (20%) and commercial companies world-wide (10%).



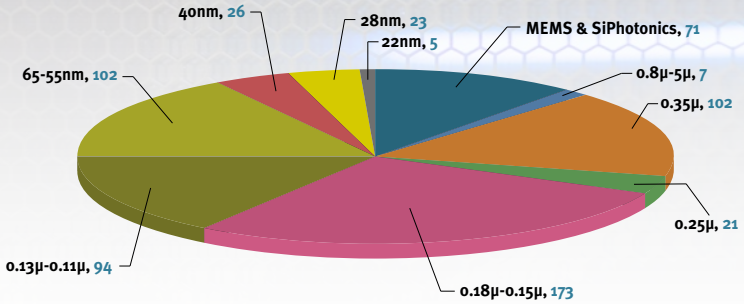
MPW designs in 2018



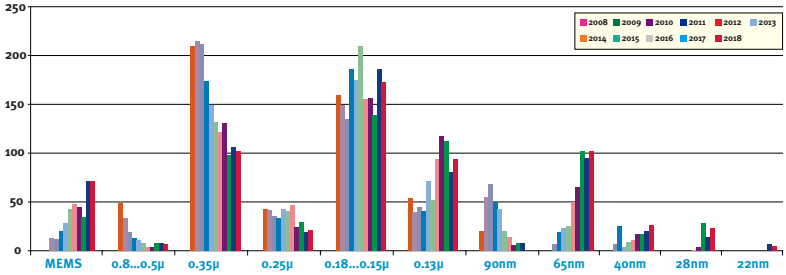
	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
Industry + non-European univ/research	115	128	138	134	154	164	153	113	143	139	144	153	169	145	182	183
Europractice Research	48	52	69	84	87	85	87	83	96	105	87	80	72	128	109	120
Europractice Academic	200	234	243	215	298	285	305	337	321	301	307	311	328	301	323	321

A GOOD TECHNOLOGY AND GEOMETRY MIX

Year over year a shift towards more advanced technologies was observed, however in 2017 this trend has stabilized, and also it is 2018 there has been no significant increase in advanced technologies, as is shown in the bar graphs. The 0.18µ / 0.15µ and 0.13µ / 0.11µ technologies still represent almost half of the total designs and even the older nodes such as 035µ still remain very popular with more than 100 design. Finally, the popularity of Silicon Photonics and MEMS in 2017 has been confirmed 2018, which is thanks to the high number of designs in the imec Si-photonics technologies (namely 61 designs in total) and also thanks to the EU-supported First User Stimulation Actions.



MPW designs in 2018: technology node and number of designs

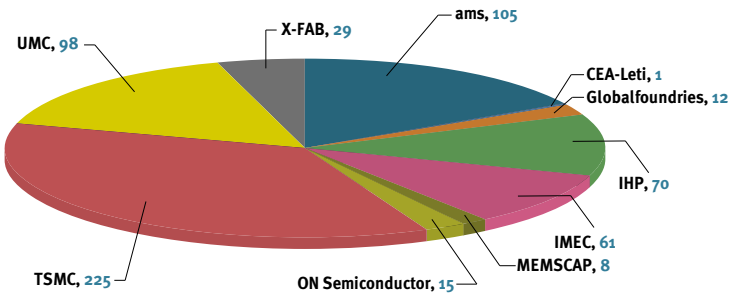


Geometry mix

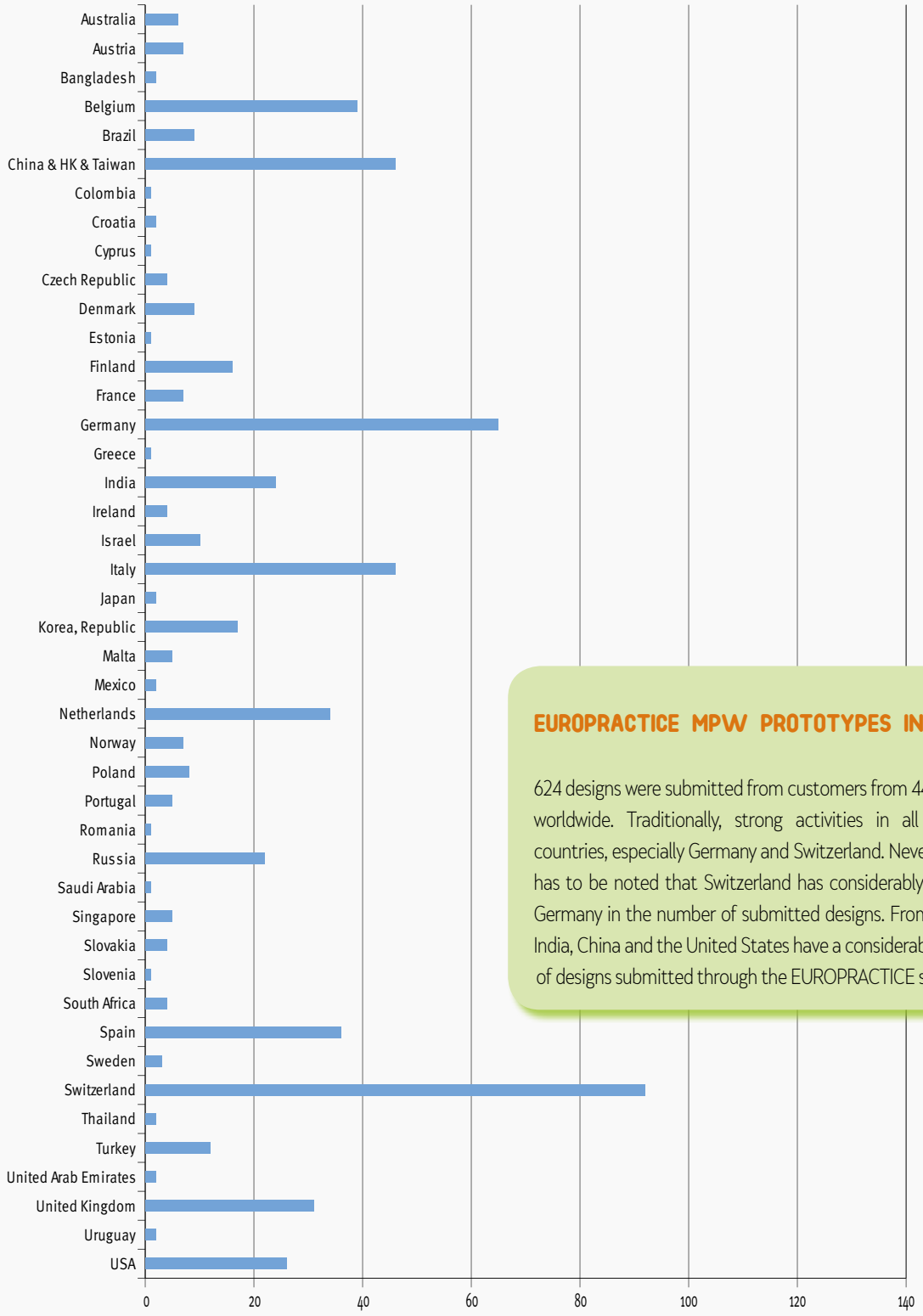
TECHNOLOGIES ACCESS THROUGH WORLD-LEADING FOUNDRIES

Technology access is provided through world-leading foundries (ams, GLOBALFOUNDRIES, ON Semiconductors, TSMC, UMC and X-FAB), complemented by specialty fabs at CEA-Leti, IHP, imec and MEMSCAP. Most of the submitted designs in 2018 were fabricated in TSMC, which is also the leading foundry for the global industry.

On the other hand, one of the European foundries, austriamicrosystems (ams) has the second largest number of designs fabricated, thanks to its user-friendly PDK and diverse technology offering. One of the other European foundries, X-FAB has doubled its number of fabricated designs as compared to last. Finally, the fabrication of Si-photonics circuits in the imec fab continues to grow as well.

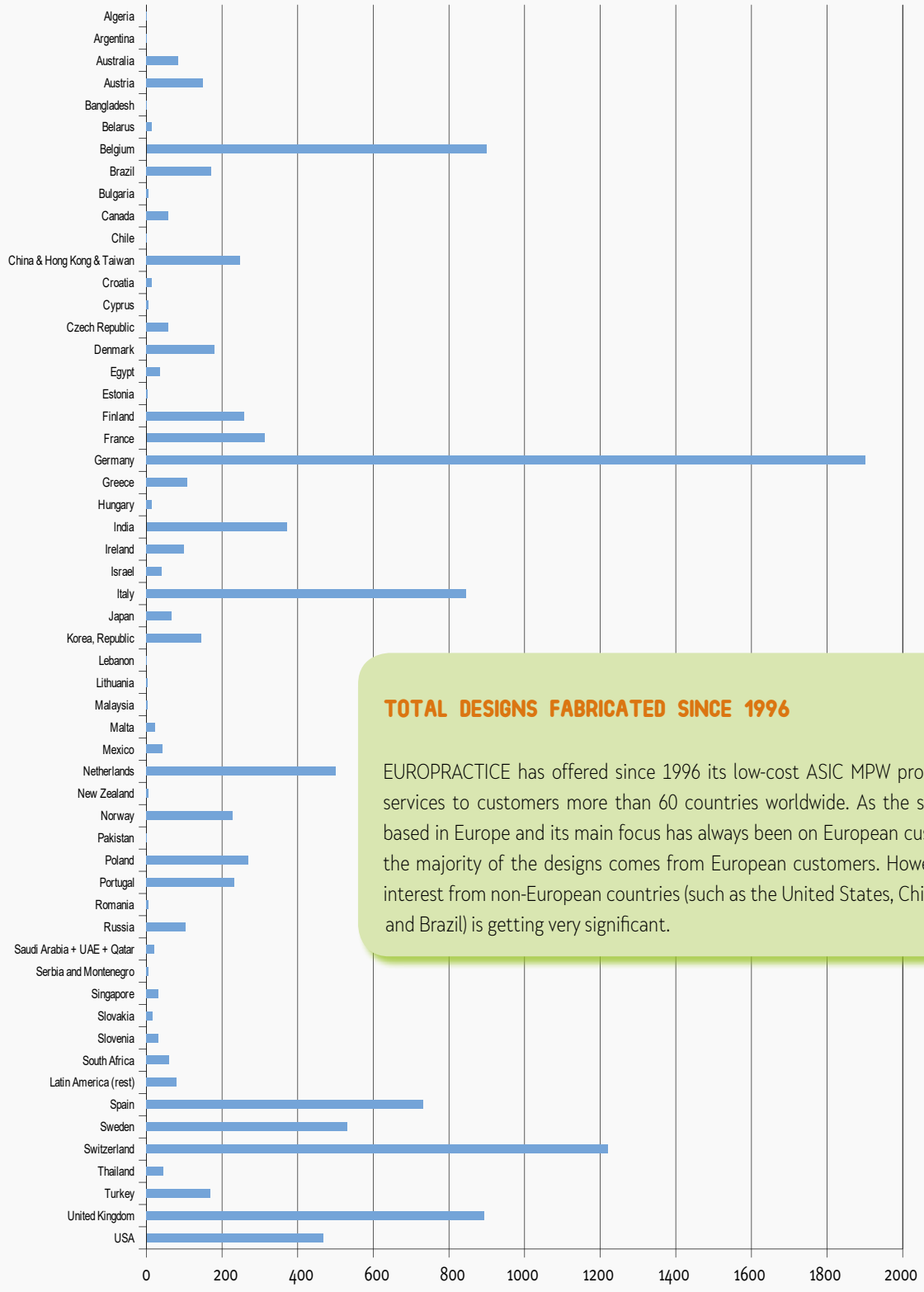


number of *designs per foundry in 2018*



EUROPRACTICE MPW PROTOTYPES IN 2018

624 designs were submitted from customers from 44 countries worldwide. Traditionally, strong activities in all European countries, especially Germany and Switzerland. Nevertheless, it has to be noted that Switzerland has considerably surpassed Germany in the number of submitted designs. From overseas, India, China and the United States have a considerable amount of designs submitted through the EUROPRACTICE service.



TOTAL DESIGNS FABRICATED SINCE 1996

EUROPRACTICE has offered since 1996 its low-cost ASIC MPW prototyping services to customers more than 60 countries worldwide. As the service is based in Europe and its main focus has always been on European customers, the majority of the designs comes from European customers. However, the interest from non-European countries (such as the United States, China, India and Brazil) is getting very significant.

ONSemi C0.7

Microelectronics research at USP of São Carlos

Group of Metamaterials, Microwaves and Optics (GMeta), Dept. of Electrical Engineering (SEL), University of São Paulo (USP), São Carlos - SP, Brazil

Contact: Prof. João Paulo Carmo, Rodrigo Henrique Gounella, João Paulo Costa, and Tiago Matheus Nordi
E-mail: jcarmo@sc.usp.br
Technology: ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR
Die size: 2234.40µm × 2234.40µm

Description

This microdevice is composed by several photonic, analog and digital IP blocks. One of the blocks comprises a second generation of an optical transceiver for integration on minimum invasive medical devices to provide intra-body communication (red-shading in the figure). This transceiver is intended to exchange data at high speed from/to the interior of the human body and was designed to operate near the 850nm. The selection behind the 850nm was due to low attenuation of the living tissue and to get high data-rates without the need to use radiofrequency waves at high frequencies, avoiding the high losses by the tissue. The transceiver is fully integrated in CMOS, excepting the optical source. Inside is composed by a digital modem with a parallel interface with the controller of the medical devices or with a microcontroller. It is also composed by two PLLs, one to provide the desired and programmable clock and other to recover the clock from the received bitstream. The difference to the first generation (also in 0.7µm from the on-semiconductor) is the first PLL that was fully converted to allow the frequency selection and the current-to-voltage converter from the CMOS photodiode used to convert light into a photocurrent. Moreover, this block also allows the selection between the option to encoding or not the bitstream to send, in order to allow an easier clock recovery in the receiver.

Another photonic block within this microdevice is a sensor to accurately read the angle of incidence of the light (yellow-shading). This block was designed to be integrated on photovoltaic sub-modules to track the sun, thus allowing the photovoltaic panels to move to the optimal position to maximize the converted power. The photodetectors generate photocurrents proportional to the angle of incidence thanks to the metal and polysilicon structures placed on top. These photocurrents are converted on output voltages for sampling and analog-to-digital conversion. The microdevice contains two sets of the former photodetectors, each one to a specific type of readout circuit. The architecture of one of the readout circuits is based on the 3T-pixel, used on CMOS images, while the other is based on current mirroring combined with transmission ports for reading and for resetting. This microdevice also contains a sample-and-hold circuit for interfacing with this photonic block. The photodetectors used in this photonic block are n+/p sub photodiodes, which are also individually provided for testing, for characterization purposes and to use with other external circuits (pink-shaded).

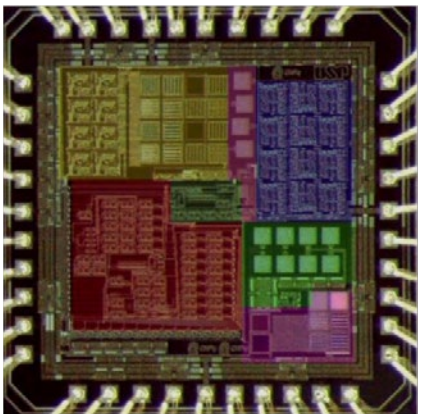


Fig.1: Photo of the fabricated microdevice and respective blocks highlighted with different shadings.

A low-power operational amplifier was also fabricated to prototype amperometric circuits for application with functionalized electrodes for the detection of the C-hepatitis (light green-shading). The target is the future integration of a developed prototype of a portable laboratory platform.

A voltage-controlled-oscillator (VCO) was also fabricated to generate signals in the range [370, 510] MHz, fully covering the LPD433 band (low power device 433 MHz) whose frequencies are located within the range [433.050, 434.790] MHz (dark green-shading). This VCO was designed to test radio-frequency circuits working in this band.

It was also fabricated a circuit to test a new and ESD-robust anti-latch structure to interface digital circuits fabricated in this technology with external circuits (wine-colored-shading).

Finally, the blue-shading in the figure highlights a second generation of an arbitrary/programmable PN sequence generator. This generator is intended to be used on chemical sensors based on radio-frequency.

Why Europractice?

I first came into contact with the Europractice services in 2005 and at that time I immediately got a positive impression. Since that time, I always used this service because among other factors, it offers affordable prototyping for research. It requires simpler procedures to access the technologies and a easy and comprehensible website, when compared to similar services in- and outside Europe. It is very easy and straightforward to access the NDAs and PDKs without complicated and useless bureaucracies. The submission page is also very easy to use. The Europractice service is always open to questions and suggestions related to delivery and billing.

Acknowledgements

Professor João Paulo Carmo was supported by the Brazilian National Council of Scientific Research (CNPq) with a PQ scholarship (Pesquisador de Pró-Actividade), grant 305250/2015-9. Rodrigo Henrique Gounella was sponsored by the FIPAI with a PhD Scholarship, grant FB-026/18. The fabrication of this microdevice was sponsored by CNPq under the project grant 400110/2014-8.

The readout integrated circuit (ROIC) for self-compensating method of bolometer-based IR focal plane arrays measurement

Department of Microelectronics (UMEL), Faculty of electrical engineering and communication (FEEC), Brno University of Technology (BUT), Brno, Czech Republic

Contacts: Ing. Roman Prokop, PhD., Doc. Ing. Pavel Neužil, PhD., Ing. Jan Pekárek, PhD.

E-mail: prokop@feec.vutbr.cz

Technology: ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR

Die size: 4647.6µm × 3256.2µm

Description

The readout integration circuit contains a self-compensating system for fixed pattern noise reduction (FPNR) of focal plane arrays (FPAs) of infrared bolometer detectors. It is based on a first-order ΔΣ modulator serving as a non-saturating signal integrator. The used method suppresses both the effect of bolometer resistance due to non-uniformity across the FPA as well as the self-heating effect. The proposed system does not require any external or internal feedback loop for FPNR. This approach can be also used for other applications where a signal compensation is required.

Highlights

- First-order ΔΣ modulator serving as a non-saturating signal integrator
- The self-heating effect is rejected as the common mode
- ≈1000 × improvement in the readout amplitude of the bolometer signal
- System suitable for the ROIC for bolometer-based FPAs

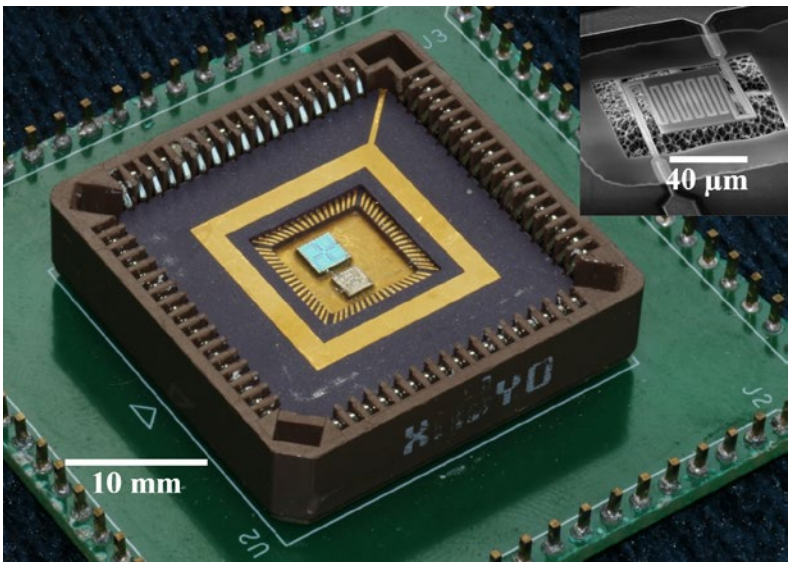


Fig. 1 Photo of ASIC and bolometer chips mounted in an LCC 68 package and placed into a testing socket. (inset) SEM image of fabricated bolometer.

Infrared (IR) radiation in the wavelength range from 8 μm to14 μm is used in many applications such as astronomy, thermal scanning to search for people or animals, medical applications and recently very popular the preventive maintenance of electrical appliances and monitoring the thermal isolation of buildings.

A modern ΔΣ principle was used in bolometer-based FPAs. Researchers massively used parallel ΔΣ analog-to-digital converters (ADC) together with multiplexing principle to process the bolometer-FPA data. Another principle of data processing with ΔΣ modulator was shown with a heat balanced bolometer operating in a closed-loop mode. In our ROIC system we use a signal processing system with a non-saturating integrator. This integrator was achieved using the first-order ΔΣ modulator combined with a sample and hold circuit (S/H). It does not require a DAC and/or any extra off-chip circuits to perform FPNR. It can be combined with a self-heating correction technique to improve the performance of the proposed system.

The principle of the non-saturating integrator (ΔΣ) for FPNR is as following. The signals from the bolometers forming the FPA are processed by ROIC to eventually form an image of IR radiation. Integrating the bolometer output signal improves the signal-to-noise (SNR) ratio, a key performance parameter of circuit processing such minute electrical signals. As mentioned above, the fundamental problem with bolometer measurement is its small ΔR due to incident IR radiation and a few orders of magnitude smaller than the nominal value of R. In addition, the actual R value fluctuates due to uncertainty in the FPA fabrication process. First-order ΔΣ modulation consists of a current integrator followed by a clocked comparator.

This system produces a pattern of two logical levels at the clocked comparator output and a residual value of VBAL and the integrator output at the end of the conversion. While the digital pattern corresponds to the nominal bolometer resistance, the VBAL shift expresses the small bolometer resistance variation caused by the bolometer temperature change due to IR.

Let's assume that the bolometer nominal resistor value is ≈10 kΩ and its TCR is 3·10−3 K−1, then the temperature change of ≈10 mK will cause the bolometer resistance change of ≈0.3 Ω. The system has a sensitivity of (−65.6 ± 1.6) mV·Ω−1 (mean ± standard deviation). Then the corresponding ROIC output voltage shift of 1 mV corresponds to ≈15 mΩ resistance change corresponding to the bolometer membrane temperature change of the ≈0.5 mK.

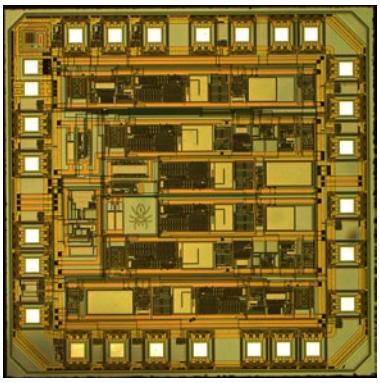


Fig. 2 – Year 2016, several testing and adjustable ROIC topologies for 1 sensor measurement

Thanks to the Europractice service we were able to process the first prototype in 2016 (Fig. 2) with some adjustable parameters to prove the principle. In 2018 the final 10-channel ROIC for 10 x 10 or 1x100 bolometer matrix measurement (Fig.3).

Why Europractice?

The Europractice service offers affordable prototyping for research. However, in my point of view, it has quite simple, easy and straightforward procedures to access the technology and to get support and information as well. The submission page is also very easy to work. The Europractice service is always open to questions and suggestions related to delivery and billing.

Acknowledgement

This work was supported by the Grant Agency of the Czech Republic under GA13-19947S project, by the Ministry of the Interior of the Czech Republic under VI20152019043 project and by Horizon 2020 ASTONISH - Advancing Smart Optical Imaging and Sensing for Health (8A16003). Cadence software was used with support through the Cadence Academic Network.

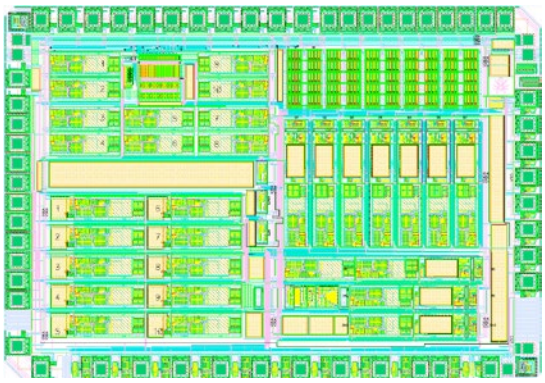


Fig. 3 – Year 2018, the final 10-channel ROIC for 10 x 10 bolometer matrix measurement

Low Noise, Wide Dynamic range Laser Radar Receiver for Pulsed Time-of-Flight Applications

Circuits and Systems Research Unit (CAS), Faculty of Information technology and Electrical Engineering, University of Oulu, Finland

Contact: Aram Baharmast, Juha Kostamovaara
E-mail: aram.baharmast@oulu.fi, juha.kostamovaara@oulu.fi
Technology: AMS 0.35µm C35B4C3
Die size: 1700µm × 1700µm

A Pulsed Time-of-Flight (TOF) laser radar system measures the round-trip transit time of a light pulse that is emitted from the laser transmitter, reflected from the target and then detected by the receiver. In the receiver side, a photodetector (in our case, an Avalanche Photo-Diode (APD)) converts the optical pulse to an electrical signal. Since the velocity of light (c) is well-known and relatively stable under varying environmental conditions, the distance to the target can be calculated from the time lapse.

In a pulsed TOF Lidar, the amplitude of the echo pulse may vary over a dynamic range of 1:10,000 or even more depending on the distance, reflectivity and angle of the target. The systematic deviation of the timing point with amplitude (known as timing walk error) is the main source of inaccuracy in TOF laser radars. On the hand, the precision of this kind of a system is typically limited by the timing jitter which generated by the noise of the receiver. This project presents a hardware technique to detect and measure echo pulses in a wide dynamic range while keeping the walk error (and the noise) low. The basic idea behind the implemented technique is the unipolar-to-bipolar conversion realized at the input of the receiver, as shown in Fig. 1. The arrived unipolar pulse is converted to a bipolar signal using a pulse shaping unit, and then the converted pulse is further amplified through the receiver channel. The first zero crossing point of the converted pulse is picked out as the timing point, and thus the clipping of the signal at high amplitudes (due to the limited dynamic range of the linear amplifiers) does not affect it if the amplifiers recover from the clipping state rapidly enough.

In this project, the front-end pulse shaper is implemented using a "resistor less" LC tank (implemented off-chip) combined with a nonlinear shunt feedback trans-impedance amplifier (TIA). The IC consists of the front-end TIA, a chain of post amplifiers, the timing discriminator and an arming comparator with a digitally tunable threshold voltage. Furthermore, an analog output buffer and offset measurement point are placed to measure the analog properties of the amplified signal through the channel (offset, noise, gain, bandwidth). The output of the receiver channel IC is then fed to a time interval measurement unit (TDC).

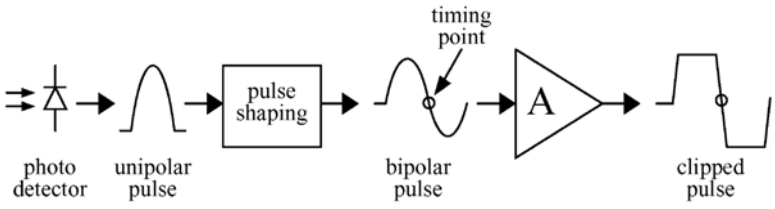


Fig.1: Principle of unipolar -to-bipolar conversion

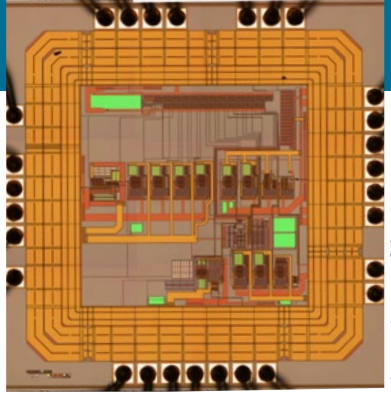


Fig.2: Picture of the fabricated chip

Results

The receiver channel was fabricated in AMS C35B4 0.35 µm standard CMOS technology. The die area, which is shown in Fig.2, is 1.7mm×1.7mm. Fig. 3

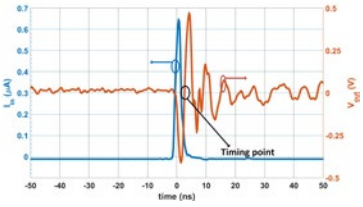


Fig.3: A typical measurement result

shows a sample output measured from the analog buffer. The total measured AC trans-impedance gain at the output of the analog buffer is ~122 dBΩ, and the measured bandwidth is about 200 MHz. The total measured noise at the output of the analog buffer is 70 mV, or ~60 nA RMS when referred to the input. The tests for evaluating other parameters of the receiver chip are still ongoing.

Why Europractice?

Our research unit and the university have used Europractice MPW services for numerous analog and mixed-signal IC designs during the course of the project. These services have been a key enabler for measurements-based research in the field of microelectronic circuit design. The excellent technical support available and the possibility for small volume production and engineering runs are highly appreciated since they produce a convenient link from research to industrial applications.

A Multiband Tuneable LNA with Interference Rejection for 5G Applications

Communication Systems & Networks Group, Department of Electrical and Electronic Engineering, University of Bristol, U.K.

Contact: Dr. Chris Gamlath (Research Associate)
E-mail: Chris.Gamlath@bristol.ac.uk
Technology: IHP SG25H3 BiCMOS process
Die size: 1158um × 1158um

Introduction

The increasing complexity of front-end designs for mobile receivers has been driven by the evolving requirements of communication system standards. One of the greatest challenges to date is the proposal of 5G carrier aggregation for mobile communication which requires the receiver to operate with up to five concurrent channels which can be spaced arbitrarily across multiple bands from 0.4 – 6GHz. This poses a significant challenge for the LNA design particularly to its interference rejection. The shortcomings of the wideband amplifier architecture have led to the investigation of narrowband architectures with tuneable centre frequency across the entire band of operation. Thus out-of-band signals experience higher attenuation and less power is needed to meet the linearity requirements.

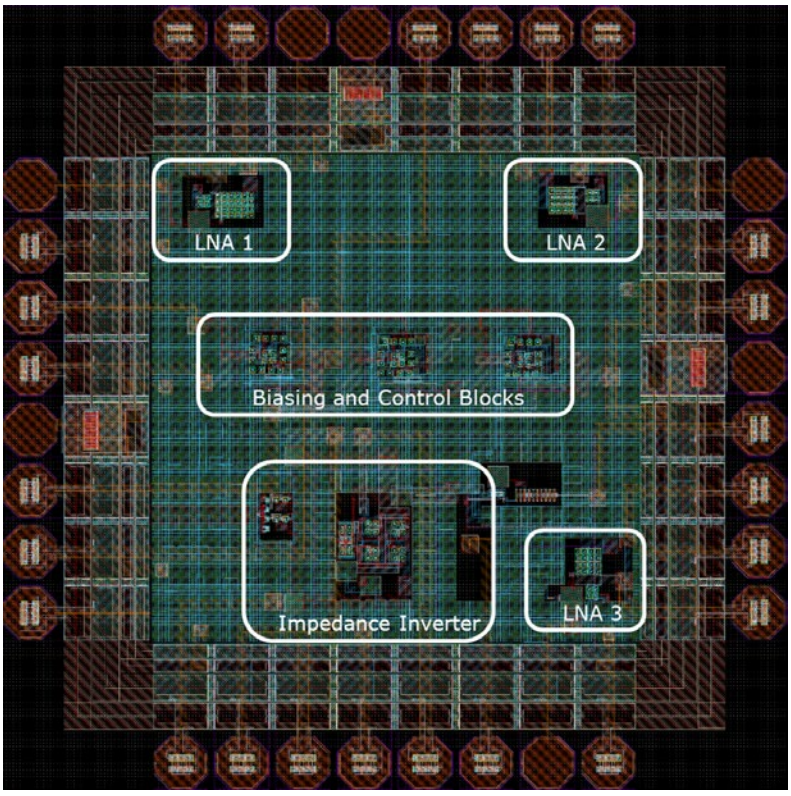


Fig. 2: Layout for the full IC

The current solution of putting together multiple narrowband LNAs in parallel quickly loses its appeal when parameters such as size, cost and power consumption are taken into account. One of the principal goals of this project is to address issues involved with the implementation of tuneable multiband systems in integrated circuit designs.

Description

An LNA prototype with multiband interference rejection filtering operating in the sub 6GHz band was fabricated in the IHP $SG_{25}H_3$ BiCMOS process. The sharp high-Q filtering for each channel was implemented using N-Path filters implemented off-chip [1]. This was combined with wideband on-chip impedance inverters to form the multiple concurrent channels. The high fT transistors available with the $SG_{25}H_3$ process (up to 110GHz) were used to create wideband impedance inverters up to 10GHz. The die area for the LNA was less than 0.04mm² with power consumption of 25mW. Each impedance inverter occupied a die area of 0.2mm² with a power consumption of less than 5mW. The final design calls for only a single LNA with the number of impedance inverters equal to the number of concurrent channels plus one. For 5 concurrent channels this amounts to a power saving of greater than 60% compared with duplicating individual LNAs. This type of architecture is mainly targeted at mobile receivers where power consumption is a priority [2].

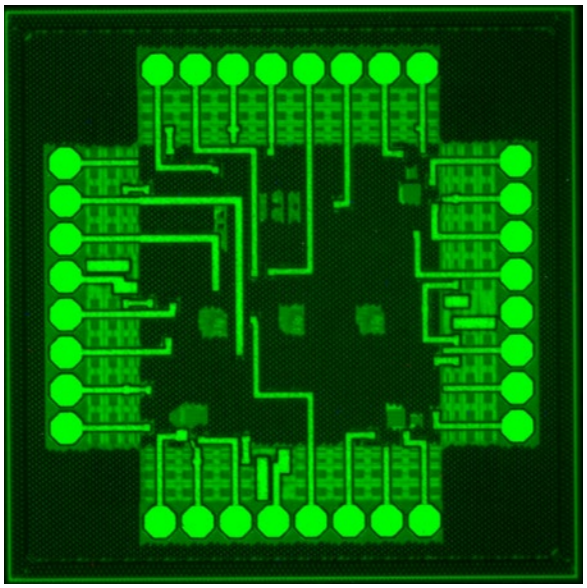


Fig. 3: A microscope photograph of the IC bare die

Results

The measured results for the fabricated device are shown in Fig. 1. This shows a less than 2dB noise figure for sub 1GHz and less than 3dB for sub 2GHz band. Although noise figure could be optimized further with this process down to below 1dB, the combination of the LNA with the interference rejection filter incurs a noise penalty. Further testing of linearity performance and OFDM channel performance is still ongoing and has not yet been completed. The layout for the full IC is shown in Fig. 2. Three separate versions of the LNA with some variation were implemented for performance evaluation. Where possible the large transistors were implemented using common centroid techniques. A microscope photograph of the IC bare die in Fig. 3.

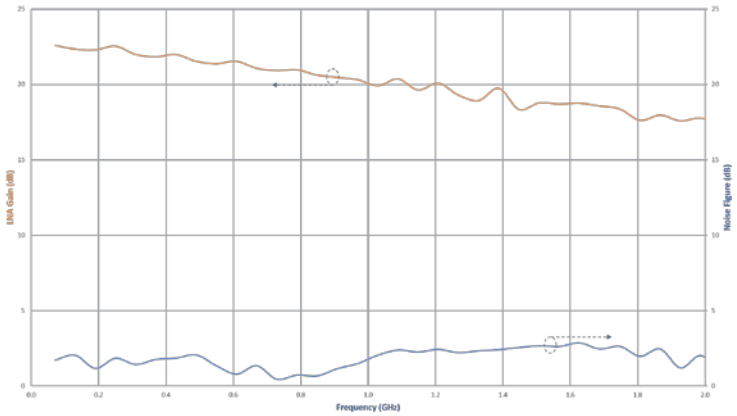


Fig. 1: Measurements on the fabricated device

References

[1] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer and B. Nauta, "Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification," in IEEE Journal of Solid-State Circuits, vol. 46, no. 5, pp. 998-1010, May 2011. doi: 10.1109/JSSC.2011.2117010

[2] C. Gamlath, E. Arabi and K. A. Morris, "A design technique for concurrent multiband tunable loads from 0.4–6GHz with independent Q tuning," 2017 IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpar, 2017, pp. 980-983. doi: 10.1109/APMC.2017.8251615

Why Europractice?

Europractice MPW scheme offers the most cost effective solution for European Universities that do not have strong links with foundry partners. It allows access to state-of-the-art IC processes at a fraction of the cost compared with commercial MPWs. This allows more IC based academic projects to be funded and an expansion of the research literature which is also useful for commercial designers. The University of Bristol Electrical and Electronic Engineering and the Photonics Department in Physics have participated in many Tapeouts via Europractice during the past decade. We have found Europractice to provide a professional and efficient service that is well suited to our needs.

Acknowledgements

The Engineering and Physical Sciences Research Council (EPSRC) U.K. is sincerely acknowledged. This work was made possible by the Frequency Agile Radio (FARAD) project, EPSRC Reference: EP/M013723/1.

Front-End IP Block for Array of X-ray Silicon Drift Detectors

High Energy Astrophysics Department, Space Research Institute (IKI), Moscow, Russia

Contact: Vasiliy Levin
E-mail: vvl@iki.rssi.ru
Technology: X-FAB XT018 0.18 µm HV SOI CMOS MET3/4/MID/THK
Die size: 1520µm × 1520µm

Description and application

Now many astrophysical space projects use the Silicon Drift Detectors (SDD) as a main sensitive element for X-ray telescopes and spectrometers. The advantages of SDD is a high energy resolution (near 130 eV at 5,89 keV), variety of the sizes from 1 to 100 mm², operation at relatively "warm" temperatures as high as -20 °C and ability to work with high counts rate. Especially SDD suited for neutron stars and X-ray pulsars exploration, where high energy and sub microseconds timing resolution required.

The goal of our project is a creation of IP block of spectrometric channel with low noise and a low power consumption for SDD signals processing. Designed IP block (Fig. 1) consists of regulated current source (RCS), charge-sensitive amplifier (CSA), shaping amplifier with additional differentiator (SHAD), peak detect and sample and hold unit (PDSH). Parameters of all blocks adjusted by digital control signals. The current source provide the DC bias of the first amplification JFET, situated in the SDD die. The current regulated by 3 bits from 50 to 300 µA. Charge-sensitive amplifier integrate the detector current and produce voltage step, proportional to the energy of registered X-ray photon. Shaping amplifier enhance signal to noise ratio, amplify CSA signal, reject DC part of the signal and produce smooth output pulse, convenient for peak detect circuit. The shaping amplifier has a CR-2xRC structure (one differentiation and two integration). This structure selected as compromise between noise suppression and power consumption. The shaping time (CR product) adjusted in six steps: 0.6, 1.1, 1.6, 2.1, 4.1 and 6.2 µs. Additional differentiator used for "zero crossing" detector to produce time mark with low jitter.

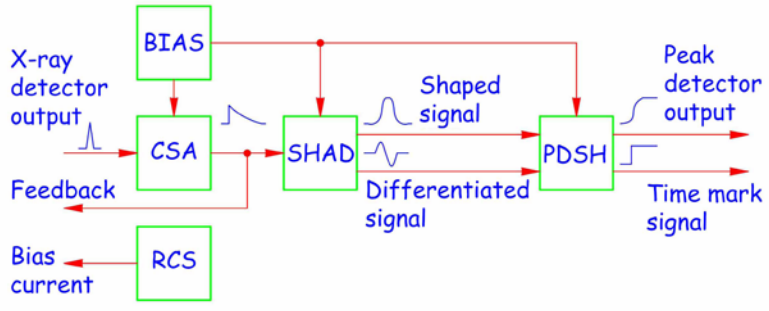


Fig. 1: Structure of spectrometric channel

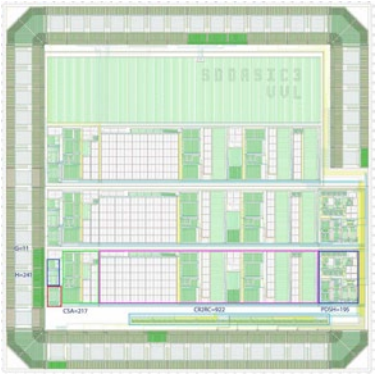


Fig. 2: SDDASIC3 layout

The spectrometric channel consume 2.2 mW from +3.3 V. The charge sensitivity with typical detector is 57 mV/keV. The dynamic range is equal to 31 keV. Simulated equivalent noise charge of the channel is 4.8 e^- (root mean square).

The length of our IP block is relatively long (the size is 1334x241 µm). To fit our design in a single mini@sic block we break the power supply rings and optimize power supply pads arrangement (Fig. 2). Using this technic, we fit two full spectrometric channels and one channel divided by blocks on the die.

Why Europractice?

Europractice mini@sic program ideally suited for IP blocks prototyping. Very important that mini@sic runs support all process options are used in general MPW runs. Additional advantage of mini@sic is ability to connect two blocks together and prototype long designs. Europractice make a world of semiconductors technologies more available.

Acknowledgement

This research has been supported by the grant 14.W03.31.0021 of the Ministry of Education and Science of the Russian Federation.

MultiSense: Ultra-Thin Reconfigurable Voltage and Capacitance Readout ASIC

Organization: Institut für Mikroelektronik Stuttgart – IMS CHIPS, Stuttgart, Germany

Contact: Mourad Elsobky, Zili Yu, Thomas Deuble, Joachim N. Burghartz
E-mail: elsobky@ims-chips.de
Technology: XH018 0.18µ HV NVM CMOS E-FLASH
Die size: 1.52mm × 1.52mm

Description

This prototype serves as a reconfigurable voltage and capacitance readout ASIC. It contains different analog and mixed signal blocks namely amplifiers, voltage reference, ADC and biasing circuitry in addition to the digital controller and SPI communication blocks. The chip design is flexible enough to allow for the characterization of the individual blocks yet still function as a whole system for early demonstrations. The signal chain starts with a switched capacitor programmable gain amplifier, which can be configured in either capacitance or voltage readout modes. This offset compensated amplifier is designed to interface with external capacitive sensors (1 fF – 32 pF) as well the on-chip bandgap-based temperature sensor (-40°C – 85°C with 0.2°C step). A 10-bit SAR ADC is implemented along with on-chip reference, driver and digital control circuits. The analog and digital cores use 1.8 V supplies while the I/O circuitry uses a 3.3 V supply. This design flexibility and rapid prototyping (6 months, 1 engineer) was enabled by the support from Europractice and the maturity of the XFAB technology library.

One application for this ASIC is the integration in a System-in-Foil (SiF), where multiple electronic components are combined into a flexible substrate. The SiF includes silicon chips, such as microcontrollers and sensor readout chips as well as organic electronics, antennas and on-foil sensors[1]. The silicon chips are back-thinned to less than 50 µm thickness and then embedded in a polymer package using a foil assembly technology called ChipFilm Patch (CFP) [2]. Furthermore,

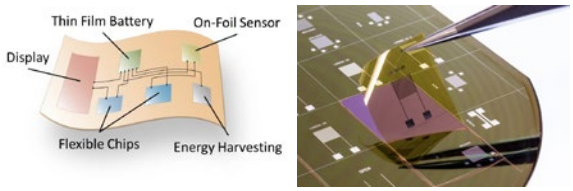


Fig. 2: SiF schematic including different flexible components such as on-foil humidity sensor [1-3]

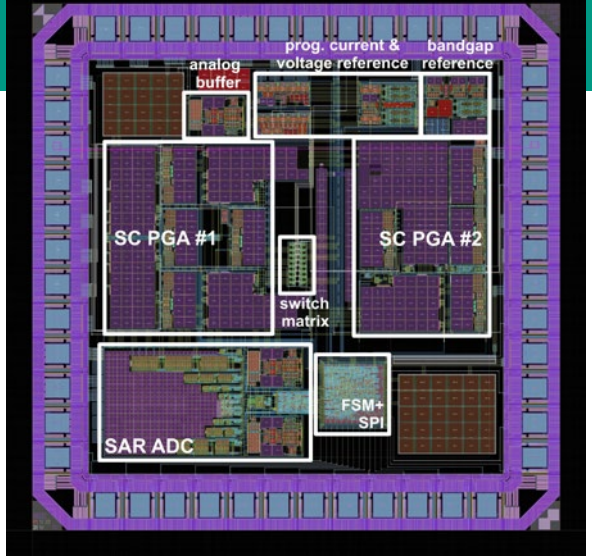


Fig. 1: The fabricated ASIC layout with die size of 1.52 x 1.52 mm²

sensor structures are fabricated on the foil surface either by printing or by using standard lithography techniques [3].

Why Europractice?

This tapeout was the first time for IMS CHIPS to participate in the mini@sic MPW run organized by Europractice. For a design idea that requires a proof-of-concept hardware, mini@asic run is our best candidate. We have chosen the low-cost and mature 0.18µ CMOS technology since our target application was low to medium speed sensor readout circuits. However we are also interested to access the advanced technology nodes technologies through Europractice. It is remarkable how Europractice makes such technologies available. In addition, Europractice representatives have shown a consistent support and professionalism starting from the early design kit installation until the tapeout and chip delivery.

Acknowledgement

This work was funded by the Ministerium für Wirtschaft, Arbeit und Wohnungsbau Baden-Württemberg and the German Federal Ministry of Education and Research (BMBF) as a part of the BW-CPS (AZ 3-4332.62-HSG/77) and ParsiFAl4.0 (#16ES0435) projects, respectively.

References

[1] Elsobky, M.; Mahsereci, Y.; Yu, Z.; Richter, H.; Burghartz, J. N.; Keck, J.; Klauk, H.; Zschieschang, U. Ultra-Thin Smart Electronic Skin Based on Hybrid System-in-Foil Concept Combining Three Flexible Electronics Technologies, Electron. Lett. 2018, 54, 338-340, DOI: 10.1049/el.2017.4682

[2] Alavi, G.; Sailer, H.; Albrecht, B.; Harendt, C.; Burghartz, J. N.; Adaptive Layout Technique for Microhybrid Integration of Chip-Film Patch, IEEE Transactions on Components, Packaging and Manufacturing Technology 2018, 8, 802-810, DOI: 10.1109/TCPMT.2018.2818762

[3] Elsobky, M.; Albrecht, B.; Richter, H.; Burghartz, J. N.; Ganter, P.; Szendrei, K.; Lotsch, B. V. Ultra-Thin Relative Humidity Sensors for Hybrid System-in-Foil Applications. in Proc. of IEEE Sensors 2017, DOI: 10.1109/ICSENS.2017.8234298

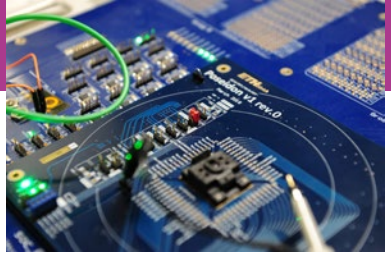


Fig. 3: Photo of chip on the Advantest SoCV93000 tester

Poseidon: A test chip for energy efficient processing solutions in GF22FDX

Integrated Systems Laboratory, ETH Zurich, Switzerland

Contact: Luca Benini, Frank K. Gürkaynak
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Technology: GLOBALFOUNDRIES 22nm FDSOI
Chip size: 3000µm × 3000µm

Description

Poseidon, is our first ASIC in 22nm technology, and consists of three independent parts which also inspired the name. Each part has its own power supply and can be controlled independently. The body bias nets were routed to external power pads allowing us to experiment different body biasing techniques. Main logic was implemented using 8T LVT/SLVT standard cells and memories from Invecas, and custom designed FLL circuits were used to generate high-speed internal clocks up to 2GHz from an external 32kHz crystal oscillator.

The first part called Quentin is a complete single-core 32bit micro-controller system based on our open source PULP platform. It contains our RISC-V based 32-bit RI5CY core with an FPU (RV32ICMF), 512kBytes of memory and a convolutional hardware accelerator.
Measurements have shown that at room temperature the most energy efficient operating point it achieved 300 MOps/mW. Using 1.4V forward body biasing the chip was able to run at 938MHz at 0.8V VDD (room temp)

The second part of the chip, contained Kerbin, the first silicon implementation of our 64bit RISC-V core Ariane (RV64ICMX). This part contains just the core and 16 kByte of instruction and 32 kBytes of data cache. The I/O and further memory is shared with the aforementioned Quentin system. The 64 bit core was clocked up to 1.5GHz (at 1.0V, room temperature). It is important to note that the source code for both parts are available using a permissive open source license on our GitHub page (**https://github.com/pulp-platform**)

The third part, Hyperdrive, is independent of the other two parts and contains a standalone neural network accelerator. In this I/O optimized implementation suitable for tiling into a systolic array, 6.5 Mbit on chip memory is used to keep feature maps in 16bit floating point format, while binary weights are streamed into the chip to be processed in parallel. Including the I/Os, Hyperdrive achieves 5.8 TOps/s/W while running at 0.65V supply.

Altogether the three parts of Poseidon have allowed us to explore a number of options to optimize energy efficiency in modern computing systems, and have given us new directions for our future ASICs.

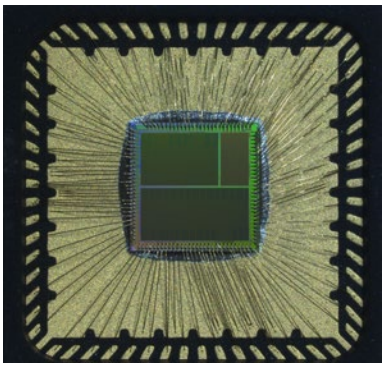

Fig.2: Die in package photo

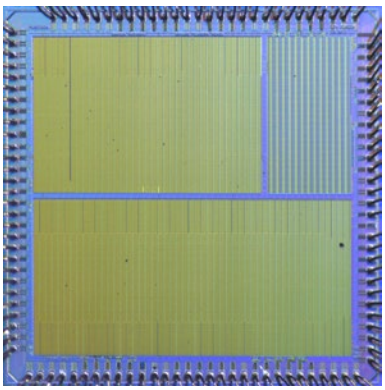

Fig.1: Die photo

Why Europractice?

For our research in energy-efficient processing systems it is important to get access to newer technology nodes, so that we can take advantage of the opportunities presented by modern nodes in our research.
Europractice has enabled us access to the GLOBALFOUNDRIES 22nm FDX node, at the time of design, the most advanced node available to research institutes without a direct agreement with a technology provider. The setup of a new technology node is always additional work, and more modern technologies such as GF22FDX require more work than some of the older technology nodes we have used, so we were very happy to work with Europratice, which has helped us in transitioning to this node and supported us throughout the tape out process.

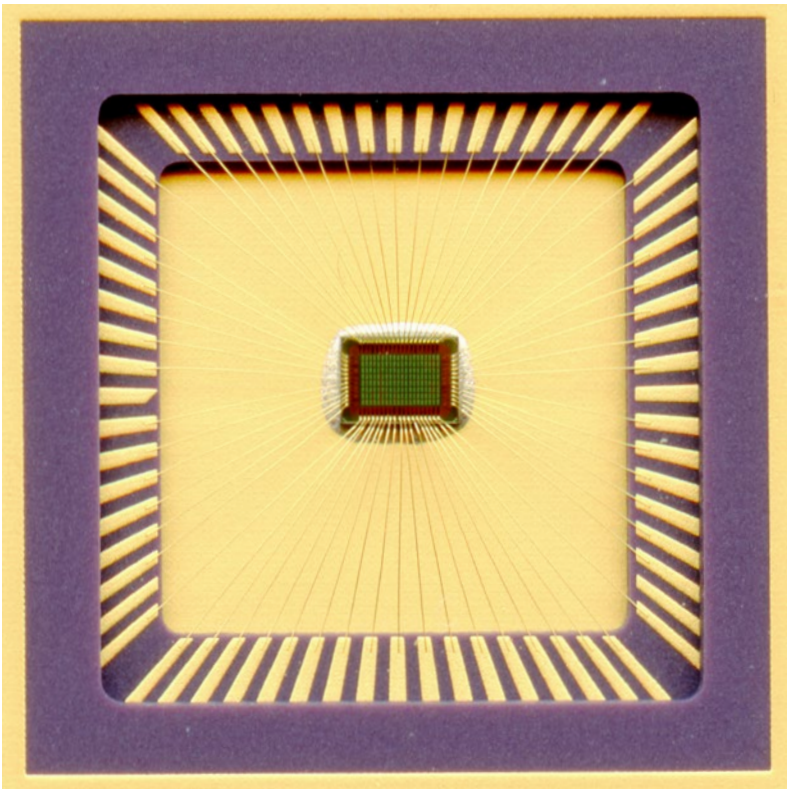

Fig.2: Picture of wire-bonded die

Ultra-low power OTA with linear VTC

Institute of Microelectronics and Optoelectronics,
Warsaw University of Technology, Warsaw, Poland

Contact: Prof. Wieslaw Kuzmicz
E-mail: wbk@imio.pw.edu.pl
Technology: GLOBALFOUNDRIES 22nm FDSOI
Circuit size: 167.5µm × 165.4µm (without IO pads)

Description

This Ultra-low power Operational Transconductance Amplifier with linear Voltage Transfer Characteristics is one of five different experimental analog and mixed-mode blocks exploring circuit solutions possible in FDSOI technologies only. FDSOI-specific architecture of this amplifier includes internal negative feedback applied to the body of input transistors.

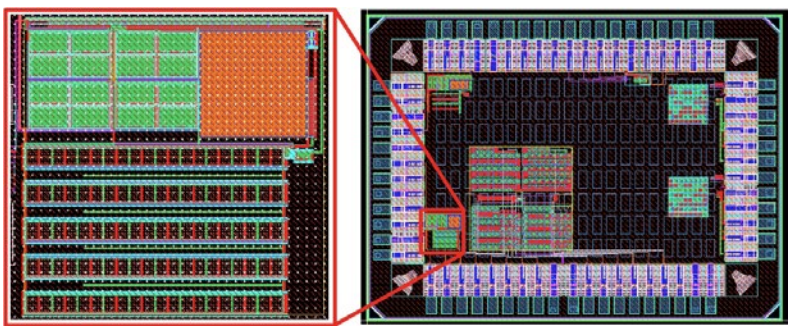

Fig. 1: Chip and circuit layout

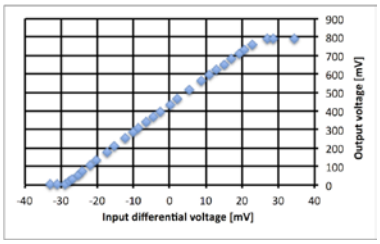

Fig. 3: Voltage transfer curve of the amplifier

This results in perfectly linear voltage transfer curve. The voltage gain is from 15 dB to 50 dB, adjustable by two external resistors. Power supply voltage: 0.8V, maximum undistorted amplitude at the output: 390 mV, bandwidth from DC to several kHz depending on load capacitance and external feedback, power consumption below 1 µW. This amplifier may find applications for amplification of low frequency signals in ultra-low power devices and systems such as e.g. amplifiers for sensors in IoT devices or medical implantable devices.

Why Europractice?

We have been using Europractice MPW service since 1995, always benefiting from wide selection of technologies and friendly, helpful technical support. Mini@sic prototyping in GLOBALFOUNDRIES 22FDX technology, the most advanced FDSOI CMOS technology, is now available from Europractice only.

Acknowledgement

This work has been funded by THINGS2DO, the JU ECSEL project no. 621221.

Testchip for Performance Characterization of Blocks for a Multi-Channel Mixed-Signal System

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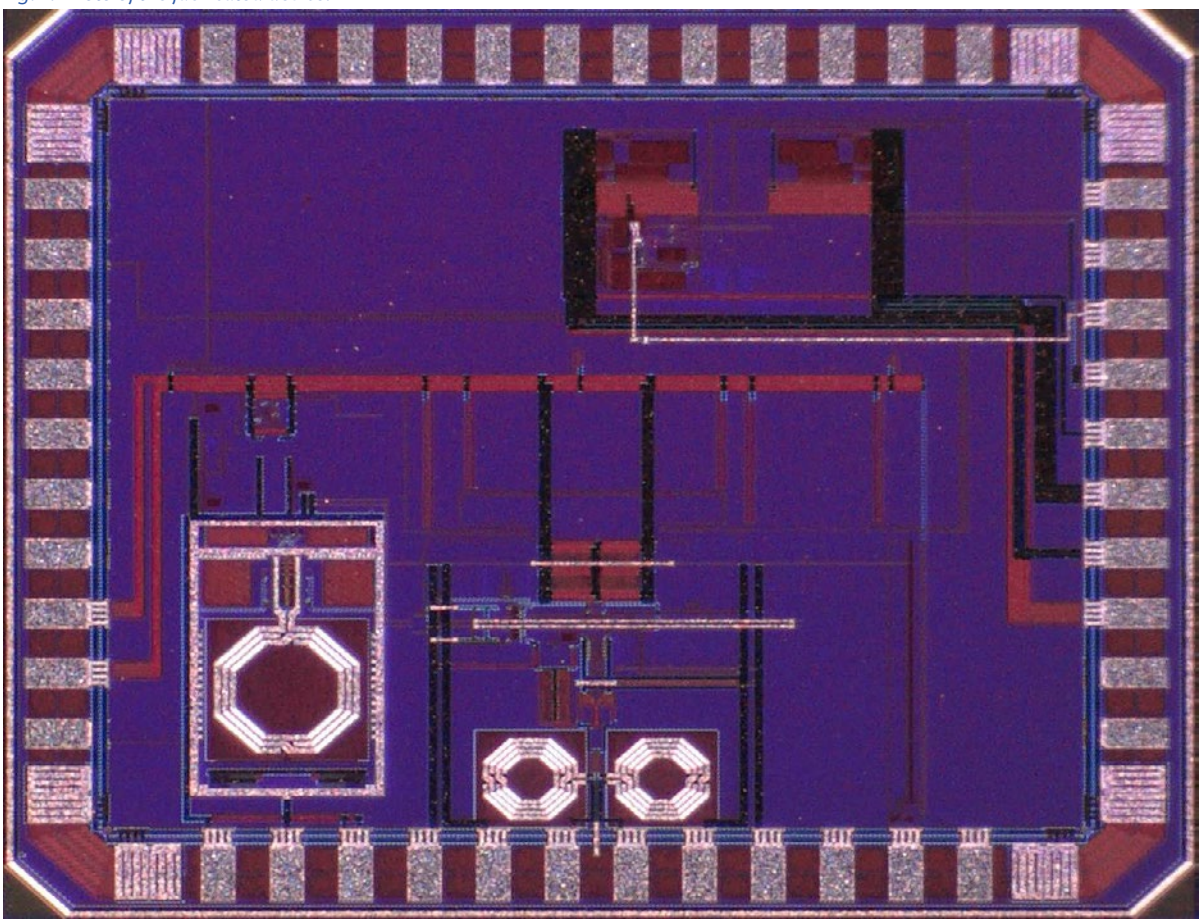
Fraunhofer Institute for Integrated Circuits IIS, Erlangen, Germany

Contacts: Harald Neubauer, Dr. Matthias Oberst
E-mail: harald.neubauer@iis.fraunhofer.de, matthias.oberst@iis.fraunhofer.de
Technology: GLOBALFOUNDRIES 55LPe
Die size: 1.7mm × 1.5mm

Description

The device contains a PLL, a CML-Driver, a current input amplifier, an ADC and digital configuration capabilities. The PLL generates a 4 GHz reference clock for the digital CML output drivers with 8 Gb/s data rate. The amplifier uses a charge-transfer configuration for current-voltage conversion. It has 16 gain modes and its feedback capacitor acts as sampling capacitor for the following ADC. Two caps are used in ping-pong mode. The ADC uses a SAR topology with a 9 bit capacitor DAC including 1 bit redundancy. The device was fabricated to test the performance critical blocks of a multi-channel mixed-signal system. The final system has more than 1000 channels comprising of the tested amplifier and the ADC. More than 100 channels will be active and generate digital data of more than 100 Gb/s.

Fig. 1: Photo of the fabricated device.



During physical evaluation we found a 88 aF parasitic capacitor reducing the ADC's ENOB by 1 bit. This saved one full mask set engineering run reprocessing for the multi-channel mixed-signal system. The amplifier was not used in the final design because of changes in specification. The PLL and the CML driver worked like specified and were used as designed for this device.
The final multi-channel system chip was taped out and is currently in production.

Why Europractice?

The Europractice service offers affordable prototyping and testing for various projects. They offer a single point of contact for various foundries with excellent support for PDKs and tapeout procedures. In addition, they offer access to modern nanometer scale technologies.

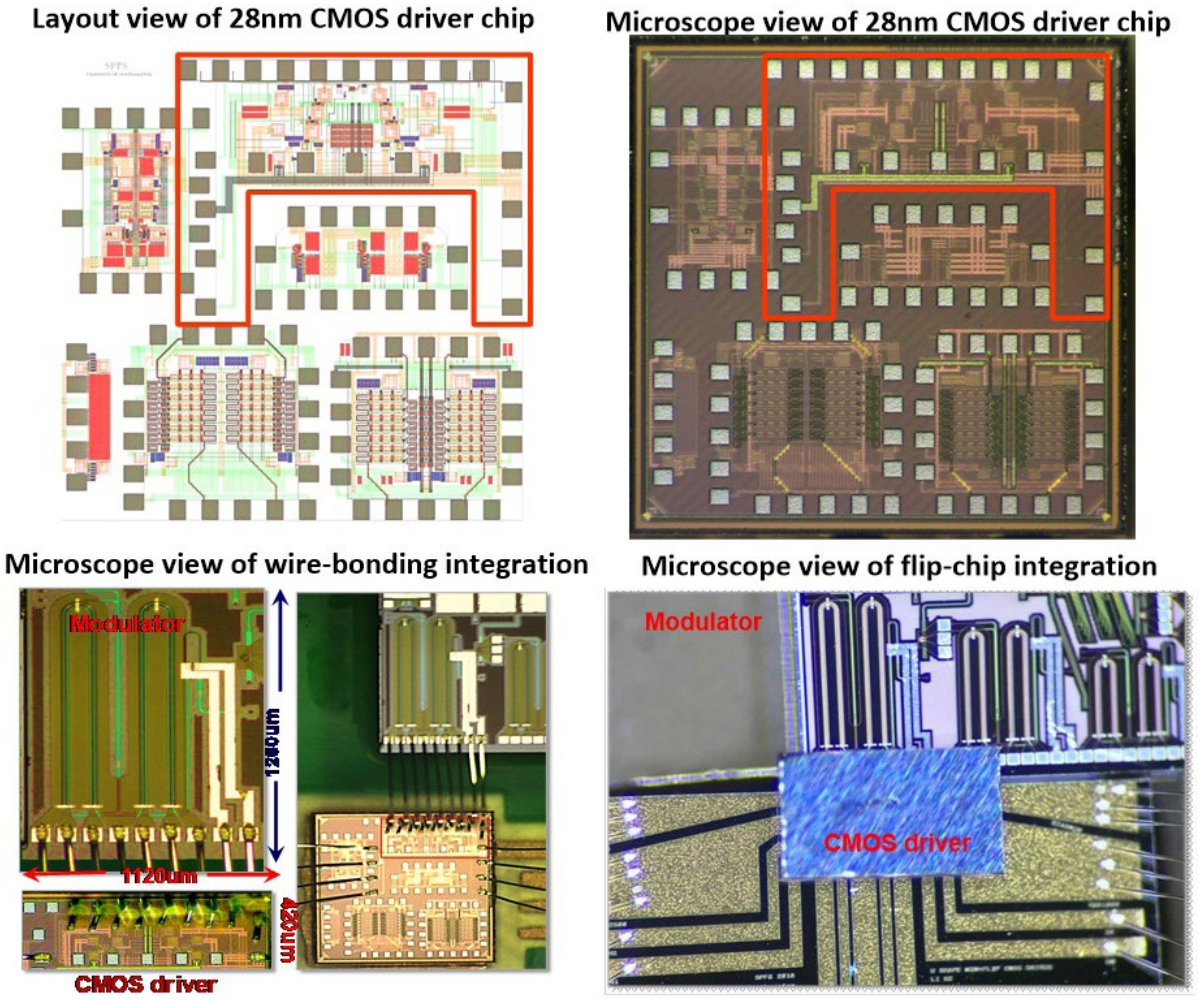


Fig.1 Layout and microscope view of the design with different integration approaches

Co-design of electronics and photonics components for Silicon Photonics transmitters

University of Southampton, UK

Contact: Dr. Ke Li, Dr. David Thomson, Prof. Graham Reed
E-mail: kl@ecs.soton.ac.uk, D.Thomson@soton.ac.uk, g.reed@soton.ac.uk
Technology: TSMC 28nm HPL + Silicon Photonics
Die size: 1570µm × 1570µm

Description

The interest in developing silicon photonic interconnect to meet the growing demands of data processing speeds and bandwidths has increased over the last decade. The development of the modulator which is one of the most important components of the interconnect has received major focus. As silicon has a weak electrooptic effect, alternate approaches such as the plasma dispersion effect has been used to achieve modulation in silicon with significant success. While there have been significant research efforts in developing standalone silicon optical modulators, work on integrating those with electronics is limited, which is necessary for the practical implementation of silicon optical interconnects. So far, work on silicon photonics–electronics integration is mostly limited to physical coupling between photonic and electronic devices such as wire–bonding or flip-chip bonding. In this work (DOI: 10.1109/ECOC.2018.8535212), we present an alternate approach where photonic and electronic devices are co-designed synergistically in terms of power efficiency, operation speed, footprint and signal integrity.

To justify the advantages of this concept, we have demonstrated a silicon photonics transmitter, which incorporates a co-designed depletion-type silicon Mach-Zehnder modulator (Si MZM) and a 28nm Complementary Metal–Oxide–Semiconductor (CMOS) driver. Thanks to the technique support from Europractice, we

got tremendous success with our first time TSMC 28nm HKMG-CMOS tape-out via the mini@sic programme. These 28nm CMOS driver chips are then integrated (both wire-bonding and flip-chip bonding) with silicon photonics modulator at nanofabrication center, Optoelectronics Research Centre (ORC), University of Southampton.

Simply based on the wire-bonding approach, the proposed transmitter can operate up to 22Gb/s with the CMOS driver power efficiency at 1.5pJ/bit, with a 3.0dB extinction ratio maintained. Further measurement results based on the flip-chip bonding approach have demonstrated operation speed up to 40Gb/s with the CMOS driver power efficiency at 2.46pJ/bit, with a clear eye-open and 2.9dB extinction ratio.

Why Europractice?

The University of Southampton has worked with Europractice on TSMC fabrication for many years. We have benefitted from Europractice's excellent technical support for CMOS chip submission. Europractice has given us affordable access to frequent multi-project wafer fabrication runs.

Acknowledgement

The financial support of the EPSRC, UK under the grants EP/L00044X/1 (Silicon Photonics for Future Systems) and EP/L021129/1(CORNERSTONE: Capability for OptoelectRoNics, mEtamateRialS, nanoTechnOlogy aNd sEnsing) is gratefully acknowledged. Dr. David Thomson gratefully acknowledges funding from the Royal Society for his University Research Fellowship.

Low Power High precision SAR ADC

MCCI, Tyndall Institute of Technology, Lee Maltings, Dyke Parade, Cork, Ireland

Contacts: Dr. Ivan O' Connell, Dr. Daniel O'Hare, Dr. Gerardo Salgado, Subhash Chevella, Anita Schuler
E-mail: ivan.oconnell@mcci.ie
Technology: TSMC 28nm
Die size: 1520µm × 1520µm

Description

Successive Approximation Register (SAR) ADCs utilise the advantages of Digital CMOS to produce the lowest power Analog to Digital Converters (ADCs). However the best performing SAR ADCs from a power point of view have resolutions around 10bits. Traditionally the highest resolution ADCs have been Delta Sigma ADCs using switched capacitors. Our ADC takes advantage of the speed benefits of 28nm CMOS to achieve a high resolution 15ENOB ADC. We used active noise shaping to avoid kT/C noise limiting the ADC performance. To achieve lower noise in the active noise shaping circuits in open-loop, we used slewing rather than the conventional settling stages. The ADC input is sampled onto a 10bit capacitor SAR ADC. The ADC converts this sampled signal into a 10 bit word and the remainder voltage is kept as a residue signal. This residue signal is applied to the loop filter and the output of the filter is subtracted from future

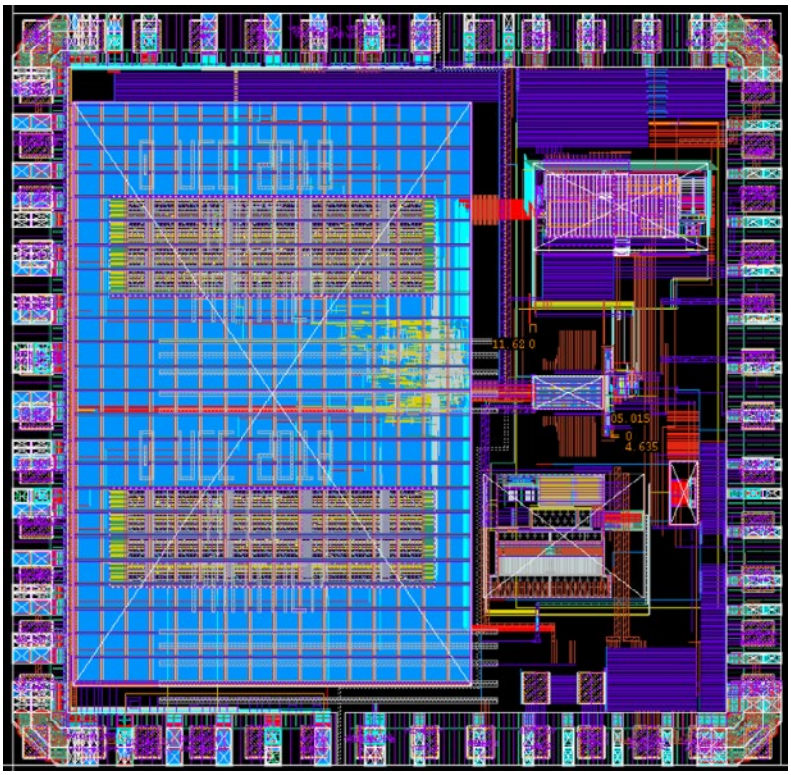


Fig. 1: Layout of the designed circuit

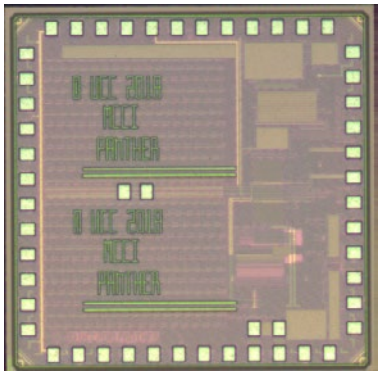


Fig.2: Photo of the fabricated ADC.

ADC conversions. This produces an oversampled ADC output with shaped quantisation and comparator thermal noise. We then used Digital Filtering to convert the 10bit output data into a 15ENOB signal at a lower data rate. The 0.9V and 1.2V supply voltages used in this ADC make it suitable for embedded applications. Operating this ADC at a higher speed (rate) allowed smaller sampling capacitors to be used. This resulted in a low area ADC which is suitable for embedded applications.

Why Europractice?

Europractice has given us PDK and foundry access to state-of-the-art semiconductor processes of TSMC and other manufacturers. We got good technical support from Europractice engineers. All technical questions were timely addressed and when necessary their resolution was escalated to foundry technical team. We have also benefitted from Europractice's support for dummy/density fill, chip submission and chip packaging processes. Finally, Europractice has given us affordable access to frequent multi-project wafer fabrication runs and also to mini@sic shuttles.

Acknowledgement

The fabrication of this ADC was sponsored by Enterprise Ireland.

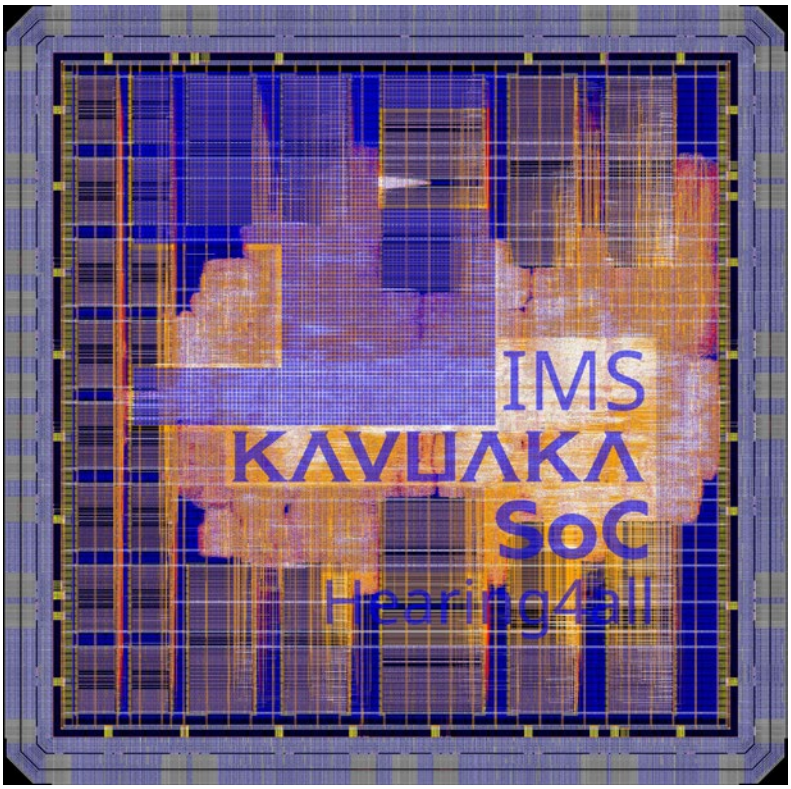


Fig.1: Layout view of KAVUAKA

The KAVUAKA Hearing Aid Processor

Institute of Microelectronic Systems, Leibniz Universität Hannover, Germany

Contact: Dipl.-Ing. Lukas Gerlach, Jun.-Prof. Dr.-Ing. Guillermo Payá Vayá, Prof. Dr.-Ing. Holger Blume
E-mail: {gerlach, guipava, blume}@ims.uni-hannover.de
Technology: TSMC 40nm LP 1P8M5X2Z
Die size: 1920µm × 1920µm

Description

Future hearing aids should become more intelligent, e.g. should be able to detect and filter out relevant speakers in complex acoustic environments. The goal is to further improve the hearing ability of the individual hearing aid users. Computationally complex algorithms are required for this task. We studied how the processor architecture of a hearing aid system can be designed and optimized on the basis hearing aid algorithms, so that such a hearing aid system can provide the required computing power under the strict power and die size constraints.

The result of this work is the hearing aid processor KAVUAKA, which is an application specific instruction set

processor (ASIP). The generic baseline VLIW processor architecture was adapted and optimized using state-of-the-art hearing aid algorithms like sound

source localization, noise reduction, beamformer and compression. Specialized and complex instructions were added to the basic instruction set. Noteworthy extensions are a multiplication and addition unit (MAC) that can compute both real and complex numbers, architectures for power reduction during register accesses, and an audio interface for low latency. During the development phase of KAVUAKA, many design space explorations including netlist simulations based on the target ASIC technology were performed. The results are used for further gate-level power reduction techniques.

The final integrated hearing aid system-on-chip consists of 4 KAVUAKA processor cores and 10 co-processors.

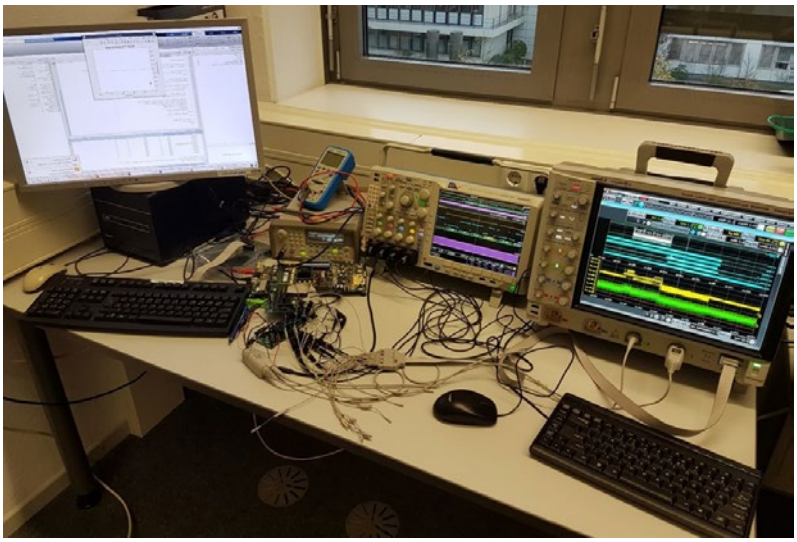


Fig 3.: Lab setup for verification and power measurements

Each of these processors and co-processors is equipped with different hardware features and a different data path width of 24 bit, 32 bit, 48 bit and 64 bit. The processors are organized in two clusters, which share memories, an audio interface, co-processors and serial interfaces. Each component can be activated separately or simultaneously to increase computing power or minimize power dissipation. This feature enables power consumption measurements for different hearing aid system configurations. The measured average power consumption is less than 1 mW per core. The area is less than 1 mm² per core.

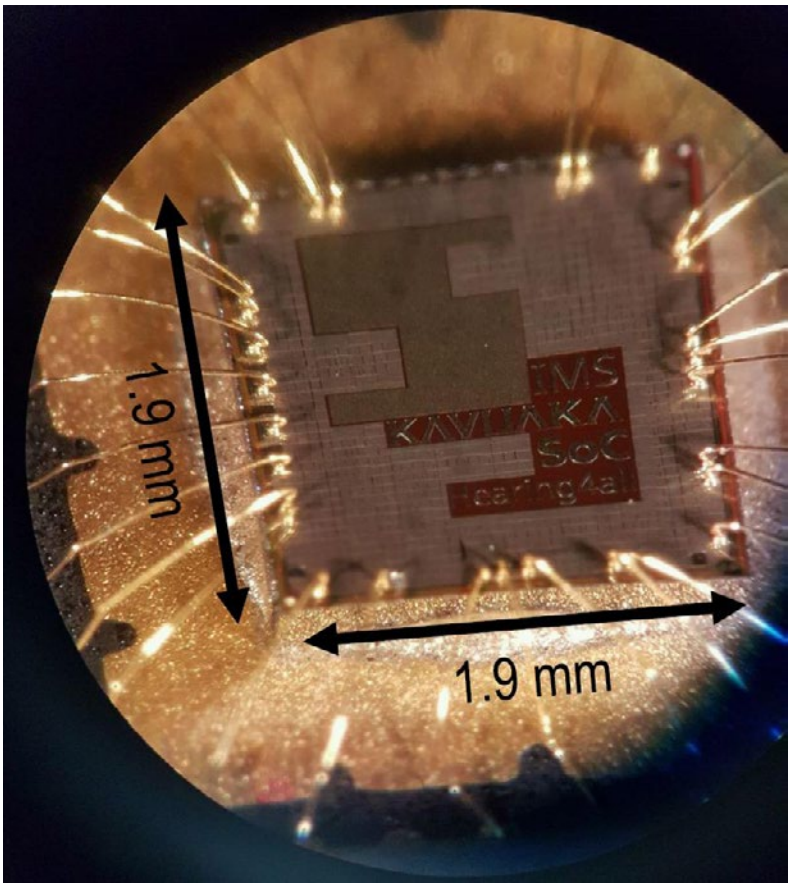


Fig.2: Microscope view of the fabricated chip

Why Europractice?

Europractice gave us the opportunity to integrate our hearing aid as an application-specific integrated circuit. Without the continuous support from Europractice this would not have been possible. With the mini@sic program for IC prototyping, we were able to reach our goal without long waiting times and at favourable conditions.

Acknowledgement

This work was funded by the DFG (Cluster of Excellence 1077/1 Hearing4All (http://hearing4all.eu)).

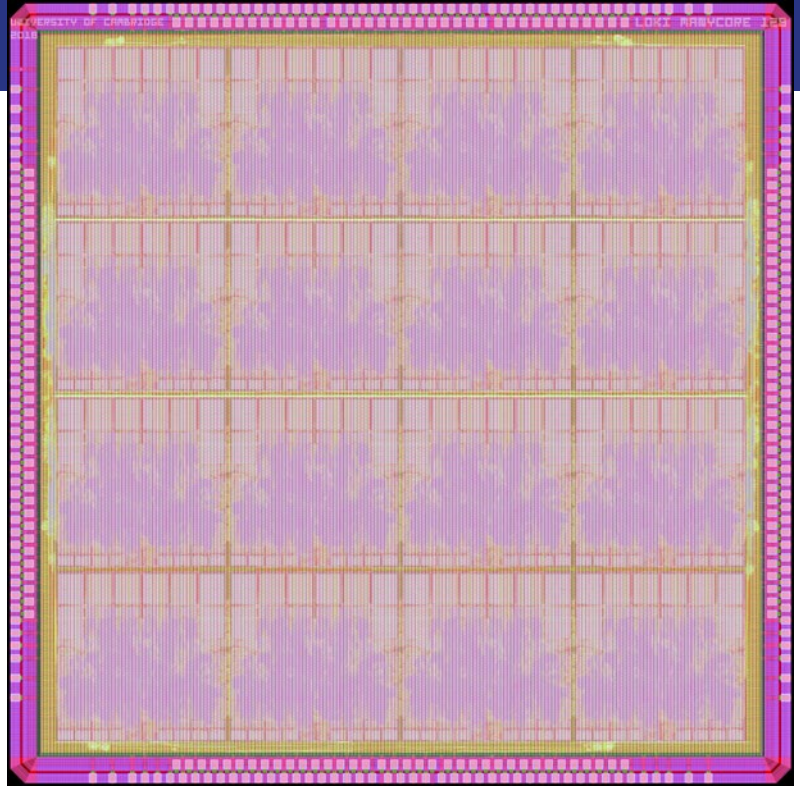


Fig.1: Layout view of the Loki chip

Loki: a 128-core processor

Department of Computer Science and Technology, University of Cambridge

Contact: Dr. Daniel Bates, Alex Bradbury, Alex Chadwick, Dr Yousun Ko, Dr. Robert Mullins
E-mail: Robert.Mullins@cl.cam.ac.uk
Technology: TSMC 40nm LP Cu 1P10M 1.1/2.5V
Transistor Count: 122 million
Die Size: 4.95mm × 4.95mm

Introduction

The Loki test chip is part of an ERC funded project exploring the design of massively-parallel single-chip architectures. The architecture interconnects a large number of individual processor cores much more tightly than traditional approaches. This provides a high-degree of control and flexibility when mapping programs to the cores. Individual cores can cooperate in a wide variety of different ways to form different execution patterns. The memory system is also highly configurable, allowing scratchpads and caches to be sized and configured as required, and specialised cache hierarchies to be created. The ability to dedicate or specialise individual cores and memories to particular tasks shares some similarities with FPGAs.

Description

Our test chip consists of an array of 4x4 tiles each containing 8 cores and 64KB of SRAM. In total the chip contains 128-cores and 1MB of on-chip memory. The cores were designed at Cambridge and implement our own communication-centric ISA. They are supported by our own LLVM compiler backend port.

The tiles are interconnected through the use of multiple on-chip interconnection networks, carrying both memory traffic and direct core-to-core messages. Each tile provides a number of crossbars to connect each core to 8 local SRAM banks. Multiple buses are also provided to permit direct core-to-core communication (including support for multicasting).

A range of applications have been prototyped and explored including convolution neural networks exploiting sparse data storage and computation. The test chip will enable us to make direct comparisons to other platforms in terms of performance and power consumption.

The design was prototyped in TSMC's 40LP process. Exploratory synthesis and place-and-route was performed at Cambridge. Hand-off to the IMEC design team was at the netlist level. The IMEC team completed the physical design work and backend tasks. The chip was submitted to the June 2018 MPW run. Packaged chips were received in December 2018 and the bring-up and test process began in January 2019.

We made extensive use of the BaseJump open-source BGA package substrate and motherboards, making use of both DoubleTrouble and finally RealTrouble (http://bjump.org). The test chips are packaged using a 352-pin wirebond BGA package (140 signal I/Os and 192 power and ground pins, 332 bond wires). Off chip communication is provided via 4 source synchronous double data rate interfaces.

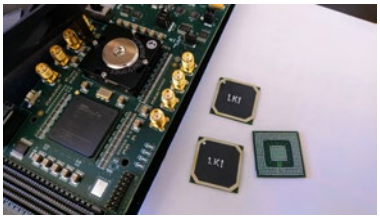


Fig.2: Packaged Loki chips and BaseJump motherboard (FPGA and BGA socket)

Results

Preliminary results indicate that everything is working as expected. We have been able to run instructions on all 128 cores. We are continuing to build infrastructure to more fully test the chip. We will hopefully publish a full set of results soon, please feel free to contact us for more information.

Why Europractice?

The Europractice MPW service provided us with affordable access to the modern fabrication technology required for our project. The expertise of the Europractice/IMEC team was also a crucial component in the success of the project. A research project such as this would simply not be possible without the services Europractice provides.

Acknowledgements

This work is funded by the European Research Council grant number 306386. The PI would like to thank the team at the ERC for all of their support throughout the project.

We would like to thank everyone in the IMEC team who worked with us, including Mustafa Haluk Cologlu who worked on the physical design, for their high-quality support and attention to detail. We are also indebted to Prof. Michael Taylor and his Bespoke Silicon Group at the University of Washington for making their BaseJump infrastructure public and for kindly providing us with so much good advice. We would also like to thank everyone who helped with the bonding/balling and packaging, BGA socket and PCB work at QuikPak, Ironwood Electronics and Sierra Circuits.

Ultra-low power UWB FMCW radar for presence detection

imec-Netherlands at Holst Centre, Eindhoven, the Netherlands

Contact: Johan Dijkhuis, Barend van Liempd
E-mail: Johan.Dijkhuis@imec-nl.nl , Barend.vanLiempd@imec.be
Technology: TSMC CRN40ULP 1P85X1Z1U ALRDL
Die size: 1300um × 1700um (before shrink) 1.17mm × 1.53mm (silicon)

Description

To reduce our CO_2 footprint in an affordable way we must reduce our energy consumption. One way to do that is to switch off large energy use like lighting and air conditioning when it is not needed. Presence detection is currently done with passive infrared sensors, but these have trouble detecting non-moving persons. By using radar the breathing and heartbeat can be monitored, so even a person reading can be detected. Also the number of persons in an area or room can be detected. Current radar solutions for these applications use hundreds of milliwatt, which is too much for batteries or energy harvesters. We have designed a FMCW radar using the 8 GHz UWB band which uses less than a milliwatt average power, which is 100 times lower than other solutions.

The 8 GHz band was selected because there is enough bandwidth available to have good resolution, and it also allows using cellular circuit techniques in standard 40 nm CMOS (as opposed to mm wave methodologies). Additionally, it allows through-wall operation. All the critical analog parts are integrated on the die (signal generation with DCO, RF PA, RX and ADC), as well as the digital blocks needed for TX spectral mask and FMCW linear ramp generation. Because the algorithms for detection are an active area of research the radar is designed to allow flexible system design and the RX signal processing is using an external FPGA. This also allows other applications like wirelessly monitoring vital signs for medical use. The digital can be integrated together with the analog in a SoC for lowest system cost and power consumption.

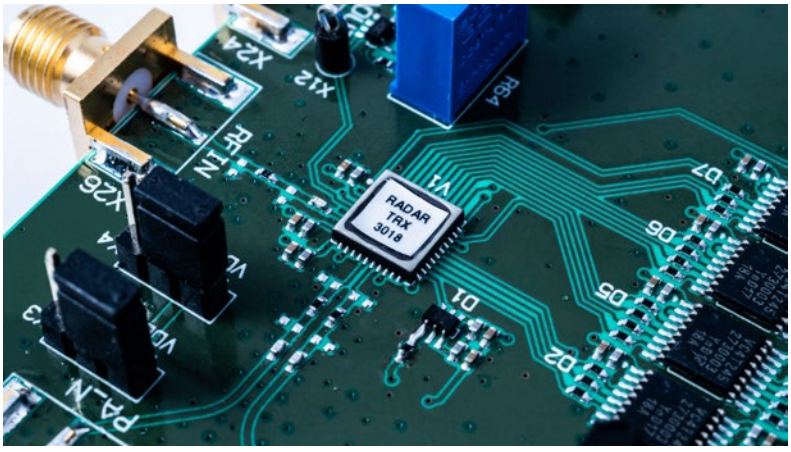


Fig. 2: photograph of measurement PCB

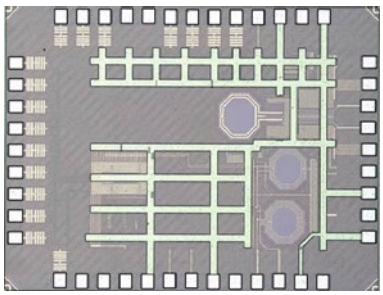


Fig. 1: die photograph

Important design challenges are the tight spectral mask requirements from regulators, the linearity of the frequency sweep and sensitivity. Using digital compensation, analog imperfections are corrected. The new RADAR transceiver is compliant with FCC and ETSI spectral regulations for the UWB frequency range. The sensor's sensitivity is good enough for a range of up to 15 meters for micro movements like breathing detection.

A paper about this work has been published at the 2019 ISSCC.

Why Europractice?

Europractice offers fast and affordable access to state of the art deep submicron process technology. The support offered and quick feedback on DRC violations and other issues is also very much appreciated.

Acknowledgement

The 8GHz UWB radar is part of imec's radar IC program developing low-cost and low-power radar technologies based on the standard CMOS process. Others include the 79GHz phase-modulated digital radar and antenna-on-chip 140GHz radar. Together with imec's novel sensor fusion algorithms, imec opens up completely new opportunities for remote sensing in various fields such as automotive, security, and human-machine interaction.

Mr. Wolf will solve problems

ETH Zürich, Switzerland in collaboration with University of Bologna, Italy

Contacts: Luca Benini
E-mail: lbenini@iis.ee.ethz.ch
Technology: TSMC 40nm LP
Die size: 3.2mm × 3.2mm

Description

Mr. Wolf is an open-source, cluster-based, low-power IoT processor based on the open RISC-V ISA developed as part of the PULP project in collaboration with ETH Zürich and University of Bologna. The processor has two main components.

The heart of the system is the cluster that contains eight 32bit RISC-V cores that can access a 64 kByte shared memory in parallel. The cluster is able to run at up to 350 MHz (@1.1V) and at this frequency, thanks to custom instruction set extensions, has been measured to execute 850/1700/3400 Million Multiply Accumulate operations per second when running matrix multiplications on 32/16/8 bit integers respectively. Two shared floating point units allow the cluster to perform up to 500 Million Floating point Multiply Accumulate operations per second.

The contains a ninth (and smaller) 32-bit RISC-V core in the SoC domain surrounding the cluster in its own voltage and frequency domain. The SoC domain includes 512kBytes of on-chip SRAM, a wide range of peripherals, a microDMA system that is able to copy data to and from peripherals independently, and the before mentioned ninth 32-bit core to run simpler computing tasks and manage the I/O. A DC/DC converter from Dolphin Integration allows both power domains to be controlled independently, and from a low power 32kHz crystal oscillator two independent FLLs provide the clock signals for the system. Together, the chip has several different power modes, that can be selected depending on the needs of the application. In data retentive deep-sleep mode most of the chip is

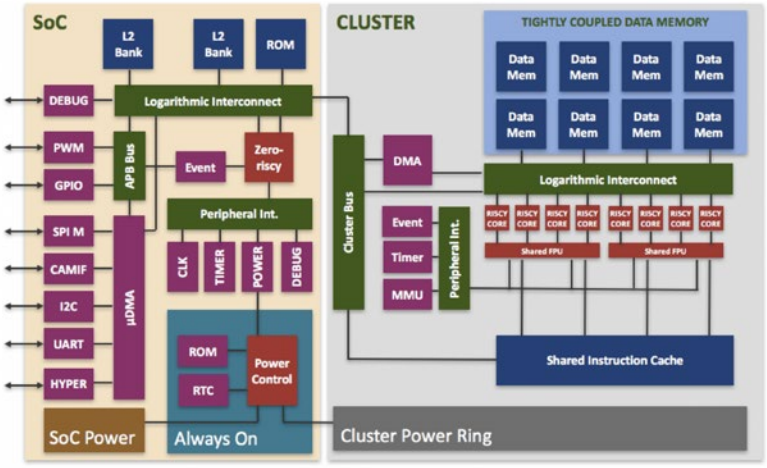


Fig.1: Block diagram of Mr. Wolf

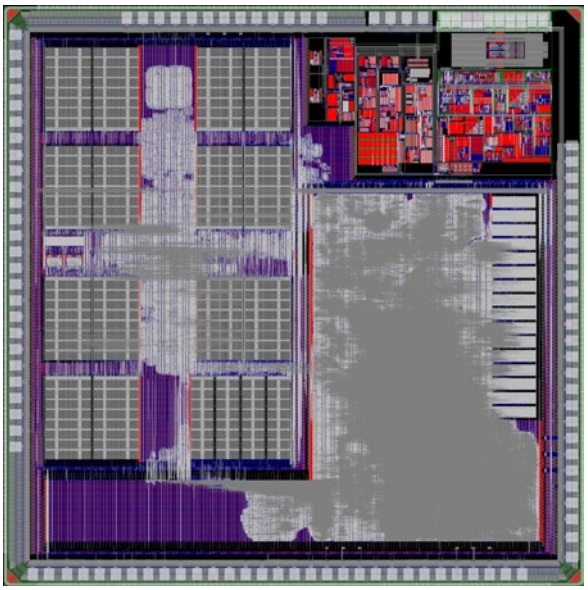


Fig.2: Layout of Mr. wolf, showing the SoC domain with 512kByte memory (top left), the cluster with eight RISC-V cores (bottom right) and the DC/DC converter from Dolphin Integration (top right).

shut down, but the memory power supply is kept at a level to preserve its contents, allowing fast wake-up. Mr. Wolf has been measured to consume as little as 108uW in this mode. On the other extreme with the cluster running at full power the total power consumption of the entire system has been measured as 153mW (at 1.1V supply). The chip can be tuned to operate at the most energy efficient operating point that matches the computation requirements of the application. At its most energy efficient operating point (0.8V supply), Mr. Wolf achieves 15/9 Million Multiply Accumulate operations per second per mW for 32-bit integer/floating point operations respectively. The performance, coupled with the rich set of peripherals has allowed us to utilize Mr. Wolf in a number of applications, such as a neural network to detect obstacles in real time for drone operation.

The SystemVerilog sourcecode of Mr. Wolf has been released using a permissive open source hardware license (Solderpad SHL 0.51) and is available under: https://github.com/pulp-platform/pulp. It is exactly this code that was taken by Greenwaves Technologies and modified for their GAP8 processor which was also released this year.

Why Europractice?

Even as a group with significant IC design experience, we need the help and support of experienced partners, especially when attempting a more complex design in a new technology. Europractice IC services have been instrumental in this regard. Since this chip was designed to be used in boards, we required a slightly higher number of chips, and Europractice IC services helped us with a suitable packaging solution for nearly 200 ICs.

References

- Antonio Pullini, Davide Rossi, Igor Loi, Alfio Di Mauro, Luca Benini, "Mr.Wolf: A 1 GFLOP/s Energy-Proportional Parallel Ultra Low Power SoC for IoT Edge Processing", In Proc. European Solid State Circuits Conference (ESSCIRC) 2018, 3-6 Sep 2018, Dresden, DOI: 10.1109/ESSCIRC.2018.8494247.
- http://pulp-platform.org

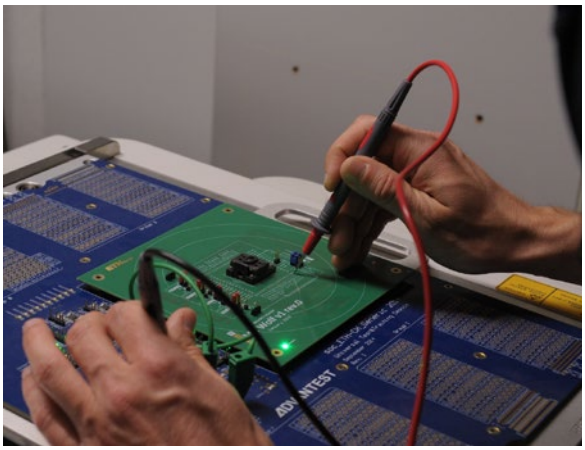


Fig.3: Mr. Wolf being tested on our Advantest SoCV93000 tester

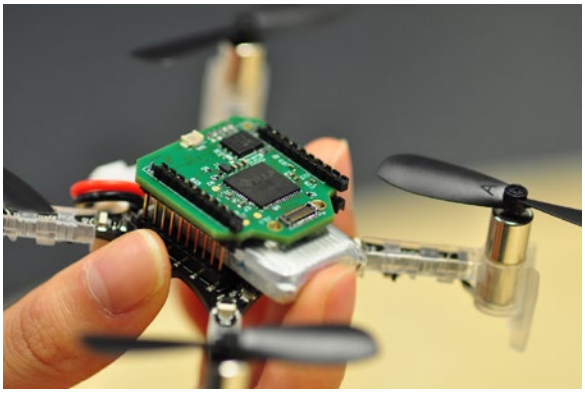


Fig.4: Mr. Wolf mounted on a nano drone. The chip is used to run a neural network to detect obstacles in real time

A successive approximation ADC for biosignal processing

University Institute of Applied Microelectronic, IUMA from ULPGC (University of Las Palmas of Gran Canaria)

Contact: Dr Juan Antonio Montiel Nelson, Dr Carlos Javier Sosa González, Dr Jesús Rubén Pulido Medina
E-mail: jmontiel, jsosa, rpulido @iuma.ulpgc.es
Technology: TSMC 65nm 1P9M_6X1Z1U_RDL
Die size: 1920µm × 1920µm

Description

Our design is composed by a successive approximation Analog to Digital Converter (ADC) with 18 bits resolution. This system is designed to record signals from biological sensors, like ECG(electrocardiography),EMG(electromyography)and EEG (electroencephalography). The sensors to record these signals uses electrodes.

The digitalization of the analog signal uses threshold configurable regenerative comparators. This regenerative comparator is based on the principle of the well-known latch-type voltage sense amplifiers used in the output reading circuitry of memories. These comparators are particularly interesting in this type of applications since they allow a fast settlement of their final value. Another advantage of this type of comparators is the ultra-low power consumption.

The ADC has a dynamic range of 178mV, working with a resolution of 680nV, due to its 218 steps. The maximum power consumption of the conversion system is 1.442uW, a very little fraction of the whole chip power consumption. The maximum decodification time is 0.602155 ns, so its maximum operational frequency is over 1.5 GHz. Due to the ECG, EMG, and EEG signals have a working frequency of only a few kilohertz, the system is fully capable to digitalize the signals. In addition, the circuit shows a very good linearity, with a DNL of 0.36.

16 ADC´s, divided in 2 columns and 8 rows, compose the chip as we can see in Fig. 1 (Layout) and Fig. 2 (Photograph). The system is digitally managed by a controller block, allowing to the analog signals engage the input of the ADC´s. The digital converted data is stored in an inner memory of 64 register with 18 bits wide. The configuration data registers and the data read are performed serial via through two signals, “si” and “so”.
Finally, the performance of the chip has been measured by connecting it to a PC, through a FPGA in order to command the configuration, and the reception of the data stored in the chip internal memory.

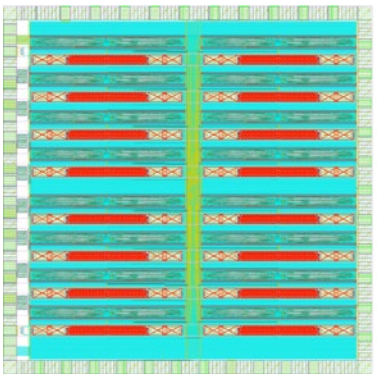


Fig.1 Layout of the chip.

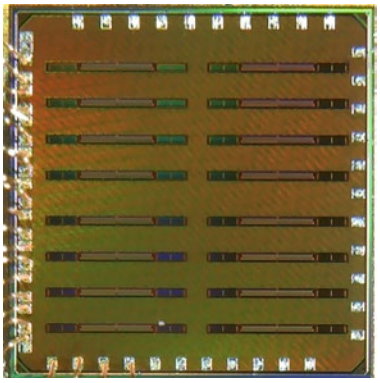


Fig .2 Photograph of the chip.

Why Europractice?

The University Institute of Applied Microelectronic, IUMA has been working with Europractice since many years. We usually work with TSMC and UMC design kits supplied by this organization. For us, is very important the work of the people from Europractice. Without their support, we can never access to advanced technology process and the design of microelectronic circuitry. We appreciate to Europractice its support and collaboration during these years, and we would like to work together during many years.

Acknowledgment

This work was funded by project SURF (TEC2014-60527-C2-1-R) of the Spanish Ministry of Economy and Competitiveness.

Low power, high-dynamic range Ring Oscillator based Delta-Sigma Analog-to-Digital Converter

Analog and Mixed-Signal VLSI group, Electrical Engineering, University at Buffalo, NY, USA

Contacts: Akshay Jayaraj, Sanjeev T. Chandrasekaran, Mohammadhadi Danesh and Prof. Arindam Sanyal

E-mail: arindams@buffalo.edu

Technology: TSMC 65nm CMOS LP MS/RF (mini@sic)

Chip size: 2000µm × 2000µm

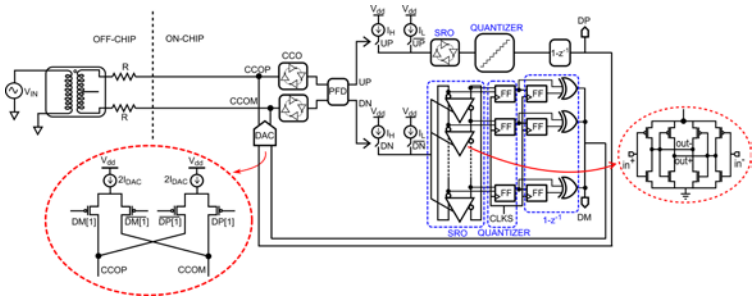


Fig. 1: ADC circuit schematic

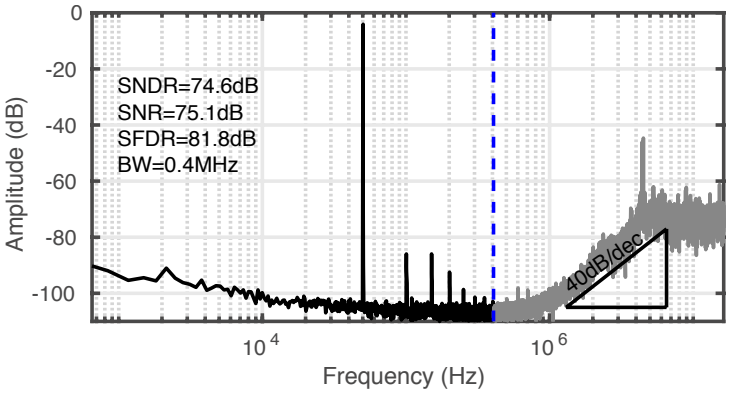


Fig. 2: Measured ADC spectrum

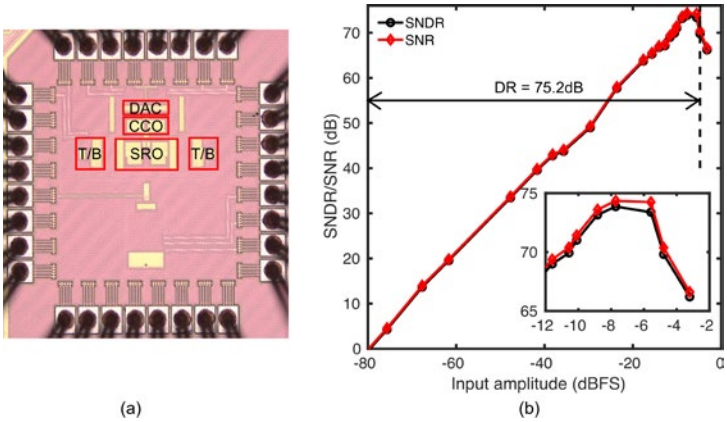


Fig. 3: (a) ADC prototype (b) measured ADC dynamic range

Project Description

The goal of this project to design very high energy efficiency delta-sigma (analog-to-digital converter) ADC using mostly digital techniques. A second-order continuous-time delta-sigma ADC is designed using two current-controlled ring oscillators (ROs). The ROs act as phase-domain integrators. A negative feedback loop using a current steering non-return-to-zero (NRZ) digital-to-analog converter is used to suppress the signal swing seen by the first RO. The phase output of the first RO is extracted using a tri-state phase/frequency detector and is given as an input to the second RO through a 1-bit current DAC. Since the second RO operates at only two frequencies, it has very high linearity. The proposed ADC does not need additional circuits for excess loop delay compensation. Instead, loop delay is compensated through tuning the RO gains. We have fabricated a 65nm prototype that consumes only 10.6fJ/conversion-step at a bandwidth of 2.5MHz which is 2.5X improvement over the current state-of-the-art. The measured common-mode rejection ratio (CMRR) is 57.9dB and power supply rejection ratio (PSRR) is 68.1dB.

Acknowledgement

This work is supported by Semiconductor Research Corporation (SRC) task 2712.020 through The University of Texas at Dallas' Texas Analog Center of Excellence (TxACE).

Why Europractice?

Europractice service offers affordable fabrication of mixed-signal chips designed in our lab. It was also easier for our University to execute non-disclosure agreement with Europractice for TSMC process than similar prototype vendors in USA.

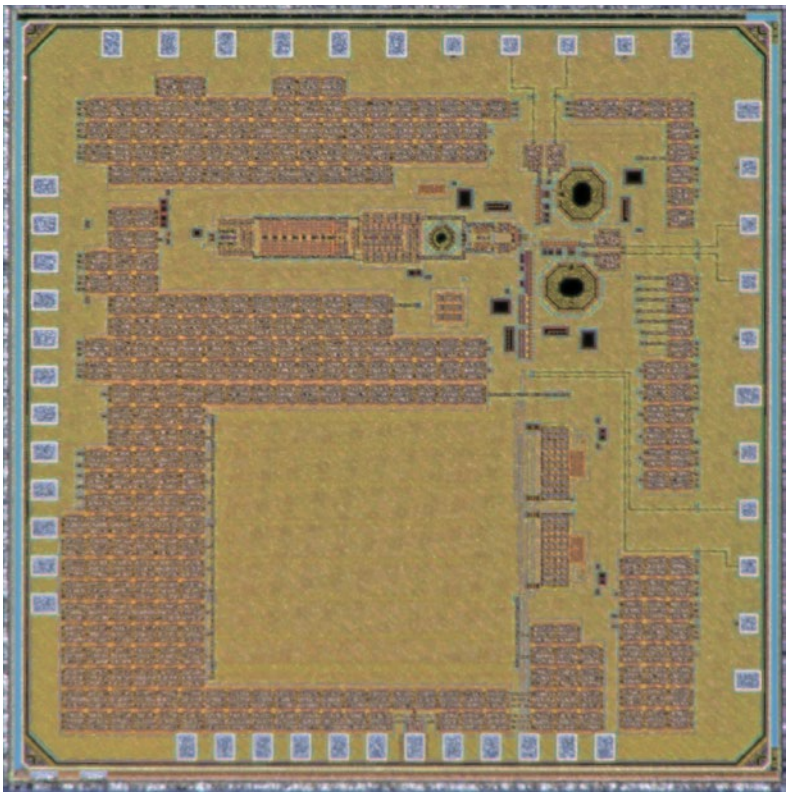


Fig.1: Photo of fabricated chip

Digitally Controlled Synthesizer, 12 GHz

eesy-ic GmbH, Frauenweiherstr. 15, 91058 Erlangen, Germany

Contact: Dr. Frank Ohnhäuser, Markus Kempf
E-Mail: info@eesy-ic.com
Technology: TSMC 65nm CMOS Logic - MS/RF, General/LP run
Die size: 2mm × 2mm

Features

- Reference Fequency 128 MHz
- Frequency Range 12 GHz - 12.5 GHz
- DCO Phase Noise ca. -80dBc/Hz @ 100 kHz
- DCO Fequency Resolution ca. 10 kHz
- Output Power ca. 0 dBm
- Programmable Loop Filter
- FMCW Ramp Generation: 500 MHz Bandwidth, 0.1ms-10ms Sweep Time
- FSK Modulator: 2 MHz Bandwidth with 5 ksymb/s - 100 ksymb/s
- Two-Point Modulation Scheme
- Calibration Algorithm for FMCW Ramp Linearization

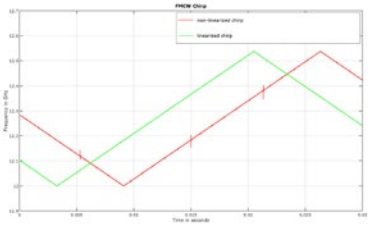


Fig.2: Chirp comparison

Description

Funded by BMBF, eesy-ic offers a digitally controlled frequency synthesizer for FMCW radar systems. Based on an All-Digital Phase Locked Loop, it generates a very stable frequency modulated signal in the range of 12 GHz to 12.5GHz which can be configured via an SPI interface. Fast and linear chirps are the groundwork for high precision positioning. The chirp duration is adjustable from 0.1ms to 10ms and the modulation frequency is programmable up to 500 MHz with 24 Bits resolution. An integrated software controlled measurement of the oscillator's frequency characteristic triggers a linearization that makes highly linear frequency ramps possible. Phase noise and modulation speed can be optimized with the aid of two-point modulation and a programmable loop filter. Additionally, an FSK modulation enables the exchange of data between two radar stations.

Why Europractice?

Regarding academic research and also developments for new products in the field of IC Design, prototyping is indispensable. Europractice offers good prices at a high level of flexibility at the same time. There is neither a problem nor any extra effort for the designer to submit multiple designs that share the same area. A variety of PDKs and multi-project wafer runs are available at pretty short and regular intervals. Also, the technical support can be of some assistance when approaching a tape-out deadline as well as any information or advice concerning the technologies and PDKs.

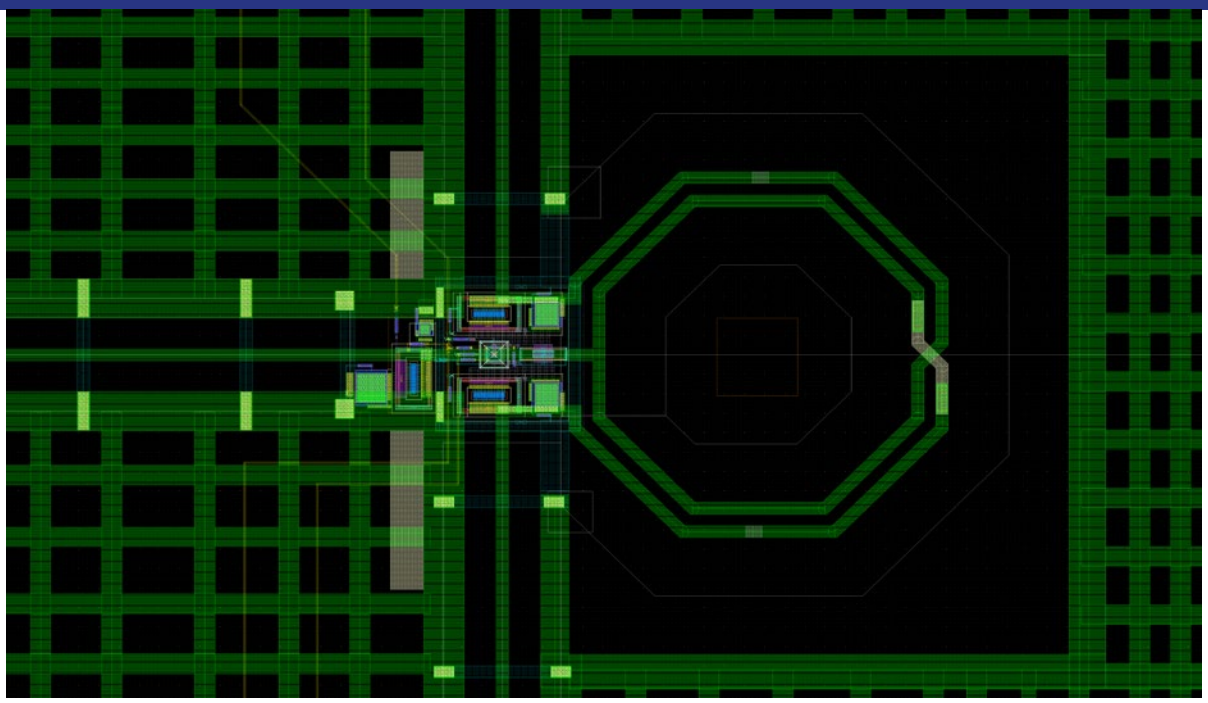


Fig.1: Circuit Layout

Tunable, Wideband, Low-Loss TX-to-RX Isolator for Full-Duplex and Frequency-Division-Duplex Phased-Array Systems in mm-W

Technion, Israel

Contact: Yanir Schwartz
E-mail: yanirs@technion.ac.il
Technology: TSMC 65nm CMOS LP MS/RF (mini@sic)
Chip size: 500um × 500um

Description

We have designed a tunable, wideband, low-loss TX to RX isolator to be implemented as a duplexer in common-antenna phased-array systems at mm-W frequencies. We have then manufactured this device in TSMC's 65nm process and designed it for a center frequency of 60GHz. The core of this device is comprised of an autotransformer which is a differential inductor with a center tap to which a balance network is connected. It is designed to have an analog cancellation of the TX signal at the RX port by going through two different paths and summing at the RX port with opposite phases. The tune abilities of this circuit allow the compensation for process corners and frequency shifting of the frequency of operation. Our design has an isolation bandwidth of over 20GHz for a minimal isolation of 30dB. It has ANT-RX and TX-ANT insertion losses of roughly 3.5dB which is only 0.5dB above the 3dB theoretical limit of such passive three-port topology.

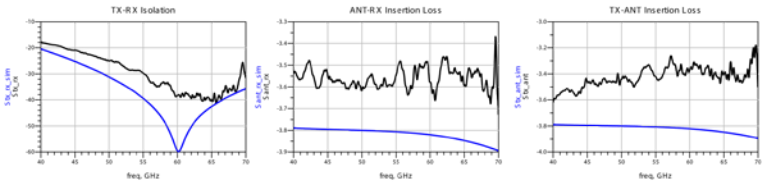


Fig.2: Measurement vs. Simulation

The measurements show that we have better insertion losses than expected, and a frequency shift in isolation. The measurement set-up is limited in dynamic range thus we cannot see the notch in the left graph, reaching simulated isolations of 60dB. We instead get a roughly flat isolation of maximum 40dB and of minimum 30dB over a frequency range of close to 15GHz. We expect this to be wider since the measurement is limited to only 67[GHz].

Why Europractice?

We chose to manufacture this chip, along with previous others, through Europractice because of their services, suitable for our academic research purposes. They have provided technical support along the way, based on their well-established experience with TSMC's processes. They also offer affordable prices making it attractive for us as a research group to experiment with various designs, as well as their high availability and reliable on-time delivery.

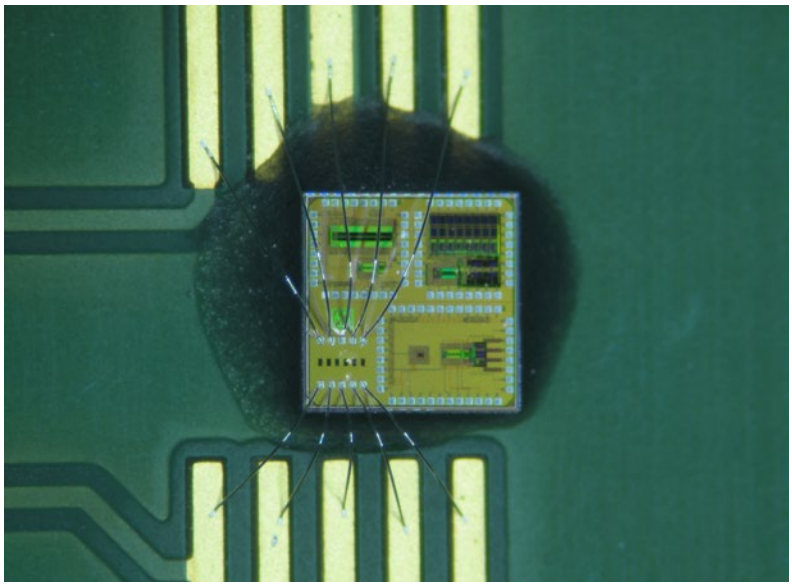


Fig. 1: die mounted on a PCB for testing

Low-power ADCs: test structures and versatile interfaces

Eindhoven University of Technology, Integrated Circuits Group, The Netherlands

Contact: Haoming Xin, Pieter Harpe, Eugenio Cantatore
E-mail: h.xin@tue.nl; p.j.a.harpe@tue.nl; e.cantatore@tue.nl
Technology: TSMC 65nm CMOS LP MS/RF
Die size: 1960µm × 1960µm

Description

We are regularly taping out circuits with Europractice. In this particular case, six different prototype circuits were integrated on a single mini@sic die for testing (Fig. 1). Most of these designs were built around low power analog-to-digital converters (ADCs), and find their application in medical and wearable sensing or IoT nodes. In the following, two of the implemented designs are discussed in more detail.

The first design, which is an extension of[1], implements a versatile capacitive sensor interface created around a low-power ADC. Rather than using a conventional amplifier-based frontend, the proposed design connects any external capacitive sensor to the ADC directly. Reference capacitors and switches are integrated in the design as well to enable proper sensing of the capacitor value. While this approach is not as good in resolution and accuracy compared to conventional architectures, the main advantage of this work is that the power consumption is extremely low, and that the power scales inherently with the selected speed, resolution, and capacitor range. In this way, an efficient versatile interface is feasible, that is useful for instance for highly energy-constrained applications.

The second design contains a 10b successive approximation (SAR) ADC, based on [2], where the main aim is to minimize chip area. This is relevant for instance for multi-channel digitizers or embedded converters as limited area may be available. In typical cases, the SAR ADC area is dominated by the large capacitive DAC. This DAC is usually large since it contains many unit capacitors (e.g. 2046 for a differential 10b DAC) that need to be accurately matched. In this work, the conventional approach of unit elements is discarded, but instead a new method is proposed that can also achieve good intrinsic matching, while significantly reducing chip area. As a result, the entire ADC core is integrated in only 36µm x 36µm.

Results

A few measurement examples are shown here. Fig. 2 shows measurements of the capacitive sensor interface, where an external MEMS pressure sensor was attached. The interface, including ADC and sensor power, consumes only 0.8nW when recording environmental pressure at a rate of 100S/s. Fig. 3 shows the linearity measurements of the 10b ADC, reaching good linearity despite the small chip area.

Why Europractice?

Europractice offers all the required design tools and a regular and affordable fabrication schedule for test ICs. Having a single organization supplying all tools, fabrication and support is greatly simplifying the process to setup and maintain an IC design group. We have been using

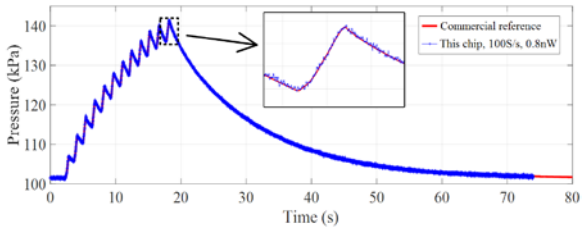


Fig. 2: measured pressure using our interface, and benchmark against a commercial reference

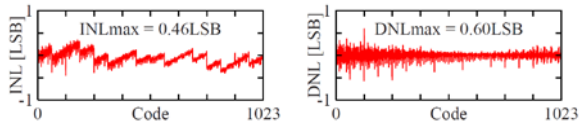


Fig. 3: measured ADC non-linearity

several technology nodes for quite many years, which was feasible thanks to the long-term dependability from Europractice. The excellent support, knowhow, and patience from all Europractice colleagues has been essential in our success. We're looking forward to many more years of collaboration.

Acknowledgement

This tape-out received funding from the EU's Horizon 2020 research and innovation programme under grant agreement No 665347 (project PHOENIX). The authors would like to thank Murata Electronics for providing sensor samples.

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[1] H. Xin, M. Andraud, P. Baltus, E. Cantatore, and P. Harpe, "A 0.1nW-1µW All-dynamic Capacitance-to-Digital Converter with Power/Speed/Capacitance Scalability," ESSCIRC Sept. 2018.

[2] P. Harpe, "A Compact 10b SAR ADC with Unit-Length Capacitors and a Passive FIR Filter," in IEEE Journal of Solid-State Circuits, Nov. 2018 (early access).

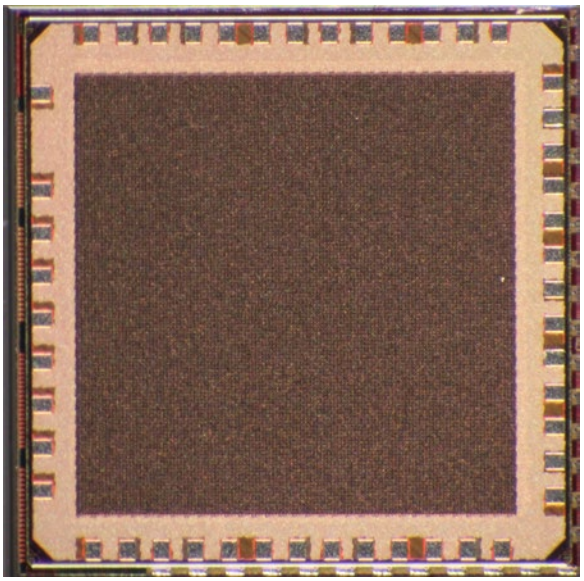


Fig.2: Picture of fabricated chip

Selective Change Driven Vision Sensor (A First User Story)

Departamento de Informática – University of Valencia, Spain

Contact: Fernando Pardo, Càndid Reig, Jose A. Boluda, Francisco Vegara
E-mail: Fernando.Pardo@uv.es
Technology: TSMC 65nm CMOS LP MS/RF (mini@sic)
Die size: 1920µm × 1920µm

Description

A 128x128 Selective Change Driven (SCD) vision sensor has been designed and fabricated using TSMC 65nm CMOS LP MS/RF technology. This vision sensor has the unique feature of sending the pixel that has undergone the largest change since the last time it was read-out. It has the capability of responding instantly to events (in the order of few microseconds), and delivering these pixels in an ordered way, attending to their contribution to the event. There is no frame or image stream, but a pixel stream based on their illumination change. This behaviour is accomplished by using a single winner takes all circuit (WTA) and a single Loser Takes All circuit (LTA) that are able to select a single pixel from the 16K pixels of the 128x128 vision sensor in less than a microsecond. To our best acknowledge, these are the WTA or LTA circuits with the largest number of inputs ever designed or fabricated. These circuits are able to

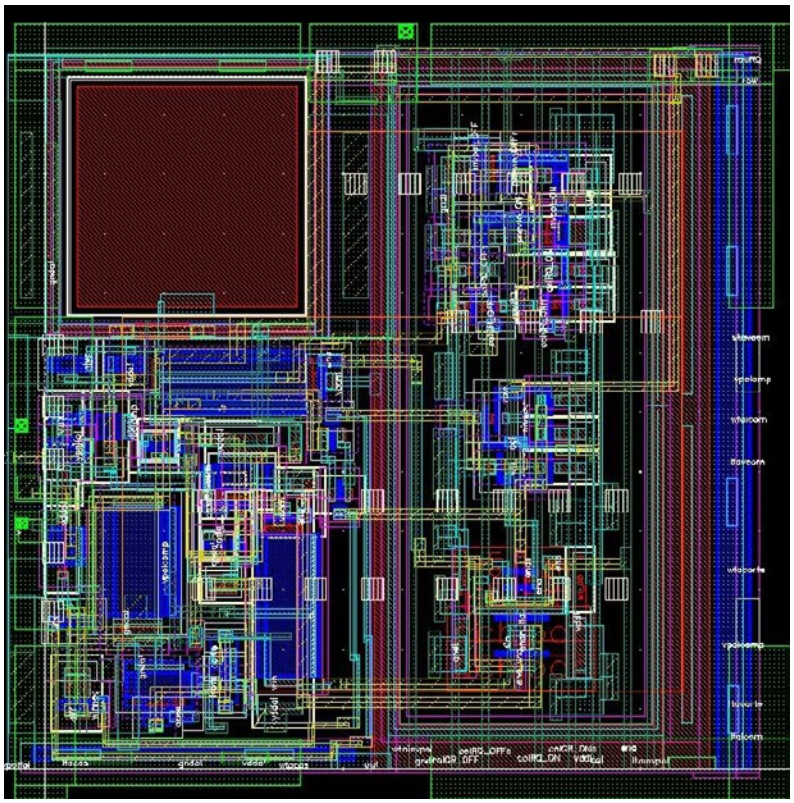


Fig.1: Layout of the design circuit

select a single pixel thanks to the combination of an analog WTA/LTA circuit and a digital selector. It is similar to other Dynamic Vision Sensors (or event-based sensors) though this SCD sensor is able to order the pixels by the magnitude of their change thanks to the WTA/LTA. Moreover, the WTA/LTA circuit allows a simpler synchronous interface controlled by an external processor instead of the sensor.

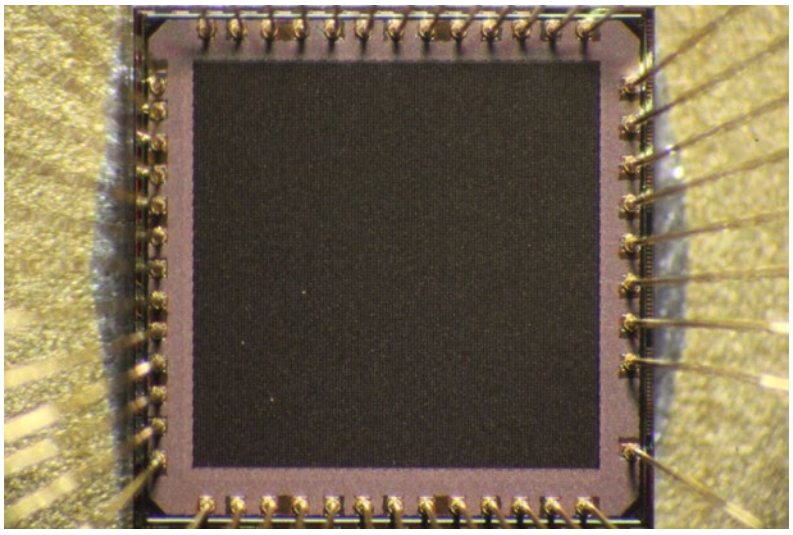


Fig.3: Picture of wire-bonded die

The basic sensing cell consists of a well-known logarithmic response cell based on continuous reading instead of light integration. When a pixel is selected for reading, its illumination level is also stored in the cell for future change comparison. The difference between the stored and the current illumination levels of all pixels in the array, are compared by the WTA and LTA circuits, which select a single loser or winner (the loser is the pixel that has undergone the largest negative change, while the winner is the pixel with the largest positive change). This operation can be performed in just 100 ns.

Why Europractice?

The University of Valencia is member of Europractice since 1993. We appreciate the software and services catalogue at very competitive prices for educational institutions offered by Europractice, and we are especially pleased with the support on new technologies. This is why we have been able to learn and try new state of the art technologies.

Acknowledgement

We would like to thank Europractice for the grant of the First User Stimulation Action that has allowed us to fabricate this chip in 65 nm technology with a significant reduction of the initial price. This research has been funded by the grant number TEC2015-66947-R of the Spanish Government (MINECO) and the European Regional Development Fund (FEDER).

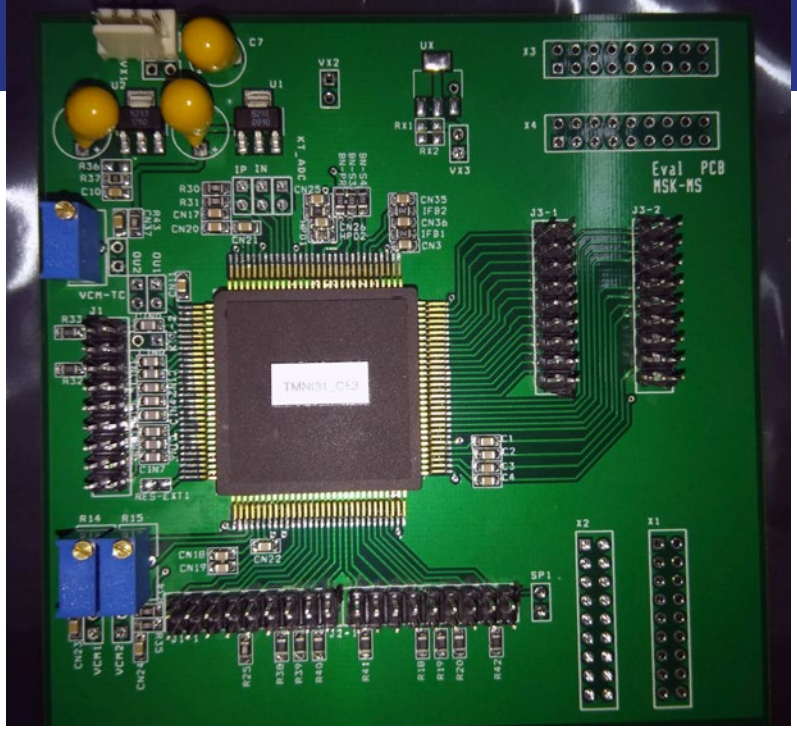


Fig.2: Test board with the chip

8-channel readout ASIC for time projection chamber and capacitive sensors

Belarusian State University of Informatics and Radioelectronics (BSUIR), CAD Laboratory, Belarus

Contacts: Viktor Stempitsky, Aliaksandr Kastrou
E-mail: vstemp@bsuir.by, nil44@bsuir.by
Technology: TSMC 0.18 um CMOS MS/RF 1.8V/3.3V
Die size: 3.4mm × 5mm

Description

The developed ASIC is intended for primary processing of signals taken from the sensing electrode, so-called «Readout Chamber» (ROC), of time projection chamber (TPC). ASIC can also be used for processing of nanosecond-range current pulses and other capacitive sensors: photodiodes, semiconductor sensors, proportional chambers, tubes etc.

A single ASIC channel is comprised of functional units: charge-sensitive preamplifier/shaper with a semi-Gaussian response (180-210 ns peaking time); shaping amplifier (SA) with ion tail cancellation circuitry; differential output baseline restorer (BLR); frontend amplifier; 10 bit 10 MSPS ADC; digital multiplexer with a chip controller; LVDS interface for outputs and clock input; reference voltages and currents block; internal power-on-reset (POR) circuit; control registers with serial interface; calibration/test modules. Input clock frequency for ADC and digital blocks is 160MHz.

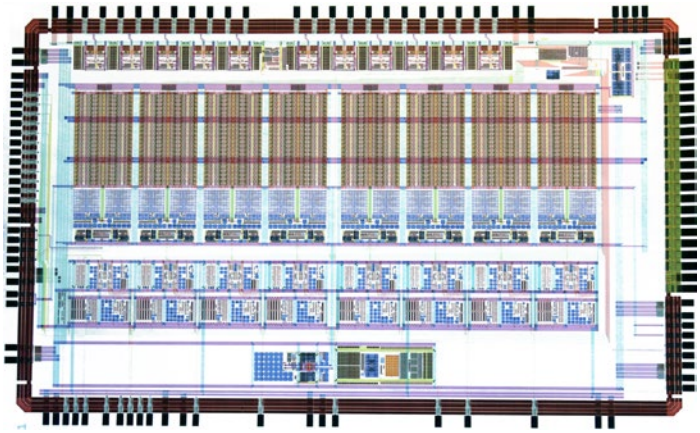


Fig.1: Layout of the fabricated chip

The frontend block of the ASIC performs the analog stages of signal processing. Input current pulse signal integration and converting of this signal into voltage (pulse with the delay time constant of the order of tens of microseconds and with the rise time less than 10 ns). Frequency filtering of the signal is implementing by a multi-stage active bandpass filter using classical RC-CR3 shaping amplifier. The feature of this stage is the availability of the additional adjustable circuit for suppression of the low-frequency component input signal spectrum, typical for the ROC TPC, proportional chambers and tubes.

10-bit high-speed ADC conversion rate is 10 MSPS and is implemented based on successive-approximation register architecture (SAR). Digital parallel multiplexer routes ADC data in continuous mode from each channel and pass to output LVDS interface. Output clock is also transmitted synchronously with data through LVDS.

Why Europractice?

We appreciate the Europractice services which allow affordable access and reasonable prices to leading edge IC technologies, frequent MPW fabrication runs, CAD tools, packaging services. It is wonderfully suitable for academic institutions.

The non-classical gate layouts to boost the Electrical Performance of MOSFETs and consequently the analog and digital CMOS ICs applications

FEI University Center, Department of Electrical Engineering, Brazil

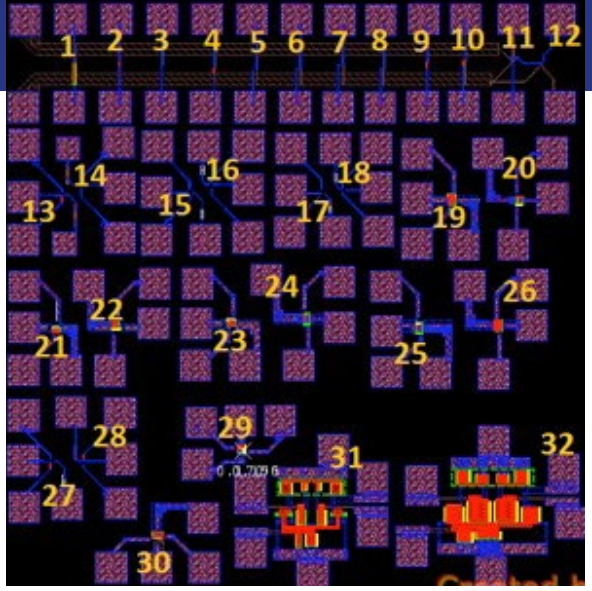
Contact: Prof. Salvador Pinillos Gimenez
E-mail: sgimenez@fei.edu.br
Technology: TSMC 0.18u CMOS MS/RF
Die size: 6.1mm × 6.1mm

Description

This project aims to study the impact of the non-standard gate geometries (hexagonal, octagonal, ellipsoidal, wave, and fish) in the electrical behavior of Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFETs) in relation to the typical rectangular one, by using 180 nm Bulk CIs CMOS technology, via IMEC Free Mini@sic Fabrication. Besides, some Planar Power MOSFETs and Operational Transconductance Amplifiers were manufactured by using this innovative layout styles to verify the advantages of these devices to improve the electrical performance of these devices in harsh environment (room temperature, high temperatures, ionizing radiation, etc.).

A lot of investments have been done to improve the electrical performance of MOSFETs, such as new transistors structures, material, manufacturing process, etc. Although still little used by semiconductor devices and integrated circuits (ICs) industries, another approach is to use innovative gate layout styles for MOSFETs, which are capable of adding new constructive effects in their structure (Longitudinal Corner Effect, LCE, Parallel connection of MOSFETs with Different Channel Lengths Effect, PAMDLE, and Deactivation of Parasitic MOSFETs in Bird's Beak Regions Effect, DEPAMBBRE). It is important to highlight that this innovative layout technique does not add any extra cost to the manufacture Complementary MOS (CMOS) ICs manufacture process (zero cost solution) [1].

Figure 1 illustrates the manufactured IC layout (Fig. 1a) and its corresponding picture (Fig. 1b).



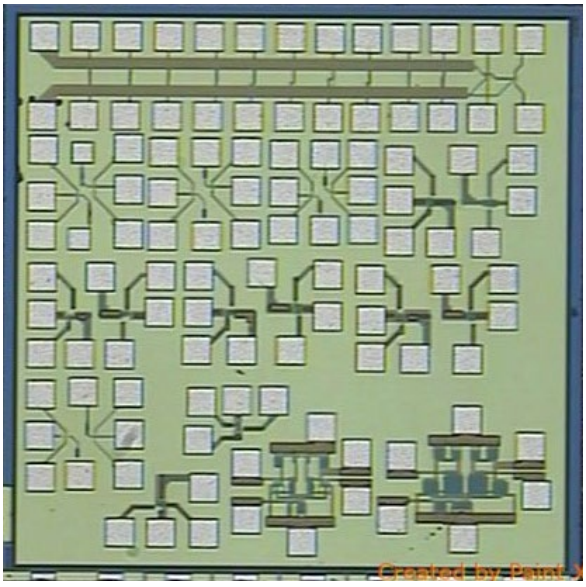


Figure 1. Layout (a) and picture (b) of the fabricated IC.

These innovative non-standard MOSFETs (Diamond, Octo, Ellipsoidal, Wave and Fish) have been evaluated and compared to the classical rectangular ones in order to quantify their better performance, regarding the same gate areas and bias conditions in room temperature and harsh environment (high temperature, ionizing radiation, etc.) [2].

Results

Regarding to show some results obtained of this CMOS ICs, Table 2 presents the MOSFETs IDS/(W/L), and the percentage gains of the DM IDS/(W/L) in relation to the RM counterpart (GDM) in Triode region, considering a VGS equal to 1.5V.

V_{DS} (V)			
	0.1	0.5	0.9
DM (α=900) I_{DS}/(W/L)	349.08µA	1.08mA	1.2mA
RM I_{DS}/(W/L)	158.39µA	0.45mA	0.49mA
G_{DM} (%)	120.4	140.0	144.9

Table 2. I_{DS}/(W/L) of the devices, and the percentage gains of the DM I_{DS}/(W/L) in relation to the RM counterpart (G_{DM}) in Triode region (V_{GS}=1.5V).

Conclusions

Based on Tables 1, we can conclude that the $I_{DS}/(W/L)$ of the DM operating in the Triode and Saturation regions are always higher (Triode region: from 120% to 145%; and in Saturation region: from 64% to 112%) than those found in the RM counterparts. This can be justified due to the LCE and PAMDLE effects, which are capable of boosting the electrical performance of the MOSFETs. Consequently, this innovative layout style can be used to boost the electrical performance of sensors, Planar Power MOSFETs and analog and digital CMOS ICs applications as in the room temperature as in the harsh environment (high temperature, ionizing radiation, etc.). These studies are being published in the literature.

Why Europractice ?

First of all, Centro Universitário FEI acknowledges Prof. Jacobus Swart (FAPESPUNICAMP), Tobias Vanderhenst (IMEC), and the EUROPRACTICE IC service for giving the opportunity of manufacturing the devices, via IMEC Free Mini@sic Fabrication. This opportunity given by IMEC enables to the Researchers and Professors of Centro Universitário FEI to perform high level and complex researches in the nanoelectronics area (devices, sensors, analog and digital CMOS ICs) and consequently publish in important national and international conferences and renowned journals.

Reference

[1] Gimenez, S. P., et. Al., An innovative Ellipsoidal layout style to further boost the electrical performance of MOSFETs. IEEE Electron Device Letters (Print), v. 36, Issue 7, p. 705-707, 2015.

[2] W. S. Cruz, J. W. Swart, and S. P. Gimenez, Using Ellipsoidal Layout Style to Boost the Electrical Performance of the MOSFETs Regarding the 180 nm CMOS ICs Manufacturing Process. ECS Transactions, Ho2-1467, 2018.

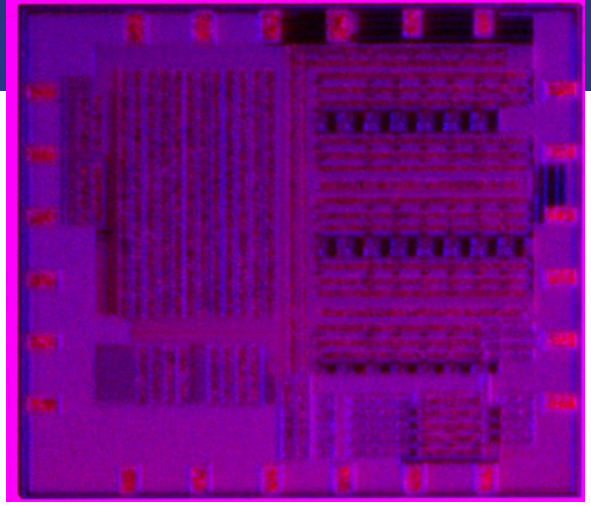


Fig. 1: Microscope view of the fabricated chip.

Integrated Synchronous Buck Converter with Adjustable Dead-Times

University of Zagreb, Faculty of Electrical Engineering and Computing, Zagreb, Croatia

Contact: Josip Bačmaga, Dr. Raul Blečić, Prof. Adrijan Barić
E-mail: adrijan.baric@fer.hr

Technology: TSMC 0.18u CMOS Logic or MS/RF
Die size: 1660µm × 1660µm

Description

The dead-times between the control signals of the synchronous switching DC-DC converters are set to prevent the overlap of the conduction modes of the transistor switches and cause malfunction or a failure of the power converter. The adjustable dead-times between the generated control signals enable to evaluate the impact of the control signals on the efficiency and electromagnetic interference (EMI) of the designed converter. An integrated synchronous switching DC-DC converter with the adjustable dead-times between the generated control signals is designed in TSMC 0.18-µm technology using the supply voltage of 3.3 V. A dual-channel programmable PWM sub-circuit with adjustable and precise timings is designed having the target switching frequency in the range from 100 kHz to 10 MHz, while the pulse width is adjustable with a timestep of 150 ps. Each channel of the PWM subcircuit is constructed of the digital building blocks used for adjusting the pulse width and relative time delay between the driving signals.

Why Europractice?

The Europractice service provides access to leading edge IC technologies and CAD tools at reasonable prices for academic institutions.

Acknowledgement

This work is supported in part by the Croatian Science Foundation (HRZZ) within the project Advanced design methodology for switching DC-DC converters.

Fig.1: Picture of the circuit board a SensaData sensor tag

Smart Active 5.8 GHz RFID tag (Smart-r-tag)

La Trobe University, Centre for Technology Infusion in collaboration with SensaData Pty Ltd, Australia

Contact details: Professor Aniruddha Desai, Director, Centre for Technology Infusion
E-mail: a.desai@latrobe.edu.au
Technology: TSMC 180nm MS/RF
Die size: 4.5mm × 5.0mm

Description

This chip is designed and fabricated with the 180nm TSMC G technology. The final product's application is for tracing and tracking goods in logistics companies and customers. This is a generic RF transceiver with inbuilt sensors and microcontroller with digital and analogue interfaces. Therefore, it can be used in any application where logging sensors and reporting the results via an RF communication is needed.

This Active RFID transceiver has the following components:

- RF TX chain: Pre-Power Amplifier, Power Amplifier, DAC, Low Pass Filter
  - Customised baluns were designed to provide the desired output levels
- RF RX chain: Low Noise Amplifier, Variable Gain Amplifier, Ploy phase and Butterworth low pass filters, differential and variable gain amplifiers, DC offset cancellation and ADC
- PLL: quadrature architecture, Delta-Sigma modulator, auto-calibration, and low phase noise
- High speed digital modem with dc-offset cancellation, pulse shaping filters to meet spectrum regulations, timing synchroniser, FIFO, and sync detection
- Power Management Unit (Bandgap References, LDOs and DC-DC), and Crystal buffers
- Ultra-low power frequency/time configurable wake-up receiver with false wake-up rejection
- SAR-ADC for internal temperature and battery monitor sensors as well as external analogue sensors
- ARM Cortex Mo Microcontroller with SPI, I2C, and UART interfaces and RAM, ROM and EEPROM blocks (included in our next tape-out)

Why Europractice ?

We chose Europractice because

- They offered professional services from initial stages of our design until tape-out and packaging. For instance, they delivered the analogue and digital libraries as fast as possible, helped us use and troubleshoot our tools while using those libraries, were prompt in responding to our queries, and responded with proficient and expert advice on our issues.
- They have connections to various industries required for designing and manufacturing such as IP providers, packaging industry and testing facilities
- They helped us work with a testing company to design our chip for manufacturability and testability
- They also provide competitive pricing while maintaining high quality servicing

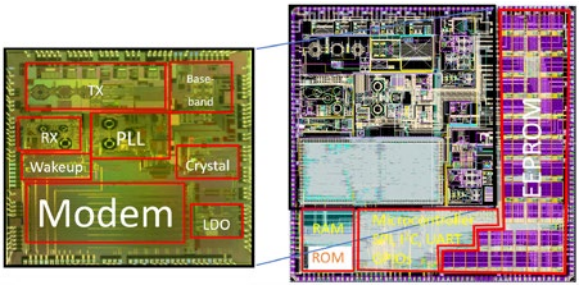


Fig.2: Picture of the fabricated chip (on the left) and the chip layout (on the right).

A Low-Power Low-Area RISC-V based MCU featuring AES Acceleration and USB

Integrated Systems Research Group – OnChip
Universidad Industrial de Santander, Colombia

Contact: Prof. Elkim Felipe Roa Fuentes
E-mail: efroa@uis.edu.co
Technology: TSMC 0.18 µm CMOS MS/ RF/GP 1P6M+AL SALICIDE 1.8/3.3V
Die size: 1660µm × 1660µm

Description

Low-capacity battery-powered and self-powered sensor nodes demand nano-Ampere always-on (AON) circuitry to monitor fluctuating supplies and generate wake-up timers. For instance, periodical-driven sensing systems for low-duty-cycle monitoring applications require low-energy start-up oscillators and voltage supervisors to detect under-voltage battery conditions during a deep power state. Power states are commonly controlled by a power management unit (PMU) that can command processor core, memory and peripherals into idle and sleep states. This microdevice implements a system-on-a-chip (SoC) prototype with a low-power 32-bit RISC-V IM based microcontroller. The processor includes AES core-related accelerator functions, a true random number generator (TRNG), a direct-access memory controller (DMAC), and a universal bus system with 1.1 specification support (USB 1.1). Sleep modes can be activated using low-energy AON subsystem with peripherals for voltage sensing and low-duty-cycle node applications. The SoC features on-chip clock sources allowing to operate the MCU from 32.768kHz to 98MHz. Clock sources in the multiplexing tree are composed by a RC relaxation circuit supporting 32kHz to 1MHz fixed frequencies, a low-frequency crystal oscillator, and a high-frequency crystal oscillator. Voltage sensing in the PMU are performed by a power-on-reset (POR) and a brown-out detector (BOD) optimized for battery-mounted devices and automotive applications. Measured start-up energies using integrated RC-based oscillators show restarting energies down to 6pJ, which is 1000X less than the energy required in MCUs applying just crystal oscillators.

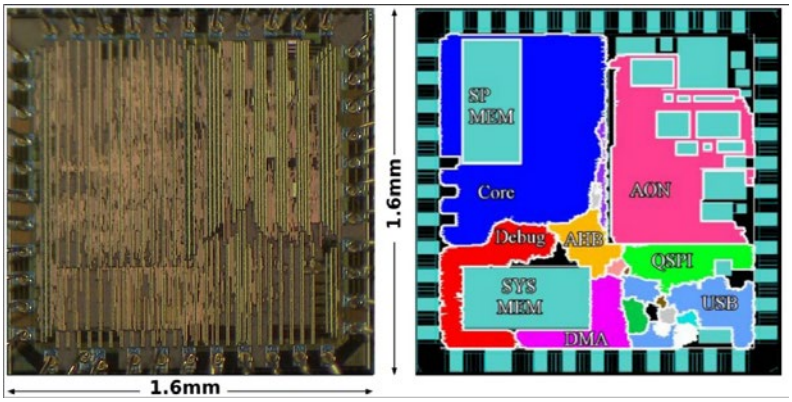


Fig.2: Picture of the fabricated design (left) and indicated the main functional blocks (right)

Why Europractice?

The Integrated Systems Research Group - OnChip, at the Universidad Industrial de Santander (Colombia), has chosen the Europractice MPW service as the best solution to get several TSMC CMOS processes regarding the affordable access and excellent technical support. As a relatively recent research group, OnChip has enjoyed the opportunity to get easy access to CMOS fabrication. We are very happy that Europractice can extend its service to countries where the semiconductor ecosystem is not one of their major strengths, which is our case in Colombia. Thus, allowing us to make our work visible and position our results in competitive scenarios.

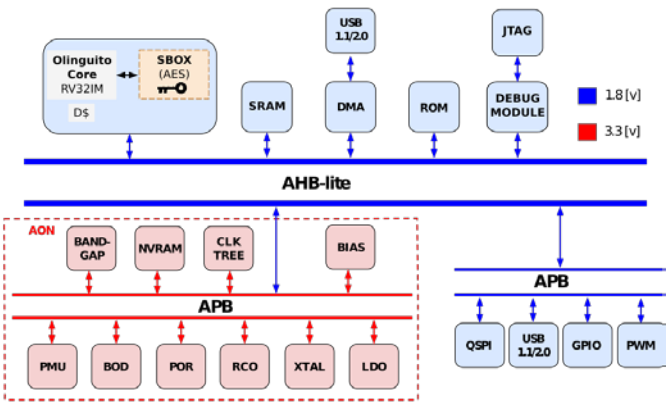


Fig.1: Schematic block diagram of circuitry

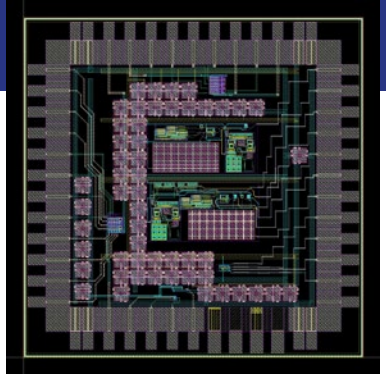


Fig.1: Layout view of the designed chip

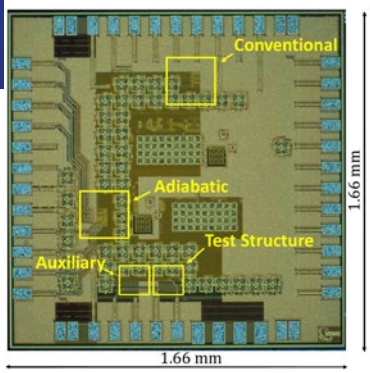


Fig.2: Microscope view of the fabricated chip

Adiabatic Binary Counter using Four-phase Sinusoidal AC-clocked power supply operating at 1 GHz

Department of Communications (DECOM), School of Electrical and Computer Engineering (FEEC), University of Campinas (UNICAMP), Campinas – SP, Brazil

Contact: Designer: Valério Maronni Salles, PhD Student
Supervisor: Prof. Dr. Luiz Carlos Kretly
E-mail: valerio@decom.fee.unicamp.br
Technology: TSMC 0.18u CMOS MS/RF
Die size: 1660µm × 1660µm

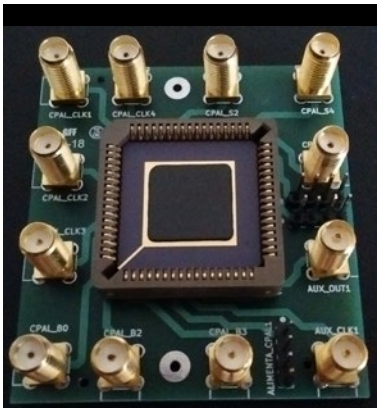


Fig.3: Chip on an evaluation board

Introduction and Motivation

There is growing interest among universities and industry in the field of energy harvesting and IoT. Energy efficiency has become a design concern in high performance devices. On the other side, there is a strong effort on the minimization of energy dissipation associated to the analog and digital circuitry. The strategy of AC-clocked power supply follows this tendency. Energy harvesting is playing an increasingly important role in supplying energy to devices, circuits, and systems in general, but energy harvesting only is not enough for optimum energy efficiency. In addition to energy harvesting, there is a need of reduction of the mass fraction of batteries. Strong efforts on minimizing energy consumption and dissipation associated to analog and digital circuitry must be done. AC-clocked power supply follows this need and the adiabatic logic low-power design technique is nowadays the best candidate to reduce energy loss. In the meantime, aligned with the concept of clean energy, it enables the reduction of the use of toxic elements applied in batteries manufacturing for DC powered circuitry.

Description

The designed chip contains four main blocks: an adiabatic binary counter using four-phase sinusoidal AC-clocked power supply, a conventional binary counter powered by DC voltage, an auxiliary circuit, and a test structure, designed with Cadence Tools. The adiabatic binary counter employs novel techniques both to eliminate the buffers between counter stages, and to simplify the AC-clocked power supply arrangement. The adiabatic binary counter is powered by 0.9 V of magnitude and 0.9 V of off-set sinusoidal wave generators, at frequencies up to 1 GHz, considered great frequency value for adiabatic circuits. The conventional binary counter was designed to allow an accurate power consumption comparison with the adiabatic binary counter. The auxiliary circuit converts the binary digital input signals into adiabatic input signals. The test structure is a ring oscillator. The adiabatic binary counter is being used as a basis for research in adiabatic logic sequential circuits. In addition, adiabatic logic presents both tolerance regarding to asynchronous input, meeting no errors in the logical output levels, and tolerance to the AC-clocked power supply phase shifting. Power savings, compared to conventional CMOS circuit, is approximately 60% @ 1 GHz, so presenting an excellent ratio at microwave initial range. By operating on microwave frequency range it is propitious to outfit microwave equipment, such as receivers, transmitters, analysers, generators and probes.

Why Europractice?

When I was given the opportunity to attend the Free IC Fabrication mini@sic Program for Brazilian Universities I knew I would have an intense job ahead of me. And it really happened. But Europractice service offers procedures that made it much easier to work, from the registration of the project on the web site until the delivery of the prototype chip. Europractice is both very agile in the information exchange with the customer and accurate when requesting and reporting on project issues. Free IC Fabrication mini@sic Program for Universities is a valuable opportunity for academic institutions.

KIPT

Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla y CSIC, Sevilla, Spain.
REDEC Group, Universitat Autònoma de Barcelona (UAB), Barcelona, Spain.

Contacts: Elisenda Roca (IMSE), Rafael Castro-López (IMSE), Montserrat Nafria (UAB)
E-mail: elisenda.roca@imse-cnm.csic.es
Technology: UMC L65N Logic/MM/RF - LL
Die size: 1.847mm × 1.847mm

Description

KIPT is a chip designed for the statistical characterization of aging (BTI and HCI) and RTN effects on both analog and digital circuits. It includes four large arrays of cells or circuit blocks: one array of SRAM and Sense Amplifier cells, one array of Analog Circuits cells and two of Ring Oscillators cells. Each cell of each array includes the circuit under test, the digital selection circuitry (for cell and operation mode selection) and the access circuitry that connects, when selected, the circuit in each cell to the output pads for testing.

Digital column and row decoders are used for row and column selection in each array. Each cell can be independently set into a different operation mode, depending on the type of test to be performed to that cell. The biasing and output measurement signals for each cell are accessed through independent analog pads.

Three operation modes can be set in each cell: 1) measurement mode, 2) stress mode, and 3) stand-by mode. In the first mode, the selected circuit is operated under nominal biasing conditions (Vdd = 1.2V in this technology), so that their performances can be measured. In the second mode, the circuits are stressed by applying an overvoltage to their terminals, so that circuits can be aged at a faster rate than during real-life operation (what is known as "accelerated stress" or "accelerated aging"). In the third mode, the stand-by mode, circuits are set into a state where no bias is applied, so that circuits are not aged unintentionally.

The SRAM and Sense Amplifier Array include 832 cells of a typical 6T-SRAM circuit and 104 cells of different types of Sense Amplifiers circuits, respectively. The Analog Circuit array contains 980 cells that include individual transistors with independent source and bulk connections (to study how aging and the substrate effect interact), inverters, current mirrors and single-stage amplifiers, all of them with different sizes and topologies. Finally, the Ring Oscillator array includes 480 cells with different Ring Oscillators topologies. All cells can be aged through accelerated stress by raising the biasing voltages in key circuit nodes or by raising the chip temperature. Differences in their circuit performances at nominal operating conditions when compared to those after a stress allow evaluating the degradation. Degradation at circuit level will be validated by the statistical characterization of aging and RTN effects performed for this technology in a previous circuit with arrays of P-MOS and N-MOS transistors, specially design for this type of characterization [1]. Therefore, this chip will be useful to characterize the impact of time-dependent variability effects at circuit level in different circuit blocks commonly used in many integrated circuits.

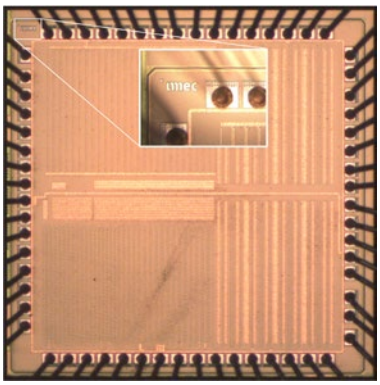


Fig.1: Picture of a wire-bonded chip

Reference

[1] J. Diaz-Fortuny et al., "A Versatile CMOS Transistor Array IC for the Statistical Characterization of Time-Zero Variability, RTN, BTI, and HCI," in IEEE Journal of Solid-State Circuits. Doi:10.1109/JSSC.2018.2881923

Why Europractice?

This chip is part of research project MARAGDA. In this project, a previous chip had to be first designed, fabricated and characterized in the same technology to evaluate the time-dependent variability of that technology. Therefore, it was important that the selected technology was supported for an extended period of time, so that all the steps of the project could consider the same technology. At the same time, we needed a well-established and commonly used commercial technology. EUROPRACTICE meets all these requirements at affordable prices for Universities and Research Centers.

Acknowledgements

This work has been supported by the TEC2013-45638-C3-R Project (funded by the Spanish MINECO and ERDF).

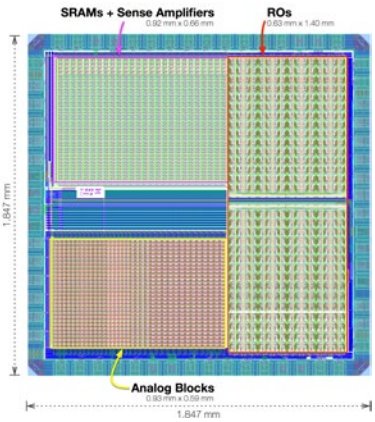


Fig.2: Layout view of the chip

ABACUS Asynchronous logic Based Analog Counter for Ultra fast Silicon strips

INFN, Sezione di Torino, Italy

Designers: Federico Fausti, Jonhatan Olave, Giovanni Mazza
E-mail: fausti@to.infn.it, olave@to.infn.it, mazza@to.infn.it
Technology: UMC L110AE Logic/MM/RF
Die size: 5.0mm × 5.0mm

Introduction

The MoVe-IT research project of the National Institute for Nuclear Physics (INFN) aims at the study of models for biologically optimized treatment planning systems in particle therapy and the development of dedicated devices for plan verification. On behalf of this collaboration, the Torino medical physics group is working at the development of a new prototype of silicon strips detector. This device, based on 50 µm thin silicon sensors with internal gain, aims to detect the single beam particle and count their number up to 109 cm^2/s fluxes, with a precision ≥ 99%. The prototype detector will cover a 3x3 cm^2 area, segmented in strips. The classic orthogonal strip positioning is used for beam profile measures. For what concerns the front-end electronics, the challenging tasks are represented by the charge and dynamic range which are respectively the 3-150 fC and the hundreds of MHz instantaneous rate (at least 100 MHz, 250 MHz ideally).

Device description

Given the novelty and the complexity of this problem, our group decided to explore the design and the production of two different front-end architectures, both having 24 channels: ABACUS_TIA and ABACUS_CSA (Asynchronous-logic-Based Analog Counter for Ultra-fast Silicon strips). The first architecture, ABACUS_TIA, is a high bandwidth TransImpedance Amplifier (TIA) based on a differential amplifier with resistive load and gain boost current sources, with a resistive feedback. Two flavours of the TIA solution have been designed and prototyped to address the project issues: a two stage TIA and a single stage TIA driven by a current buffer. The first solution reduces the effects of the input capacitance by increasing the open-loop gain, at the expense of increasing power consumption and a slightly decrease in speed. The second solution decouples the detector from the gain stage, thus providing a lower sensitivity to the input capacitance. The disadvantage is that the buffer stage provides an extra contribution to the noise.

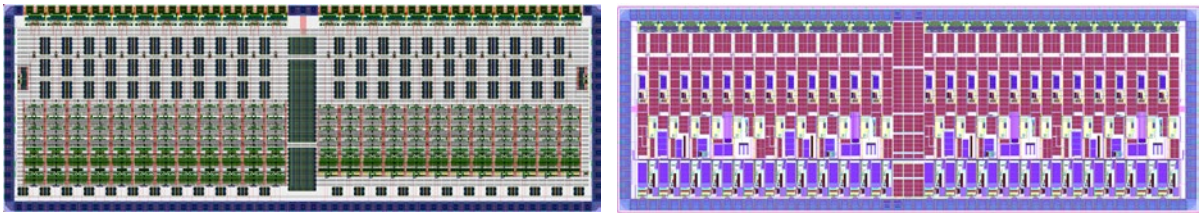


Fig.1: Two different front-end architectures of ABACUS

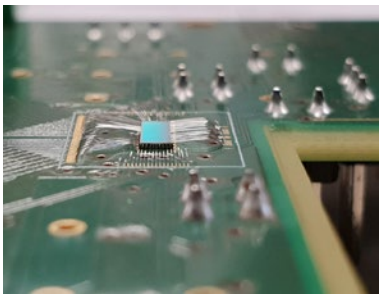


Fig.2: Picture of wire-bonded die at board level

The second architecture, ABACUS_CSA, is a fast Charge Sensitive Amplifier (CSA) based on a cascoded single ended amplifier with gain boost. In order to shorten the RC tail, a digital reset of the integrating capacitor has been implemented. The reset signal is automatically generated by the output comparator; a recovery system has been implemented to keep the reset signal width sufficiently large to effectively discharge the capacitor.

Local DACs have been implemented per channel for fine tuning of the comparator threshold. The discriminator output for both architectures is provided by a differential CML driver to maintain high signal rate.

Why Europractice?

The Italian National Institute for Nuclear Physics (INFN) has an historical partnership with Europractice, especially concerning the ASIC MPW runs for research applications, in the field of particle and radiation detectors. In these last decades, the role of Europractice became crucial in most of the INFN project management and scheduling activities, allowing several groups to study a detector development with intermediate prototypes.

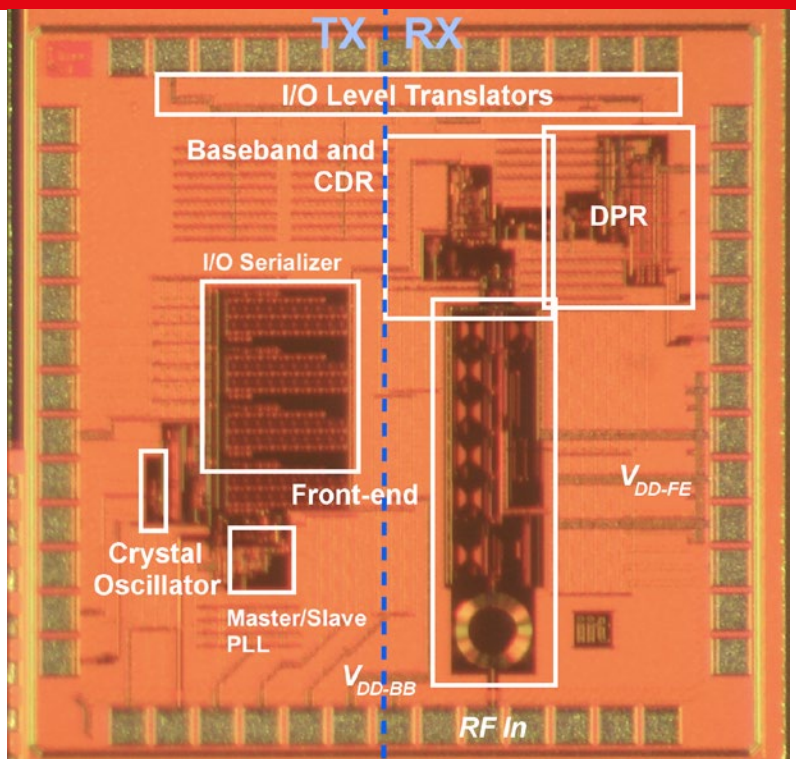


Fig.1: Picture of the die with indicated the main functional blocks

1Gbps Ultra-Wide-Band Transceiver for CMOS Neural Recording Applications

Istituto Italiano di Tecnologia (IIT) Electronic Design Laboratory (EDL),
Via Melen 83, 16152 Genova, Italy
Neuroscience and Brain Technologies (NBT),
Via Morego 30, 16163 Genova, Italy

Contact: Marco Crepaldi, Technologist, Istituto Italiano di Tecnologia, EDL (marco.crepaldi@iit.it), Giannicola Angotzi, NBT (giannicola.angotzi@iit.it), Luca Berdondini, NBT (luca.berdondini@iit.it).

Technology: UMC L130 MM/RF (mini@sic)

Die size: 1.525mm × 1.525mm

Description

The mini@asic (overall taped out twice) comprises a complete sub-meter IR-UWB transceiver comprising a 1Gbps transmitter and the corresponding pulse-based receiver, for applications exploiting large-scale neuronal interfacing with CMOS probes [1-2]. The transceiver is designed to enable the simplex real-time wireless transmission of neural recordings acquired with micro-arrays including up to 1024 active electrodes. The transmitter (TX, floorplanned on the left) achieves pulse synthesis using a double phase-locked loop (PLL) architecture. It generates 4 GHz center frequency OOK pulses that last 500 ps from a single 31.25 MHz crystal oscillator. Pulse synthesis is based on the use of a cascade of a master and a slave PLL with the latter locked to the former. Both PLLs are implemented with CMOS digital cells and ring oscillator-based VCO. The 130 nm RFCMOS chip operates at a measured 5 pJ/pulse energy budget for an active area of 0.04 mm². Input interfacing is provided by a full-custom serialization logic operating at 250 MHz with four 1.2-3.3 V external parallel channels (overall, multiplexing data to a 1 GHz serial line). From reset time, the master-slave transmitter achieves locking in a measured time of 450 ns, settling in 4µs, and the output pulses across the antenna load are generated with a 3.42 ps RMS jitter standard deviation. The obtained phase noise of a continuous OOK stream at 4 GHz, 1 MHz offset, is -93 dBc/Hz, respectively. The receiver (RX, floorplanned on the right), that has been specifically designed to acquire the pulses generated by the above TX, is an asynchronous threshold energy detector. The baseband circuit generates digital pulses that are synchronized with the transmitter clock using a double PLL-driven all-digital clock data recovery (CDR) and packet re-synchronizer, that automatically detect packets with a data-aided mechanism. The receiver occupies an active area of 0.34 mm², operates at 1.2 V supply, recovers synchronization errors in 30 ns, and, being part of the same transmitter design, it is fully driven by the same 31.25 MHz reference crystal. The complete system, including full-custom output serialization, high-current driver logic operating at 1 GHz on a 50 Ω load, crystal oscillator, and complete RF front-end and baseband, consumes a measured power consumption of 115 mW. TX-RX measurement results obtained in an office/laboratory environment using PCB antennas, demonstrate sub-meter over-the-air transmission at 1 Gbps in absence of RF filters for a $4.4 \cdot 10^{-3}$ packet error rate and $3 \cdot 10^{-3}$ synchronization error rate performance.

Associated publications

[1] M. Crepaldi, G. N. Angotzi, A. Maviglia, F. Diotalevi and L. Berdondini, "A 5 pJ/pulse at 1-Gpps Pulsed Transmitter Based on Asynchronous Logic Master–Slave PLL Synthesis", in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 3, pp. 1096-1109, March 2018.

[2] M. Crepaldi, G. N. Angotzi, A. Barcellona and L. Berdondini, "A 1 Gbps UWB OOK Receiver with Double PLL All-Digital CDR and Data Packet Re-Synchronizer", IEEE International Symposium on Circuits and Systems (ISCAS), Florence, 2018, pp. 1-5.

Why Europractice?

Europractice is one of the most efficient, valuable and cheapest ways to fast prototype integrated circuits for European research-based environments. Europractice, in particular with the support of IMEC to check physical design errors and for general support for fabrication, always enables well-controlled design time, efficiency and precious support during all prototyping phases. With the parallel providing of design tool service, EP represents a unique, and well consolidated means for the European researchers to make their application-specific designs come true to silicon.

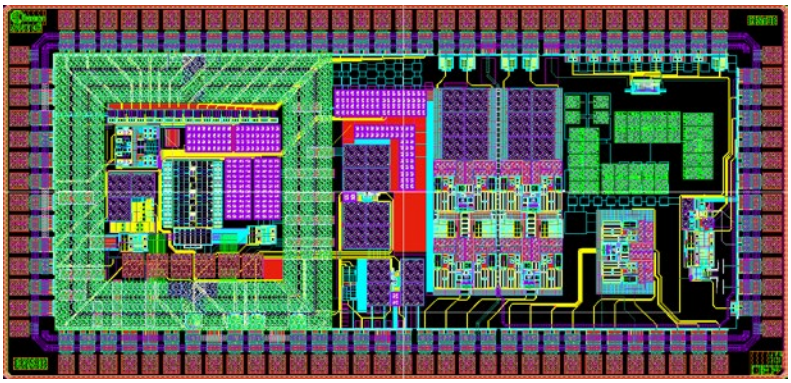


Fig.1: Layout of the designed circuit

A on-chip energy harvester system for low voltage applications

Department of IC Design and Test, Institute of Electronics and Photonics, Slovak University of Technology in Bratislava (Slovakia)

Supervisor: prof. Ing. Viera Stopjaková, PhD.

Designers: Daniel Arbet, Lukáš Nagy, Martin Kováč, Miroslav Potočný, Michal Šovčík, Matej Rakús, Lukáš Kohútka

E-mail: viera.stopjakova@stuba.sk, daniel.arbet@stuba.sk, martin_kovac@stuba.sk

Technology: UMC L130 MM/RF (mini@sic)

Die size: 1.525mm × 1.525mm

Introduction and Application

Nowadays, the demand for battery powered portable electronic appliances has been continuously growing. Majority of new devices in automotive industry, transport, wireless communication systems, medical science, and so on require intelligent, compact and energy saving solutions in the scale of integrated circuits (IC) for reasonable price. The basic requirement for portable devices is rather low power supply voltage (e.g. in the range of 250-500 mV [1]). Extended battery life and low power consumption have become the key parameters for microelectronic systems, especially in terms of growing trend of its fully energy autonomy ensured by energy harvesters (EH). Moreover, continuing miniaturization and increasing complexity of the specific devices as implanted medical gadgets also exerts the pressure on technology development and transistors shrinking to push design to more affordable cutting-edge technologies as low-cost CMOS process. The multidisciplinary character in packaging issue, sensors and processing unit implementation as well as wireless communication capability introduce new challenge to ensure reliability and reproduction of production process. For these reasons the scientific objectives of the prototype chip are focused on research, design and analysis of new effective methods for ultra-low voltage analog and mixed-signal IC design (VDD ≤ 0.6 V) as well as their implementation and application in affordable CMOS technologies with the power consumption and energy autonomy taken as a priority.

System Description

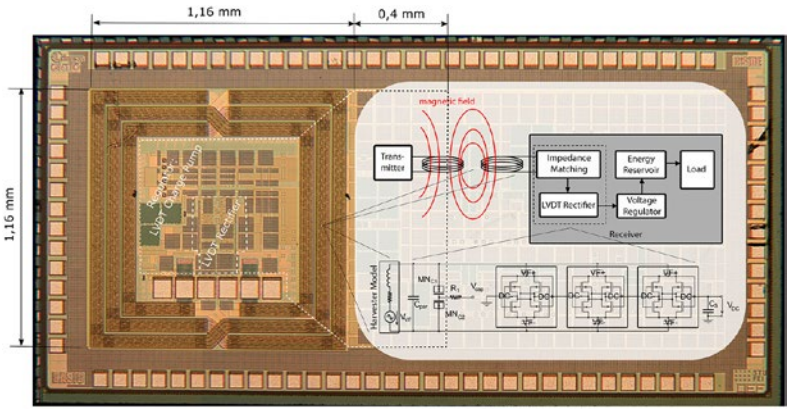


Fig. 2: Die photography of the fabricated chip

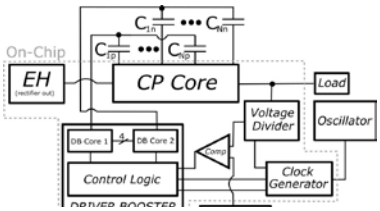


Fig. 3: Block diagram of EHS with detailed description of the voltage regulator

With the support of APVV 15-0254 [2] grant and Europractice under mini@asic program, the prototype chip (Figure 1) of the wireless, low-voltage energy harvester system (EHS) has been developed and fabricated in UMC 130 nm standard CMOS process under supervision of IC Design and Test department at Slovak University of Technology in Bratislava. EHS consists of a fully on-chip novel symmetrical topology of an inductor-like antenna that outperforms the standard few-turn spiral realizations at all key parameters, such as inductance and quality factor. Additionally, the designed symmetrical topology with central tap supported by a multi-layer and multi-stack structure brings new degree of freedom to the possibility of incorporating an innovative rectifier topology working in hundreds of MHz frequency band (in the prototype, about 200-240 MHz central frequency is considered). The electromagnetic field transfer energy was chosen as one of solutions allowing the on-chip implementation of EHS to improve production reliability omitting the influence of additional post-processing steps accompanied in Micro-Electro-Mechanical Systems (MEMS) or System-in-Package (SiP) development processes. The output of antenna (also called rectenna) is then followed by a low-voltage, dynamic threshold (LVDT) AC-DC full-wave voltage rectifier/multiplicator with a differential suppression of the threshold voltage by built-in in-line capacitors. The rectifier is equipped with non-adaptive impedance matching circuit and draws from the dynamic threshold design approach raised from triple-well CMOS process features. This introduces a new wind into ICs design in terms of low- voltage/low-power circuits such as for instance the before-mentioned medical applications (e.g. active implantable medical device) and let to increase power throughput across the proposed rectifier by lowering its input impedance by the control of substrate potential. To create the desired output DC voltage, the cross-coupled DT charge pump (Figure 2), which is characterized by its own low-voltage operational capability, has been employed. The charge pump utilizes power affable ON/OFF regulation feedback loop, especially designed for stern, low-voltage start-up conditions by a driver booster (DB). Together serve as the masters to control the charge pump output up to 600 mV, depending on level of the rectified DC voltage. Low-power character is also ensured by careful design of hysteresis based bulk-driven comparator and fully integrated switched-capacitor voltage divider omitting static power consumption.

Measurements and expected results

Up to now, only few measurements have been carried out, especially at the level of individual blocks. As previously mentioned, the symmetrical structure of the proposed antenna can improve performance of state-of-art realizations, where expected values are about 34% and 20% in case of inductance and quality factor, respectively. In terms of active device measurement, initial evaluation results show slight deviations from the simulation results. It is caused by the fact that the proposed ASIC works at ultra-low value of the supply voltage, and therefore all transistors are pushed into weak inversion region where their models (BSIM3v3) are not precise. The LVDT rectifier achieves the maximum power efficiency of 70% and can deliver up to -12 dBm of power at less than 300 mV input voltage amplitude. In the case of the regulated self-powered charge pump, we measured the capability of starting from the charged output capacitor (Figure 3).

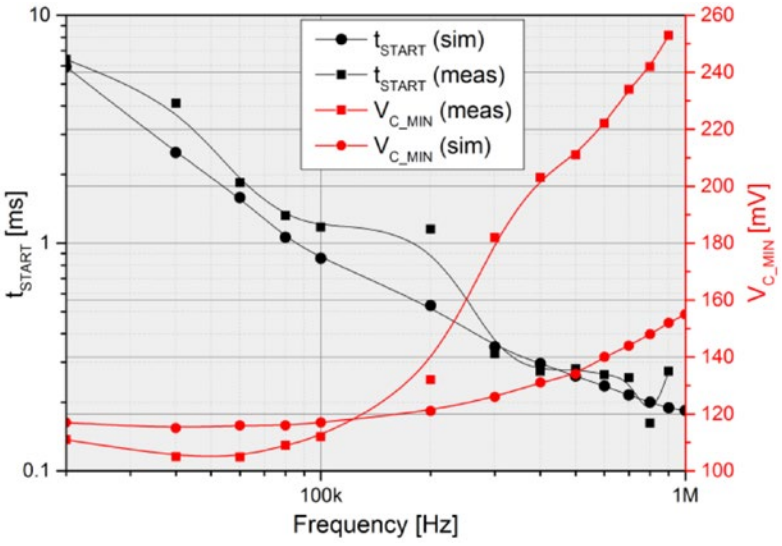


Fig. 4: Start-up measurement result of regulated self-powered charge pump

For the low value of switching frequency, the whole system can reliably start-up if the output capacitor (C=10 nF) will be charged at about 120 mV. For the switching frequency of 100 kHz, the start-up time will be about 1 ms.

In the ongoing measurements, we investigate the efficiency of the energy transfer from the external RF electromagnetic source to the proposed ASIC and the whole EHS as a single functional system.

Why Europractice?

Europractice offers our Department opportunity to design and fabricate through the mini@asic runs in the cutting-edge technologies for a very reasonable price. The selected technology was the best way to show that low-voltage EHS based on integrated inductor-like antenna can be implemented in the pure CMOS process. Our team would like to thank IMEC and Europractice IC service team for the high quality of technical support given from the layout phase to the packaging process.

Acknowledgement

This work was supported in part by the Slovak Research and Development Agency under grant APVV-15-0254 and by the Slovak Republic under grants VEGA 1/0762/16 and VEGA 1/0905/17.

References

[1] Nele Reynders and Wim Dehaene. Ultra-Low-Voltage Design of Energy-Efficient Digital Circuits. Springer, 2015.

[2] Slovak Research and Development Agency grant APVV 15-0254 (INSiDE): Development and implementation of analog integrated systems for ultra-low voltage applications http://deimos.elf.stuba.sk/projekty/inside/

HitDetectionCSA - An Analogue Transient Recorder ASIC with Charge sensitive Front End

GSI Helmholtzzentrum für Schwerionenforschung GmbH, Department for Experiment Electronics, Germany

Contacts: Harald Deppe, Holger Flemming, Peter Wieczorek
E-mail: h.flemming@gsi.de
Technology: UMC L180 MM/RF (mini@sic)
Die size: 3.24mm × 3.24mm

Description

The HitDetectionCSA ASIC is the latest descendant of a family of transient recording ASICs developed at GSI for particle detector readout in fundamental research. The main feature of HitDetectionCSA is an integrated charge sensitive amplifier (CSA) with an extreme large dynamic range.

The charge coming from a particle detector is integrated in the feedback capacitance of the CSA. For large amounts of charge additional capacitances are switched on dynamically to obtain the large dynamic range. The integrated charge leads to a voltage step at the output of the CSA as shown in figure 1. This voltage step is sampled and stored

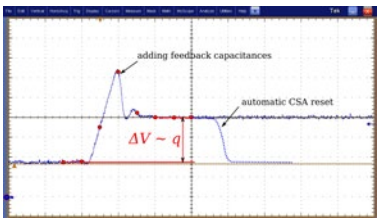


Fig.1: Voltage profile of the HitDetectionCSA

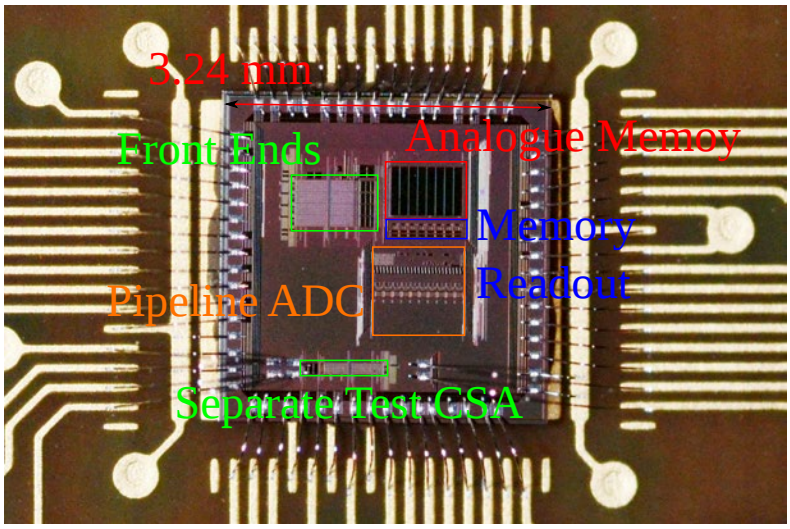


Fig.2: Picture of fabricated ASIC with the functional blocks indicated.

in the analogue memory of the transient recorder and after storing the CSA feedback is discharged.

After transient recording the memory is read out asynchronously and the transient is digitised by an integrated 12-bit pipeline ADC. Four CSA channels, the analogue memory with read out, the pipeline-ADC and a digital interface are integrated on the prototype ASIC which is shown in figure 2 with marked functional blocks.

Figure 3 shows the output voltage of the CSA as a function of the input charge. The output voltages increases with increasing input charge until approximately 1 V is reached. Then the next feedback capacitor is switched on. This pattern is repeated four times. When all capacitors are switched on the output signal saturates for the highest charges finally. The noise level corresponds to an input charge of 0.38 fC (2372 electrons) while the maximum charge is 42 pC. So the dynamic range of the CSA is 110000 which corresponds to 16.75 bits.

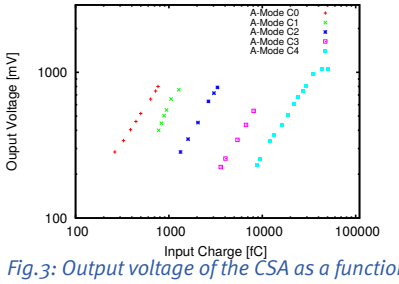


Fig.3: Output voltage of the CSA as a function of the input charge.

Why Europractice?

Several boundary conditions in particle physics detectors like space requirements, compact designs, radiation environment call for using microelectronics while the production volume as well as the budget is relatively small. Without EUROPRACTICE software and MPW service neither the CAD tools not the ASIC production would be affordable in our environment. So the Europractice service plays an important part in fundamental nuclear physics research.

Two modules on a test chip: i) Two-channel ECG and ETI (electrode tissue impedance) analog signal conditioning in the presence of motion artifact and ambient noise ii) Two-channel resistive sensor interface and signal conditioning system

Biomedical group, Department of Electrical Engineering, Indian Institute of Technology Bombay, India

Contact: Designers: Meraj Ahmad, Sourya Dewan and Maryam Shojaei Baghini
Supervisor: Prof. Maryam Shojaei Baghini
E-mail: mshojaei@ee.iitb.ac.in
Technology: UMC L180MM/RF (mini@sic)
Die size: 1525µm × 1525µm

Description

i) Two-channel ECG and ETI (electrode tissue impedance) analog signal conditioning in the presence of motion artifact and ambient noise

In ambulatory monitoring of ECG, where movement of the subject is not avoidable, a key technical challenge is to overcome the induced motion artifact in the ECG. Electrode-tissue interface impedance (ETI) is a quantity of significant interest in canceling the motion artifact from ECG recording using adaptive filtering techniques.

Test chip IITB_SENSOR_INTERFACE_SEPT_2017 was designed in UMC 180nm mixed- mode technology and a portion of the test chip is designed for

simultaneous measurement of electrode-tissue interface impedance and electrocardiogram. The layout view of the chip with labeled modules on the test chip, is shown in Fig 1.

As a part of the test chip, a low noise chopper stabilized programmable square wave current generator (range 100nA - 40μA) was designed for common mode current excitation to measure electrode-tissue interface impedance. The current sources were dynamically matched to minimize the offset current.

For simultaneous electrode-tissue impedance and ECG measurement, instrumentation amplifiers with cascaded Gm (trans-conductance stage) and TI (trans-impedance stage) were designed. The chopper-modulated instrumentation amplifiers with current balance topology for ETI and ECG were designed with ultra-low power (17.82μW and 22.5μW, respectively), low noise (in-band integrated noise of 1.1μV), and high-CMRR (mean 110dB).

A system prototype using the test-chip IITB_SENSOR_INTERFACE_SEPT_2017 was developed as shown in Fig 2. This prototype was used for simultaneous recording of ECG and ETI across subjects with motion artifact, of which one set of acquired signals is shown in Fig. 3.

ii) Two-channel resistive sensor interface and signal conditioning system

Micro Electro Mechanical Systems (MEMS) devices have been widely used in variety of applications such as physical, chemical, biological and environmental sensing applications. Piezoresistivity is a common sensing principle for MEMS based sensors and ΔR/R is an important parameter to be measured.

Test chip IITB_SENSOR_INTERFACE_SEPT_2017 was designed in UMC 180nm mixed-mode technology and a portion of the test chip was designed for multi-channel resistive sensor Interfacing and analog signal conditioning enabling ΔR/R measurements. The layout view of the test chip is shown in Fig. 1.

Two multipurpose instrumentation amplifiers with cascaded Gm (trans-conductance stage) and TI (trans-impedance stage) were designed. These amplifiers can be programmed as resistance to voltage convertor or as a voltage amplifier with or without noise reduction. A low noise chopper stabilized programmable square wave current generator (range 100n - 40μA) was also designed for common mode current excitation to measure ΔR and R. A novel flicker noise reduction technique was employed to measure ΔR/R as low as 10s of ppm. A 10 dB improvement of SNR is observed after enabling noise reduction with the ASIC as shown in Fig. 4.

Why Europractice?

Europractice provides students and research scholars access to the various semiconductor ASIC fabrication technologies to test and prototype their designs at affordable academic prices. Europractice gave us excellent technical support during the entire design cycle from the GDSII preparation to the submission stage

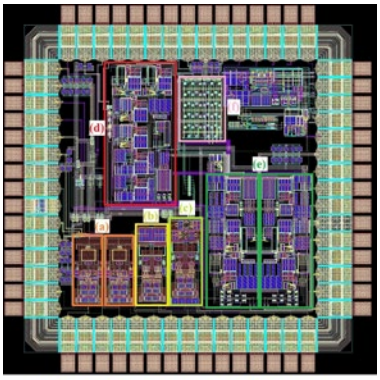


Fig.1: Layout view of the chip

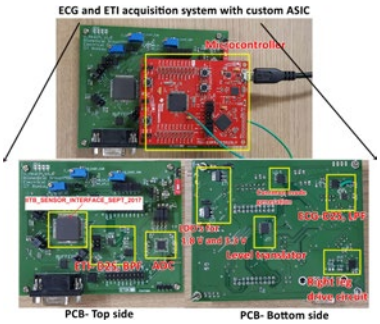


Fig.2: Pictures of the fabricated system prototypes (PCBs).

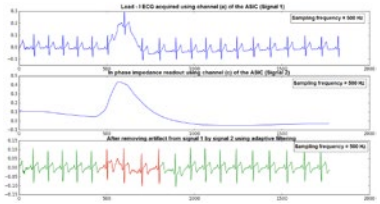


Fig.3: ECG and ETI measurement wave forms

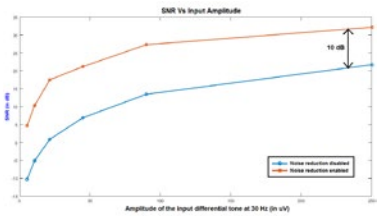


Fig.4: SNR comparison with and without noise reduction

and finally to the packaging stage. The entire procedure is well planned by the Europractice team.

Acknowledgements

- SMDP phase-III educational and research program (Chip-to-System) of MeitY, Government of India
- VLSI lab and SrijaTI lab of the Department of Electrical Engineering, IIT Bombay

Capacitive Intraocular Pressure Sensor (A First User Stimulation Design)

Centro Singular de Investigación en Tecnoloxías da Información, University of Santiago de Compostela, Spain

Contact: Paula López Martínez
E-mail: p.lopez@usc.es
Technology: MEMSCAP PolyMUMPS
Die size: 10mm × 10mm

Introduction

Glaucoma is one of the main causes of irreversible blindness in the world. Measuring the intraocular pressure (IOP) is one of the key factors in its early diagnosis and can help to slow down the spread of the disease. The goal of this work is the development of a small size and low-power implantable device to constantly monitor the IOP, defined as the difference between the pressure outside and inside the eye. The pressure sensor will be implanted inside of the eye, in the posterior chamber. To guarantee accurate measurements, the sensor must have a measuring relative pressure range of 0-60mmHg with a resolution of 1 mmHg.

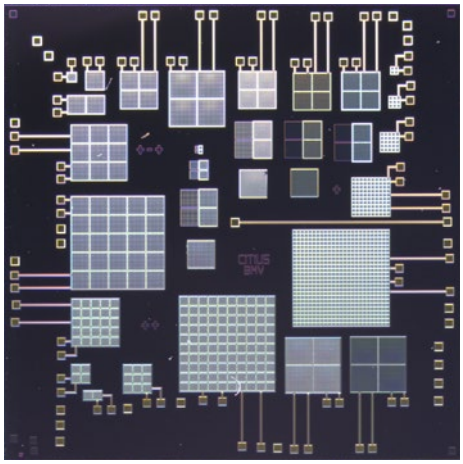


Fig. 1. Microphotograph of the fabricated chip

Description

With the aim of measuring the intraocular pressure we fabricated a set of capacitive sensors using the PolyMUMPS MEMSCAP technology. Different sensing principles were considered as well as different device sizes in order to find out the most convenient configuration. To build the sensing capacitor the following arrangements were considered: Poly2/Poly1, Poly2+Poly1/Polyo and Poly1/Polyo.

Why Europractice?

Europractice offers affordable and accessible access to foundry services to research institutions that could otherwise not easily support regular fabrication costs. The procedures to access the different technologies are clearly explained in their website and the online customer support is fast and trustworthy. Since our reported MEMS design was selected and financially supported by the First User Stimulation program, we also would like to thank the European Commission for their support.

Design of an Indirect-Drive Electrostatic Micro-mirror

University of Malta - Department of Microelectronics and Nanoelectronics, Msida, Malta

Designers: Russell Farrugia
Supervisor: Prof. Ivan Grech, Prof. Joseph Micallef
E-mail: russell.farrugia@um.edu.mt
Technology: MEMSCAP SOIMUMPs
Die size: 9mm × 9mm

Introduction

In this project, three scanning micro-mirrors were designed for high performance optical projection applications such as embedded pico-projectors and automotive head-up displays. The 1 mm-diameter scanning mirrors are operated at resonance using angular vertical comb-drive structures made possible by the SOIMUMPs process. The designs consist of support structures intended to minimize mirror dynamic deformation encountered during high frequency torsional oscillations. Figure 1 shows the layout of the complete chip, whereby duplicates of the mirror designs were included in order to measure the effect of the deposited reflective coating (SOIMUMPs Blanket Metal layer) on the static mirror curvature.

Description

A novel indirect-drive actuation method is incorporated in one of the mirror designs, as shown in Figure 2, in order to improve the actuation efficiency and hence reduce the required actuation voltage. Dynamically, the cou-

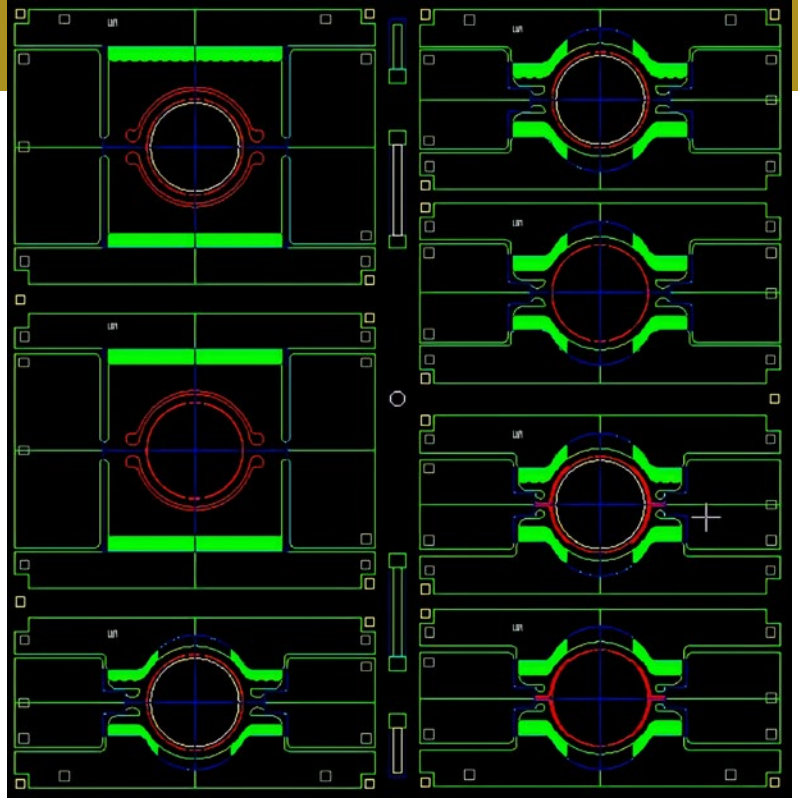


Fig. 1: Layout of the fabricated chip

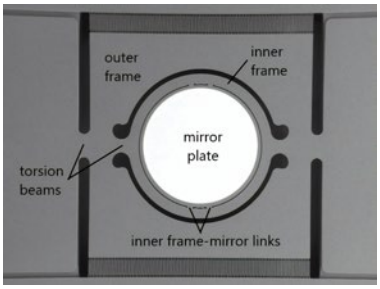


Fig. 2: SEM image of the indirect-drive resonant micro-mirror

pling between the mirror and an outer frame results in two torsional modes: in-phase and out-of-phase mirror rotation relative to the outer frame. At the out-of-phase mode, a small amplitude of the outer frame having a large inertial moment results in amplified micro-mirror rotation. The device is fabricated from a single 25 µm mono-crystalline doped-Si layer while a 3 µm finger gap is formed using deep reactive ion etching (DRIE). The micro-mirror design optimization was carried out using finite element (FE) and computational fluid dynamic (CFD) simulations in order to maximize the indirect-drive amplification factor and minimize the drive voltage amplitude. The non-linear harmonic response and the quality factor of the micro-mirror were evaluated using the optical measurement system shown in Figure 3, which, consists of a 2D position sensing detector (PSD), HeNe laser source and a high voltage amplifier.

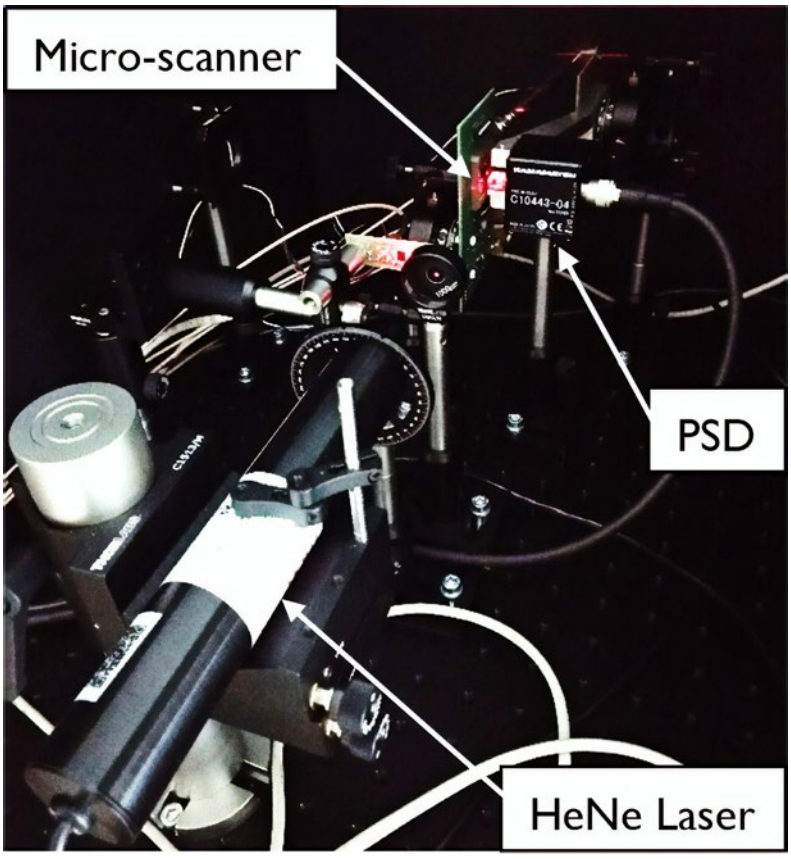


Fig. 3: Micro-scanner characterization using a PSD-based optical test bench

Why Europractice?

Europractice provides doctoral students, researchers and academics with access to state-of-the-art MPW foundry services for the fabrication of MEMS/MOEMS device prototypes. The University of Malta has always been provided with the necessary technical feedback and expertise at every stage of the chip design process.

Acknowledgements

The authors would like to acknowledge imec/Europractice for their support through the First User Stimulation Action of MEMS and Si-Photonics.

Silicon photonic integrated circuit for reconfigurable optical add /drop multiplexing

TECIP Institute, Scuola Superiore Sant'Anna, Italy

Contact: Vito Sorianello
E-mail: vito.sorianello@santannapisa.it
Technology: ISIPP50G – IMEC Si-Photonics (Active platform)
Die size: 5.15mm × 5.15mm

Description

We report on the design and fabrication activities of Silicon photonic integrated circuit based on reconfigurable optical add /drop multiplexing (ROADM) blocks. The device is realized in Silicon Photonics with a polarization diversity scheme in order to receive and operate with any arbitrary polarization coming from a standard single mode fiber (SMF-28). The polarization diversity scheme is implemented by using at the input ports consisting of dual-polarization grating couplers that split the incoming polarization state into two orthogonal states TE and TM that propagate on two identical paths. The same dual-polarization coupler is used at the output ports to recombine the two polarization components of the signals. Each path consists of a linear array of micro-ring resonator (MRR) based switching unit for adding or dropping the wavelength division multiplexing (WDM) signals to/from the network. The integrated ROADM is equipped also with 1x2 MRR based optical switches for the selection of the line path direction West to East or East to West. These switches allow the re-configurability of the network for path protection against fiber breaks. The design is based on the following device specifications: 8 WDM C-Band channels with 200GHz spacing, 25Gb/s NRZ channel bit rate, 1dB filter bandwidth 40 GHz (to support 25Gb/s NRZ channel bit rate), adjacent channel isolation: ›20dB, polarization insensitive I/O optical ports. The line switching unit is based on two main sections: a second order MRR filter on the main bus acts as the wavelength selective add/drop device, two single MRR at the output of the second order MRR filter constitute a 1x2 switching element which allows the selection of the line East or West propagation direction on the bus for the added or dropped channel. Each ring of the switching unit is provided with integrated silicon micro-heaters to set the microring resonance at the selected WDM wavelength, i.e. four electrical controls. Moreover, each I/O port and each switching unit are monitored by integrated SiGe photodetectors as power monitors for device calibration and to implement a closed loop control of the circuit. Three photodetectors for each switching unit and one photodetector for each port. Considering sixteen switching units (eight per polarization path), and ten I/O ports, the total amount of electrical control signals is 122.

The ROADM circuit has been designed on the base of the above specifications and compliant with the design rules and processes of the ISIPP50G active platform at IMEC (Belgium). In the designed ROADM we used custom designed building blocks as well as building blocks from the ISIPP50G technology library. The design is based on fully etched Si wires with 480 nm width and 220 nm height.

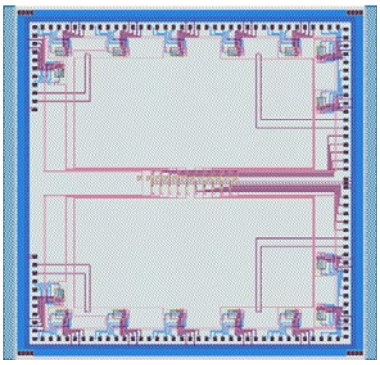


Fig. 1 : Polarization Insensitive ROADM Mask layout

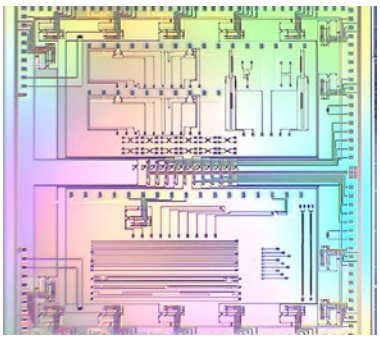
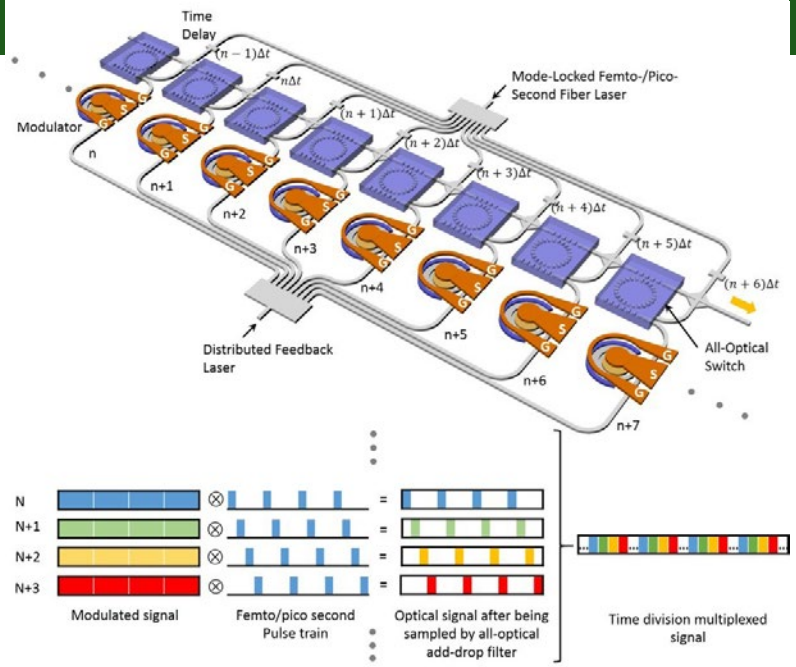


Fig.2: Optical microscope picture of the fabricated device

The mean radius of each microring of the add/drop filter is 6.2µm while the direction switch ring mean radius is 6.6µm. The resulting FSR of the switching unit is 1.8THz. In order to match the -1dB bandwidth specification, the coupling coefficient of the add/drop micro-rings is set to 19%, while the coupling coefficient of the switch microring is 18%.

Why Europractice?

Europractice allows easy-to-access multi-project-wafer (MPW) solutions for reliable prototyping of integrated circuits. Among the available processes, Imec ISIPP50G is a top-quality state-of-the-art technology for Silicon Photonics devices and circuits offering a consolidated photonic design kit (PDK) with active and passive devices up to 50Gb/s.



All-Optical Switch Enabled Ultrafast Time-Domain Multiplexing

Omega Optics Inc., Austin - TX, The United States of America

Contacts: Dr. Xiaochuan Xu, and Dr. Swapnajit Chakravarty
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Technology: imec-SiPhotonics iSiPP50G
Die size: 5150µm × 2500µm

Description

Even as the continuation of Moore's law comes in question, the increasing trend of network connections and bandwidth consumed is progressing exponentially with no foreseeable sign of halting. Service providers need to double their capacity every eighteen months to keep pace. Some sources estimate that the total amount of content passing through the world's networks will increase from 800,000 petabytes in 2009 to 35 zettabytes in 2020, meaning that by the end of this decade, service providers will need an astonishing 44 times the capacity they have in 2009. Including even more carrier wavelengths in the wavelength division multiplexing (WDM) system is unrealistic due to the inhibitive system complexity and significantly reduced non-regeneration distance. Considering a single wavelength could potentially transport signals at a speed up to tens of Tbps, increasing data rate of each carrier wavelength becomes an apparent choice. The data rate of a single carrier is primarily limited by the time division multiplexing, which currently relies on electronic devices. As the single carrier data rate continues to increase, electronic devices must be abandoned if speeds greater than 1 Tbps are to be feasibly obtained. All-optical multiplexing and de-multiplexing are the only solution.

Fig.1 is the schematic of the time domain multiplexing. Light from a distributed feedback laser is split into N channels. Each channel is modulated by electrical signal at a speed of D Gbps. The pulse train from a mode-locked fiber laser with D GHz repetition rate and 1 ps pulse width is also split into N channels and a time delay of (n-1) ps is introduced into n-th channel. The pulse train is used to periodically turn on the THz all-optical switch and couple the D Gbps signals into the bus waveguide while reducing the signal duration from 100 ps to 1 ps and adding a time delay of (n-1) ps. A 1 Tbps signal is obtained by combining N=100 channels with time delay spacing of 1 ps and D=10. This tape out includes a proof-of-concept four-channel time-domain multiplexer and isolated components for testing purpose. Each channel in the multiplexer is comprised of a standard high speed ring resonator modulator in the PDK and an ultrafast and low power consumption all-optical switch designed by Omega Optics Inc. Each channel is capable of carrying signals up to 50 Gbps. In total, the MUX could generate 200 Gbps digital signal.

Fig.1: Concept of the time-domain multiplexing

Why Europractice?

Omega Optics Inc. has been using the Multi-Project Wafer prototyping of Europractice since 2013. It allows us to get access to leading edge IC technologies at an affordable price. The Silicon photonics PDK provides a complete set of photonics components. The quality of the fabrication is impressive. The staff is always there to answer questions. It is wonderfully suitable for small businesses and academic institutions.

Acknowledgement

The research was sponsored by the US Department of Energy under the small business innovation research grant DE-SC0013178

Silicon photonic integrated circuits for photon-pair generation and filtering

Photonic Components Research group, ETRI, Korea

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E-mail: jongmool@etri.re.kr
Technology: imec-SiPhotonics Passives
Die size: 5.15mm × 5.15mm

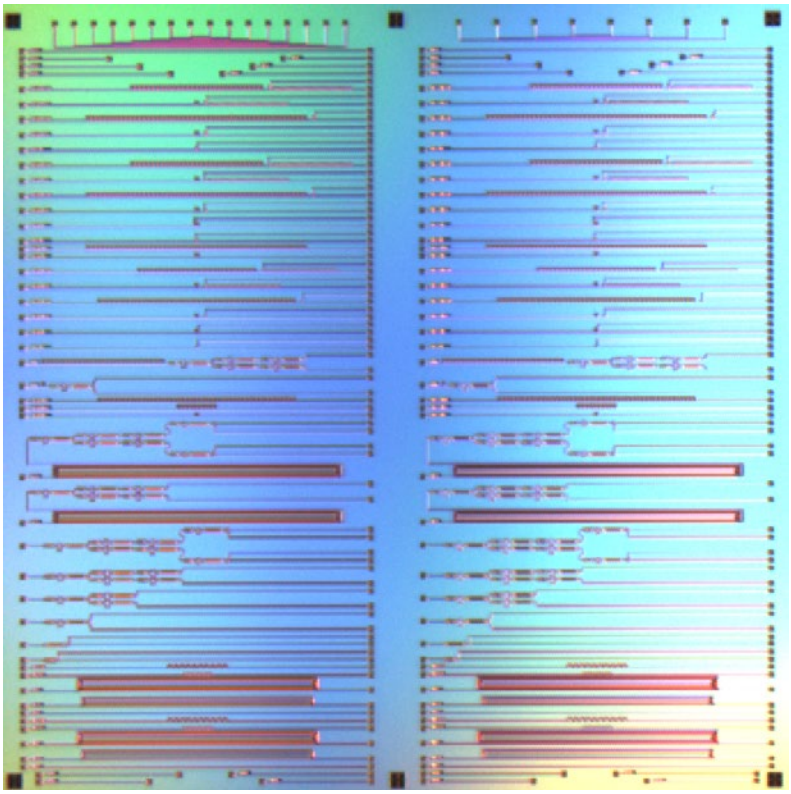

Fig.1: Microscope image of the fabricated chip.

Description

Silicon photonics technology is an attractive candidate to realize a quantum information processing platform by integrating quantum-correlated photon-pair sources, wavelength filters, and quantum interference circuits, etc. Quantum-correlated photon pairs can be generated based on spontaneous four-wave mixing (SFWM) with a strong pump field through a silicon-waveguide ring resonator or a long length of the silicon waveguide. High-extinction wavelength filters are required to separate the photon pairs from the pump and other background noises. Mach-Zehnder interferometers (MZIs) and splitters are also required in the quantum information processing.

We used imec-SiPhotonics Passives technology to design and demonstrate silicon photonic circuits to test the combination of the photon-pair sources and the wavelength filters. Various type of ring resonators and waveguide spirals are designed for the photon-pair generation. Cascaded MZIs and multiple ring resonators are designed for the wavelength filtering. The design includes the various combination of the photon-pair sources and the wavelength filters. The test results of the fabricated chips are showing a positive prospect for the integration of the photon-pair sources and the wavelength filters. We will use the results for our research toward the quantum information processing platform.

Why Europractice?

I have experienced the Europractice as the best way to use Multi Project Wafer (MPW) services on silicon photonics, for many years. The Europractice provides very well organized procedure to access the technology with Process Design Kits (PDKs) supported by several design tools for the users to select their favorite design tool. The Europractice service has been always open to questions and suggestions related to submission, delivery and billing.

Acknowledgement

We acknowledge the financial support by the Korean Ministry of Science and ICT (MSIT) under the grant 20170000740011001.

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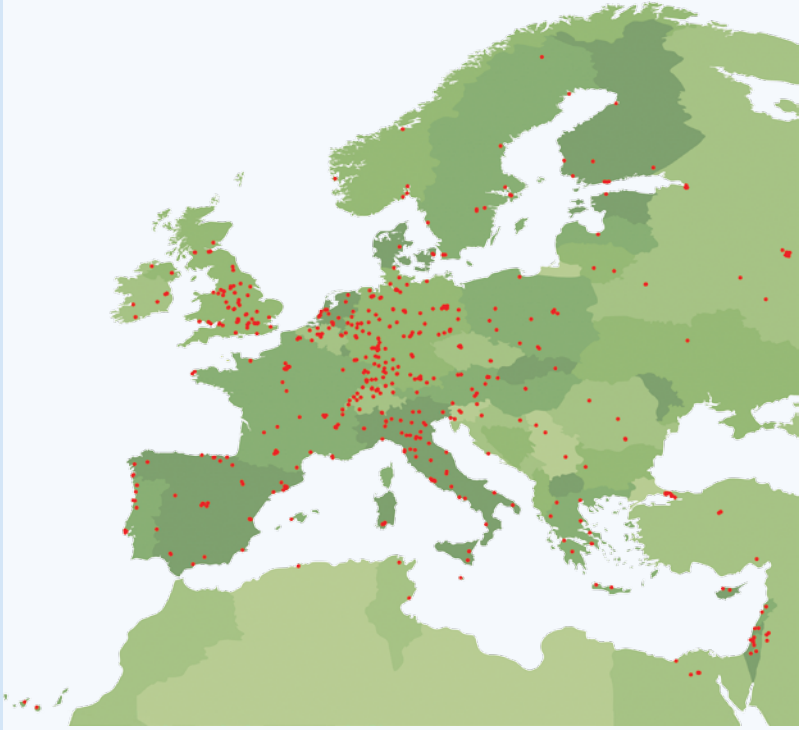

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A36440	Universität des Saarlandes
A35990	Universität Duisburg-Essen
A35830	Universität Hamburg
A14740	Universität Kassel
A14310	Universität Kassel - Fachbereich Elektrotechnik/Informatik
A14920	Universität Konstanz

A37500	Universität Paderborn
A39220	Universität Rostock
A38220	Universität Siegen
A39110	Universität Stuttgart
A37540	Universität Ulm
A39770	Universität zu Lübeck
A16090	Westfälische Hochschule

Ghana

A14770	Kwame Nkrumah University of Science & Technology

Greece

A39280	Aristotle University of Thessaloniki
A14150	Athens University of Economics and Business
R20790	Demokritos, National Center for Scientific Research
R21080	Foundation for Research and Technology Hellas
A37550	National and Kapodistrian University of Athens
A35140	National Technical University of Athens
A39490	Technical University of Crete
A15110	Technological Educational Institute of Western Macedonia
A13690	Technological Educational Institute Stereas Elladas
A00530	University of Ioannina
A37680	University of Patras
A35960	University of Patras - Electrical and Computer Engineering
A14340	University of the Peloponnese
A13550	University of Thessaly

Hungary

A40010	Budapesti Muszaki és Gazdaságtudományi Egyetem
A47540	Pázmány Péter Katolikus Egyetem

Ireland

A01190	Cork Institute of Technology
R22400	Dublin Institute for Advanced Studies
A13410	Institute of Technology, Carlow
A39310	Institute of Technology, Tallaght
A36490	Trinity College Dublin
R21720	Tyndall National Institute
A35300	University College Cork
A15730	University College Dublin
A36510	University of Limerick

Israel

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A13910	Ben-Gurion University of the Negev
A14690	Holon Institute of Technology
A15190	Jerusalem College of Technology
A14540	Kinneret College on the Sea of Galilee
A14070	Ort Braude College of Engineering
A13330	Technion - Israel Institute of Technology
A14380	Tel-Aviv University
A13240	The Hebrew University of Jerusalem

Italy

R21300	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi
R21800	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi Roma
R20550	Elettra-Sincrotrone Trieste
R22450	European Gravitational Observatory
R00140	Fondazione Bruno Kessler
R22430	INFN Laboratori Nazionali Del Sud
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R22390	Instituto Nazionale di Fisica Nucleare Sezione di Perugia
R22070	Instituto per lo Studio dei Materiali Nanostrutturati
R21600	Istituto Italiano di Technologia
R22040	Istituto Nazionale di Astrofisica - IASF, Milano
R22120	Istituto Nazionale di Astrofisica - Istituto di Radioastronomia - Radiotelescopi di Medicina
R22010	Istituto Nazionale di Astrofisica Osservatorio Astronomico di Cagliari
R21570	Istituto Nazionale di Astrofisica, Istituto di Radioastronomia
R21160	Istituto Nazionale di Astrofisica, Osservatorio Astrofisico di Arcetri
R22490	Istituto Nazionale di Fisica Nucleare
R21190	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali del Gran Sasso
R20450	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali di Frascati
R20580	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali di Legnaro
R20710	Istituto Nazionale di Fisica Nucleare, Sezione di Bari
R20400	Istituto Nazionale di Fisica Nucleare, Sezione di Bologna
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R20990	Istituto Nazionale di Fisica Nucleare, Sezione di Ferrara
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R22200	Radio Analog Micro Electronics srl
A15070	Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna
R21940	The Abdus Salam International Centre for Theoretical Physics
A39410	Università degli Studi dell'Aquila
A12990	Università degli Studi di Bergamo
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A16080	Yarmouk University

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R40030	Instytut Technologii Elektronowej
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A47300	Politechnika Gdanska
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A60160	Bauman Moscow State Technical University - Kaluga
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A48110	Far Eastern State Transport University
A47810	Lomonosov Moscow State University
A60060	Mordovian State University named after N.P.Ogarev
A48040	Moscow Institute of Physics & Technology (MIPT) - Control Systems
A47850	Moscow Institute of Physics & Technology (MIPT) - Wireless Technologies
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A60170	Moscow State Technical University of Radioengineering, Electronics and Automation
A60110	National Research Nuclear University MEPHI
A47520	National Research University of Electronic Technology (MIET)
A60240	National University of Science & Technology 'MISiS'
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A40240	Vladimir State Technical University named after Alexander and Nikolay Stoletovs
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A47820	Univerza v Mariboru

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A14560	University of Pretoria

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R20850	Centre Tecnològic de Telecomunicacions de Catalunya
R21910	Centro de Acústica Aplicada y Evaluación No Destructiva
R21740	Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
R22100	Centro Nacional de Supercomputación, Barcelona
R00060	CNM - Instituto de Microelectrónica de Barcelona
R22460	Consorcio ESS Bilbao
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R20700	Ikerlan
R21550	Institut de Ciènces Fotòniques
R21520	Institut de Ciències de L'Espai
R21230	Instituto de Fisica Corpuscular
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A37330	Universidad Complutense de Madrid
A13340	Universidad de Alcalá
A35891	Universidad de Cantabria
A12590	Universidad de Castilla - La Mancha
A15370	Universidad de Deusto
A39080	Universidad de Extremadura
A38590	Universidad de Granada
A14720	Universidad de La Laguna
A38780	Universidad de Las Palmas de Gran Canaria - Departamento de Informàtica y Sistemas
A36390	Universidad de Las Palmas de Gran Canaria - Instituto Universitario de Microelectrónica Aplicada (IUMA)
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A38600	Universidad de Navarra
A13860	Universidad de Salamanca
A37080	Universidad de Santiago de Compostela
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A38790	Universidad de Zaragoza - Facultad de Ciencias
A37690	Universidad del Pais Vasco
A12320	Universidad Politécnica de Cartagena
A38820	Universidad Politécnica de Madrid - Centro de Electrónica Industrial
A35130	Universidad Politécnica de Madrid - Departamento de Ingeniería Electrónica
A39100	Universidad Pública de Navarra
A36250	Universitat Autònoma de Barcelona
A39390	Universitat Autónoma de Madrid
A38660	Universitat de Barcelona
A38360	Universitat de les Illes Balears
A13150	Universitat de València
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A15100	Universitat Politècnica de Catalunya - Manresa
A35190	Universitat Politècnica de València
A16290	Universitat Pompeu Fabra
A39180	Universitat Rovira i Virgili
A16340	University of Vigo - AtlanTTic

Sweden

R20690	Acreo Swedish ICT AB
A38670	Chalmers Tekniska högskola
R21990	European Spallation Source
R22140	European Spallation Source ESS AB
R22050	Institutet för Rymdfysik
A38180	Kungliga Tekniska högskola, Kista
A16360	Kungliga Tekniska Hogskolan, Stockholm
A37350	Linköpings universitet
A00260	Luleå tekniska universitet
A37370	Lunds universitet
A39840	Mittuniversitetet
A16350	Stockholms universitet
R20910	Totalförsvarets forskningsinstitut FOI
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R20680	Centre Suisse d'Electronique et Microtechnique - Neuchâtel
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich
A14780	École d'Ingénieurs et d'Architectes de Fribourg
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A36110	École Polytechnique Fédérale de Lausanne - Microelectronics Systems
A37340	École Polytechnique Fédérale de Lausanne - Neuchâtel
R22180	Eidgenössische Materialprüfungs- und Forschungsanstalt
A38310	Eidgenössische Technische Hochschule Zürich
A38800	Eidgenössische Technische Hochschule Zürich - Basel
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R20800	Paul Scherrer Institut
A05000	Scuola Universitaria Professionale della Svizzera Italiana
A13090	Università della Svizzera Italiana
A15480	Universität Basel
A15530	Universität Bern
A12920	Universität Zürich
A13630	Université de Genève

The Netherlands

R20520	ASTRON Netherlands Foundation for Research in Astronomy
A15420	Erasmus Universitair Medisch Centrum Rotterdam
R20430	European Space Agency - ESTEC Microelectronics
R20540	European Space Agency - ESTEC Payload Technology
R00280	Nikhef
A12650	Radboud Universiteit Nijmegen
A14510	Rijksuniversiteit Groningen
R21250	SRON Netherlands Institute for Space Research
R21200	Stichting imec Nederland
A35701	Technische Universiteit Delft
A38050	Technische Universiteit Eindhoven
R20370	TNO-FEL
A00170	Universiteit Twente - CAES
A35491	Universiteit Twente - Electrical Engineering
A15960	Universiteit van Amsterdam
A12010	Vrije Universiteit Amsterdam

Tunisia

A12930	École Nationale d'ingénieurs de Sfax
A15300	École Nationale d'ingénieurs de Tunis

Turkey

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A15680	Ankara Yildirim Beyazit Üniversitesi
A39170	Bogaziçi Üniversitesi
A13270	Hacettepe Üniversitesi
A38270	Ihsan Dogramaci Bilkent Üniversitesi
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A16250	Istanbul Medipol Üniversitesi
A15610	Istanbul Sehir Üniversitesi
A37960	Istanbul Teknik Üniversitesi
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A15280	Orta Dogu Teknik Üniversitesi Kuzey Kibris Kampusu
A15970	Özyegin Üniversitesi
A13010	Sabanci Üniversitesi
A15260	T.C. Okan Üniversitesi
A13530	TC Kocaeli Üniversitesi
A14730	TOBB Ekonomi ve Teknoloji Üniversitesi
R38860	Türkiye Bilimsel ve Teknik Arastirma Kurumu -BILGEM
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A14250	Yeditepe Üniversitesi

UK

A39450	Aston University
A36280	Brunel University
A15450	Cardiff University
A15790	City University London
A16000	Coventry University
A16050	Cranfield University
R22090	Culham Centre for Fusion Energy
R20950	Diamond Light Source
A35160	Heriot-Watt University
A13480	Imperial College London
A36342	Liverpool John Moores University
A38450	Loughborough University
A37900	Manchester Metropolitan University
A35330	Newcastle University
A15850	Nottingham Trent University
A38040	Oxford Brookes University
A14980	Queen Mary College of London
A37490	Queen's University of Belfast
A13510	Royal Holloway University of London
A35030	Sheffield Hallam University
A14030	Staffordshire University
R20600	STFC Daresbury Laboratory
R00050	STFC Rutherford Appleton Laboratory
R22030	STFC UK Astronomy Technology Centre
A37660	Swansea Metropolitan University
A37870	Swansea University
A15390	The Open University
A13520	University College London
A12480	University of Bath
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A36000	University of Bristol
A35780	University of Cambridge
A12260	University of Dundee
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A37420	University of Edinburgh
A35440	University of Essex
A39440	University of Glasgow
A37600	University of Hertfordshire
A37400	University of Huddersfield
A35410	University of Hull
A35630	University of Kent
A37730	University of Leeds
A14760	University of Leicester
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EUROPRACTICE

All information for fabrication support, MPW run schedule, prices, etc. is available on our WEB site
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