

The background of the cover is split vertically into two colors: blue on the left and yellow on the right. Both sides feature a pattern of microprocessors. The blue side shows a grid of smaller, lighter-colored chips, while the yellow side shows larger, more detailed chips with a grid of gold pins. The text 'ACTIVITY REPORT 2016' is centered in the middle of the image, overlaid on the yellow background.

ACTIVITY REPORT 2016



EUROPRACTICE

EUROPRACTICE IC SERVICE

ASIC DESIGN AND MANUFACTURING FOR INDUSTRY AND ACADEMIA

EUROPRACTICE was launched by the European Commission in 1989 to help companies improve their competitive position in world markets by adopting ASIC, Multi-Chip Module or Microsystems solutions in the products they manufacture. The program helps to reduce the perceived risks and costs associated with these technologies by offering potential users a range of services, including initial advice and ongoing support, reduced entry costs and a clear route to chip manufacture and product supply. The ultimate goal of EUROPRACTICE is to enhance European industrial competitiveness in the global marketplace. Their services are open to industrial companies (especially SMEs), research institutes and academic users.

SERVICES OFFERED TO EUROPEAN ACADEMIC INSTITUTIONS:

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by offering 650 European universities and research institutes affordable access to the latest IC (Integrated Circuits) design tools and technologies. This is reflected in the training provided to universities from which the best IC design engineers emerge, essential for the SMEs innovation in new IC products.

- Affordable access to industry-standard and state-of-the-art CAD tools
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- Low-cost prototyping in various technologies (both ASIC and More than Moore) via MPW runs
- Training courses in advanced design flows

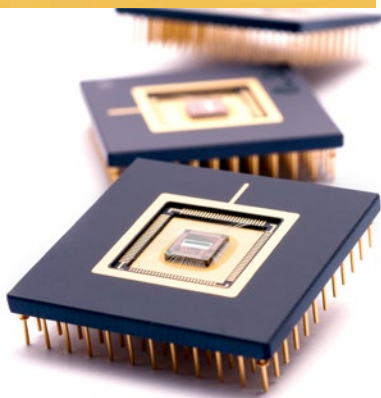
IC SERVICES OFFERED TO THE GLOBAL INDUSTRY:

EUROPRACTICE also offers industry worldwide access to microelectronic and microsystem design services, MPW prototyping, small volume production, packaging and test operations. Note, this does not include access to design tools.

Industry from all over the world have rapidly discovered the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who do not always need the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise. This you can get all from EUROPRACTICE IC service, a service that is already established for 20 years in the market.

THE EUROPRACTICE SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:

- imec, Leuven (Belgium)
- Fraunhofer-Institut für Integrierte Schaltungen (Fraunhofer IIS), Erlangen (Germany)
- STFC Rutherford Appleton Laboratory (United Kingdom)



FOREWORD

Dear EUROPRACTICE customers,

Another successful year has passed, in which we supported a record-number of customers and realized a total of 575 tape-outs in a wide range of technologies. 75% of the designs were sent in by European universities and research institutes while the remaining 25% of the designs were sent in by non-European universities and commercial companies world-wide. The on-going trend pushing towards smaller technologies also continued in 2016, where a record-high number of 28nm designs were realized and where we also started to offer the 22nm FDSOI technology from Globalfoundries. Also in 2017 and the years to come we will continue to innovate our offering both for the IC technology and for the design tools.

Thanks to the continuous innovation of EUROPRACTICE service to about 650 European universities and research institutes and to more than 300 small and medium-sized companies, Europe can remain competitive and its industry can accelerate their businesses. Europe needs a vibrant high-tech sector to boost its economy across all other industries and application domains.

In order to stimulate European universities to design a first IC in standard 0.18 μ technology or to start a first IC in an advanced technology (90nm and beyond), a first-user stimulation action was launched at the end of 2015. Early 2016, the selection was concluded and 10 best design proposals in each category were awarded a free or highly-reduced prototype fabrication by the EUROPRACTICE2013 EC-funded project. 8 Very First Users and 7 First Advanced Users managed to tape-out their designs on a *mini@sic* run before 30 September 2016, which is a very nice result. Some examples of these selected designs are described further in this report.

After the success of this first stimulation action in EUROPRACTICE2013, two new Stimulation Actions for FIRST USER European EUROPRACTICE university members were defined as a part of the EUROPRACTICE2016 project funded by the European Commission. Once more the 10 best design in the two categories were selected by an Independent Committee. The designs are expected to be realized in silicon in the course of 2017.

We thank the European Commission (DG Connect) for their continuous support. The current EUROPRACTICE 2016 project will run till 30 June 2018 and last year already a new successor project proposal was submitted to secure the EC funding till mid-2020 (although the decision for funding is still pending). The EC funding and the membership fee from more than 650 academics (universities and research institutes) ensures that we can continue our commitment to continue the EUROPRACTICE service and to offer our members with easy and affordable access to state-of-the-art design tools and to IC technologies.

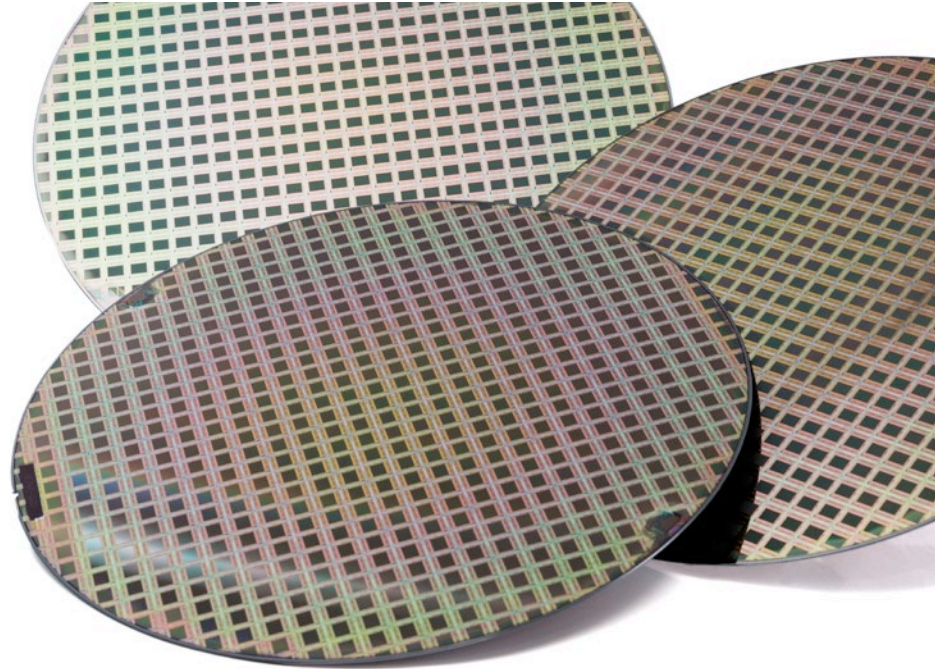
Last but not least, we thank all of you, our customers; universities, research institutes and companies over all the world for using our service and we wish you a successful 2017.

Looking forward to another record-breaking year.

Romano Hoofman (project manager EUROPRACTICE2016)
and the entire Europractice team

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EUROPRACTICE SERVICES

NOW ACTIVE FOR MORE THAN 25 YEARS

The European Commission has financially supported broker services that offer the European universities, researchers appropriate access to CAD tools, advanced technologies, design kits, IP blocks and training to support their education, prototyping and small volume production. These services have been offered by EUROCHIP (1989-1995) and multiple phases of EUROPRACTICE projects (1995-present) and are widely recognized as world-leading.

Currently approximately 650 academia from the EU member States and "extended" Europe are supported by this EUROPRACTICE service funded by the EC.



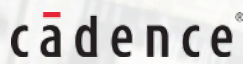
ELIGIBLE INSTITUTIONS ARE CURRENTLY ABLE TO ACCESS:

THE CAD SERVICES

Institutes in the Member States of the European Union plus those in European countries that are presently associated to Horizon 2020 (Albania, Bosnia-Herzegovina, Croatia, Iceland, Israel, Liechtenstein, Faroe Islands, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Serbia, Switzerland, Turkey) plus those from International Cooperation Partner Countries but limited to African, Eastern Europe and Central ASIA (EECA), Mediterranean Partner Countries (MPC) and Western Balkan Countries (WBC) are welcome to apply. Distribution of CAD tools is also subject to the following additional conditions: all export regulations apply and the EDA vendor must additionally approve distribution to all Research Institutes and Universities that are not in EU Member States.

THE MPW IC PROTOTYPING SERVICE AT DISCOUNTED PROTOTYPING PRICES

Those in the Member States of the European Union plus those in European countries that are presently associated to Horizon 2020 (Albania, Bosnia-Herzegovina, Croatia, Iceland, Israel, Liechtenstein, Faroe Islands, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Serbia, Switzerland, Turkey) plus those from International Cooperation Partner Countries but limited to the Eastern Europe and Central Asia (EECA) and more specific restricted to Belarus, Russia and Ukraine. For all these countries, Dual-Use Goods export license restrictions and foundry approval apply. For completeness: institutions from other countries world-wide can use the service at normal non-discounted prices as we restrict discounted prices to the wider-Europe.

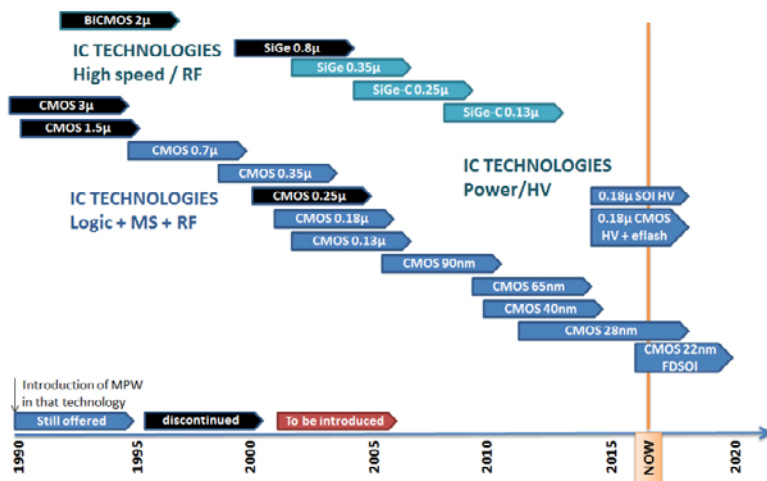


AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated low cost prices with the major CAD vendors world-wide and also with IP and programmable device vendors. Consequently, European academic institutions can purchase EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics, ...) design at very low prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service also provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows them to participate easily in EC-funded projects, ranging from IP block and component design to complete system design, working together with their peer institutes and industrial partners.

MPW PROTOTYPING FOR CUSTOMIZED ASICS



In general, foundries are not willing to give access to their fabrication lines to academic institutes and small companies due to the high level of technical support required, unless a high-volume production is guaranteed – which is not the case for university prototype fabrication or SME small volume needs.

Over the last 15 years, leading IC-foundries have recognized that EURORACTICE is the ideal partner to offer MPW services to smaller users and academia as EURORACTICE is the entity that offers both access and technical support (and the foundry does not need to bother with the large scale of users). Currently, 5 of the 7 foundries have ASIC manufacturing facilities in Europe (namely OnSemi, ams, IHP, X-FAB and GLOBALFOUNDRIES).

The EURORACTICE IC Service watches closely not only the evolution in scaling logic CMOS technologies but also the evolution of new add-ons for the standard CMOS technology such as SiGe, RF, SOI, etc. MPW runs in new and/or add-ons in existing technologies will be installed when there is sufficient demand from its users and when financially viable. Over the last 20 years, new technologies have been introduced by EURORACTICE (and EUROCHIP 1989-1995) from 3μ to 22nm today.

The EURORACTICE-PLUS partners have installed a comprehensive support infrastructure with the following tasks:

1. Negotiating with foundries and cell library vendors to introduce new technologies and associated new or updated technical information (documentation, design kits, cell libraries),
2. Checking new design kits and adapting existing design kits received from the foundry to CAD versions,
3. Completion of NDAs with academics in order to distribute the design kits and libraries (currently more than 4000 NDA's in place),
4. Distribution of design kits and libraries under NDA control,
5. Providing technical support to European Academia for teaching and IC design on the different design flows in the different CAD tools, cell libraries (models, cell information, RAM, ROM, spice parameters, models, ..), technologies issues (thickness of layers, specific characteristics, special process information not available in the standard documentation, ...), and also checking of their designs before fabrication.

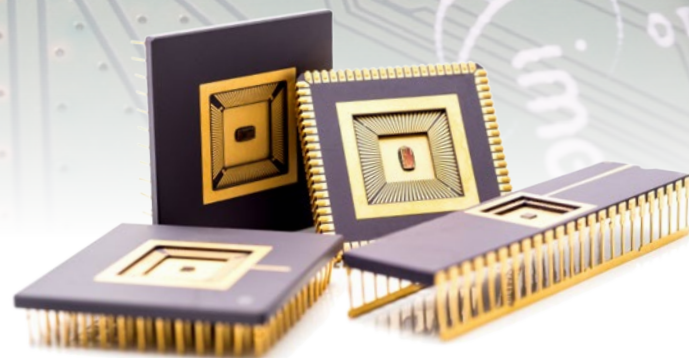
MPW PROTOTYPING FOR MORE-THAN-MOORE TECHNOLOGIES

For several years, EURO PRACTICE has offered CAD tools and MPW runs for discrete MEMS design in MEMSCAP technologies, which include Poly-MUMPs, SOI-MUMPs and piezo-MUMPs.

More recently, Teledyne Dalsa MEMS MIDIS and Micralyne MicraGEM-Si technologies have also been offered through CMC in Canada as part of the cooperation between the MPW centres worldwide. The Teledyne Dalsa technology can be used for accelerometers, gyroscopes, resonators, inertial sensors or combinations of those, while the Micralyne technology is suitable for display technology, optics and telecommunications, inertial sensing, biomedical and environmental sensing.

Besides the traditional MEMS technologies, EURO PRACTICE also offers optical photonics technologies (in particular Si-photonics). The MPW service in these technologies at CEA-Leti and IMEC was set-up in ePIXfab, but has been transferred to EURO PRACTICE since 2015. In addition, IHP offers an integrated SiGe-Photonics technology based on their SG25H4 high frequency technology. Since March 2015, EURO PRACTICE also offers photonics packaging together with Tyndall National Institute in Ireland. The photonics ecosystem continues to gather momentum attracting new users (both from academia and from industry) and increasing technical scope of the photonics offering via EURO PRACTICE. Research and development continues to be active amongst telecom, datacom and bio-sensing sectors.

All-in-all, this is a significant More-than-Moore portfolio, which complements the ASIC portfolio. The offered MPW services in these selected technologies are set up in the same way as described for the ASICs including technical support, distribution of foundry design kits, etc.



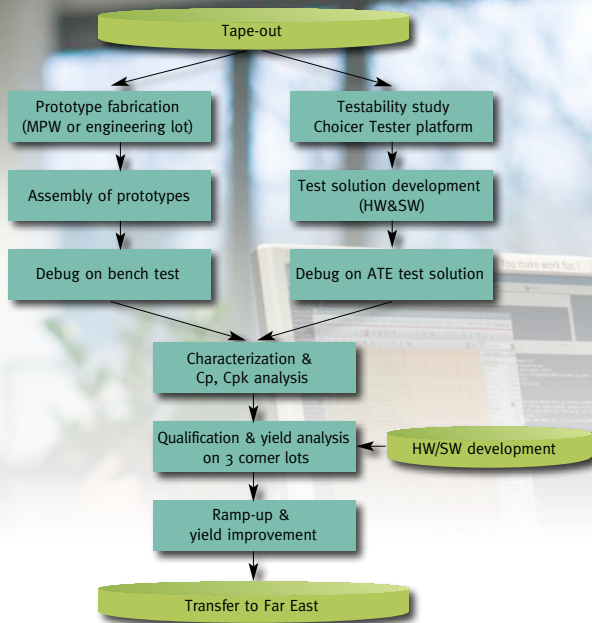
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BACKEND OPERATION SERVICES

Standardly, EURO PRACTICE delivers unpackaged untested prototypes. However, EURO PRACTICE does offer a low cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of packages are available ranging from DILs to PGAs and QFNs.

Side by side with world class partners and our long-term agreements, Europractice boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management. The most relevant companies involved in our semiconductor supply chain are listed below:

- **Foundry partners:** TSMC, UMC, ON Semi, ams, IHP, X-FAB, GLOBALFOUNDRIES, MEMSCAP, imec and CEA-LETI
- **Ceramic assembly partners:** HCM.Systrel, Optocap, Kyocera
- **Plastic assembly partners:** ASE, Kyocera
- **Wafer bumping partner:** Pactech, ASE
- **Test partners:** ASE, Microtest, Delta, Rood Technology and bluetest
- **Failure analysis:** Maser Engineering
- **Library partners:** Faraday, ARM



FROM PROTOTYPES TO VOLUME PRODUCTION

After successful ASIC prototyping, the Europractice partners (Fraunhofer IIS and imec) can also provide the customer access to the full production and qualification stage (from low to mid-high volumes).

PROTOTYPE FABRICATION

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. Europractice will produce the first prototypes for the customer and organize the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program.

The devices can be tested on both wafer level as well on packaged devices. The goal is to reduce the test time and to test the ASIC for manufacturing problems using the ATPG and functional patterns. The devices can be tested on both wafer level as well on packaged devices.

Europractice will support you during the development of single site test solution as well as with a multi-site test solution when high volume testing is required. Based on the test strategy followed diverse type of implementations can be realized.

DEBUG AND CHARACTERIZATION

Before going into production, a characterization test program will check if all the ASIC specifications are met according to the customer expectations. Threshold values are defined for each tested parameter. The software will test all different IP blocks and the results will be verified with the bench test results. A characterization at Low (LT), Room (RT) and High (HT) temperature will be performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be strong against process variations, the product qualification can start. Europractice can support you through the full qualification process using different kind of qualification flows ranging from Consumer, Industrial, Medical to Space according to the Military, Jedec and ESCC standards.... In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

SUPPLY CHAIN MANAGEMENT

Europractice is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.

Customer products are treated internally as projects and followed closely by the imec engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. Europractice therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

YIELD IMPROVEMENT

Europractice can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the qualification of the device on 3 different corner lots, Europractice can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers will be analyzed to check for yield issues related to assembly or wafer production. Europractice is using the well proven tool Examiner™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.



LOW COST IC PROTOTYPING

The cost of producing a new ASIC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. This is largely due to the NRE (Non-Recurring Engineering) overheads associated with design, manufacturing and test.

EUROPRACTICE has reduced the NRE, especially for ASIC prototyping, by two techniques:

1. Multi Project Wafer Runs or
2. Multi Level Masks.

MULTI PROJECT WAFER RUNS

By combining several designs from different customers onto one mask set and prototype run, known as Multi Project Wafer (MPW) runs, the high NRE costs of a mask set is shared among the participating customers.

Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full prototyping wafer run. A limited number of tested or untested ASIC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time".

In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

EUROPRACTICE is organising about 200 MPW runs per year in various technologies.

MULTI LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi Level Mask (MLM). With this technique the available mask area (20 mm x 20 mm field) is typically divided in four quadrants (4L/R : four layer per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is thus reduced by a factor of four. By adapting the lithographical procedure it is possible to use one mask four times for the different layers by using the appropriate quadrants. Using this technique the mask costs can be reduced by about 50%.

The advantages of using MLM single user runs are : (i) lower mask costs, (ii) can be started any date and not restricted to scheduled MPW runs, (iii) single user and (iv) customer receives minimal a few wafers, so several hundreds of prototypes.

This technique is preferred over MPW runs when the chip area becomes large and when the customer wants to get a higher number of prototypes or preserie. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.

This technique is only available for technologies from ON Semiconductor, IHP, TSMC and XFAB.

TECHNOLOGIES

For 2017, EUROPRACTICE has extended its technology portfolio. Currently, customers can have access to prototype and production fabrication in the following technologies :

- On Semi 0.7 μ C07M-D
- On Semi 0.7 μ C07M-A
- On Semi 0.35 μ C035U
- On Semi 0.7 μ C07M-I2T100 100V
- On Semi 0.35 μ C035-I3T80U 80V
- On Semi 0.35 μ C035-I3T50U 50V
- On Semi 0.35 μ C035-I3T50U (E) 50V
- On Semi 0.35 μ C035-I3T25U 3.3/25V
- ONC18MS 0.18 μ m
- ONC18MS-LL 0.18 μ m
- ONC18HPA 0.18 μ m
- ONC18-I4T 0.18 μ m 45/70V
- On Semi 0.5 μ CMOS EEPROM C5F
- On Semi 0.5 μ CMOS EEPROM C5N
- ams 0.35 μ CMOS C35B4C3
- ams 0.35 μ CMOS C35OPTO
- ams 0.35 μ HV CMOS H35B4D3
- ams 0.35 μ SiGe-BiCMOS S35
- ams 0.18 μ CMOS aC18
- ams 0.18 μ HV CMOS aH18
- BARC Diode for ams C35OPTO
- WLSCP for ams C35B4C3
- IHP SGB25V 0.25 μ SiGe:C
- IHP SG25H3 0.25 μ SiGe:C
- IHP SG25H4 0.25 μ SiGe:C
- IHP SG25H_EPIC
- IHP SG13S 0.13 μ SiGe:C
- IHP SG13C 0.13 μ SiGe:C
- IHP SG13G2 0.13 μ SiGe:C
- IHP SG25 PIC (photonics)
- IHP BEOL SG25
- IHP BEOL SG13
- X-FAB XH018 0.18 μ HV NVM E-Flash
- X-FAB XT018 0.18 μ HV SOI
- X-FAB XS018 0.18 μ OPTO
- TSMC 0.18 CMOS L/MS/RF (G)
- TSMC 0.18 CMOS HV BCD Gen2
- TSMC 0.13 CMOS L/MS/RF (G,LP)
- TSMC 90nm CMOS L/MS/RF (G,LP)
- TSMC 65nm CMOS L/MS/RF (G)
- TSMC 40nm CMOS L/MS/RF (G)
- TSMC 28nm CMOS HPL/HPC
- UMC L180 Logic GII
- UMC L180 MM/RF
- UMC L180 Logic LL
- UMC L180 EFLASH Logic GII
- UMC CIS18 – CONV diode
- UMC CIS18 – ULTRA diode
- UMC L130 Logic
- UMC L130 MM/RF
- UMC L110AE Logic/MM/RF
- UMC L65N L/MM/RF (SP)
- UMC L65N L/MM/RF (LL)
- UMC 55N EFLASH EEPROM LP
- UMC 40N Logic/MM – LP
- UMC 28N Logic/MM – HPC
- GF 55nm LPe/LPx-NVM/LPx-RF
- GF 40nm LP/LP-RF/RF-mmWave
- GF 28nm SLP/SLP-RF
- GF 22nm FDSOI
- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- MEMSCAP PIEZOMUMPS
- ePIXfab-imec SiPhotonics Passives
- ePIXfab-imec SiPhotonics ISIPP50G
- ePIXfab-LETI SiPhotonics Passives + Heater
- Teledyne Dalsa MIDIS

MINI@SIC PROTOTYPING CONDITIONS FOR UNIVERSITIES AND RESEARCH LABORATORIES

Prototyping costs have been increasing with scaled technologies due to high mask costs. Even on MPW runs with shared costs, the minimum prototyping fee (corresponding to a minimum chip area) is high for advanced technologies such as 90, 65, 40, 28 and 22nm.

In order to stimulate universities and research institutes to prototype small ASIC designs, Europractice has introduced in 2003 the concept of mini@sic.

That means that Europractice has selected several MPW runs on selected technologies on which universities and research institutes have the opportunity to prototype very small ASIC designs at a highly reduced minimum prototype fee. The minimum charged chip area is highly reduced.

Through the mini@sic concept, the price is reduced considerably. For the most advanced technologies however, the prototyping fee is further reduced through extra funding by the European Commission through the Europractice project (only for European universities and research institutes).



FIRST USER STIMULATION PROGRAM

At the end of 2015, a first stimulation action was launched to encourage EURO PRACTICE university members to have an ASIC prototyped for the first time or to move to more advanced technology nodes

Implementation was proposed as follows:

- To stimulate university members that have not yet prototyped an ASIC. Europractice selected 10 first user application, who were granted free (excluding assembly) prototyping of a minimum block on a *mini@sic* run in 0.18u CMOS (UMC, TSMC and ams).
- To stimulate university members that have not yet prototyped an ASIC in a technology of 90nm or below. Europractice selected 10 such first users prototyping of a min. area block of a *mini@sic* run in 65nm/55nm (TSMC, UMC and GLOBALFOUNDRIES) at a price of €5,000 (excluding assembly).

The First Users submitted their applications early January. For each category/competition 23 design proposal were received, from which the best proposals were selected. Three experts were approached to perform the selection (10 best proposals in each category) based on criteria defined by the EC, namely Application, Design methodology, Inventiveness, Presentation, Clarity of the case. As conclusion, 8 Very First Users and 7 First Advanced Users managed to tape-out their designs on a *mini@sic* run before 30 September 2016, which is a very nice result. Some examples of these selected designs are described further in this report.

After the success of this first stimulation action in Europractice, two new Stimulation Actions for FIRST USER European EURO PRACTICE university members were defined as a part of the EURO PRACTICE 2016 project funded by the European Commission. Once more the 10 best design in the two categories were selected by an Independent Committee. The designs are expected to be realized in silicon in the course of 2017.

TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

EURO PRACTICE training courses for European universities and Research Institutes are primarily aimed at academic staff and PhD students. Unlike training courses which address single topics or individual design tools, the EURO PRACTICE training courses address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow. Since the courses are based on the EURO PRACTICE EDA/ CAD tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organisation and make full use of the EURO PRACTICE services/infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants will be able to extensively practice the concepts described in lectures and have access to experts who are able to answer questions about the concepts, design tools or technology process discussed on the course. Where it is known that a design flow is well supported by multiple vendors and/or processes then multiple course variants will be offered that reflect the design tool / processes installed base. Offered training courses follow a “train-the-trainer” philosophy, so that participants can convey the knowledge acquired to colleagues within their own organisation. Training course participants will be provided with course notes (manuals) which they can then keep and refer to at a late date when applying the techniques to their own work.

EUROPRACTICE WEBSITES



The current Europractice service is holding 2 web pages in order to promote the service and to keep all (potential) users updated on new available tools and technologies.

- The EDA / CAD tool web site (www.europractice.stfc.ac.uk) is hosted and maintained by STFC. This page is updated at least twice per week by STFC and contains all the latest information about the design tools, training courses and events.

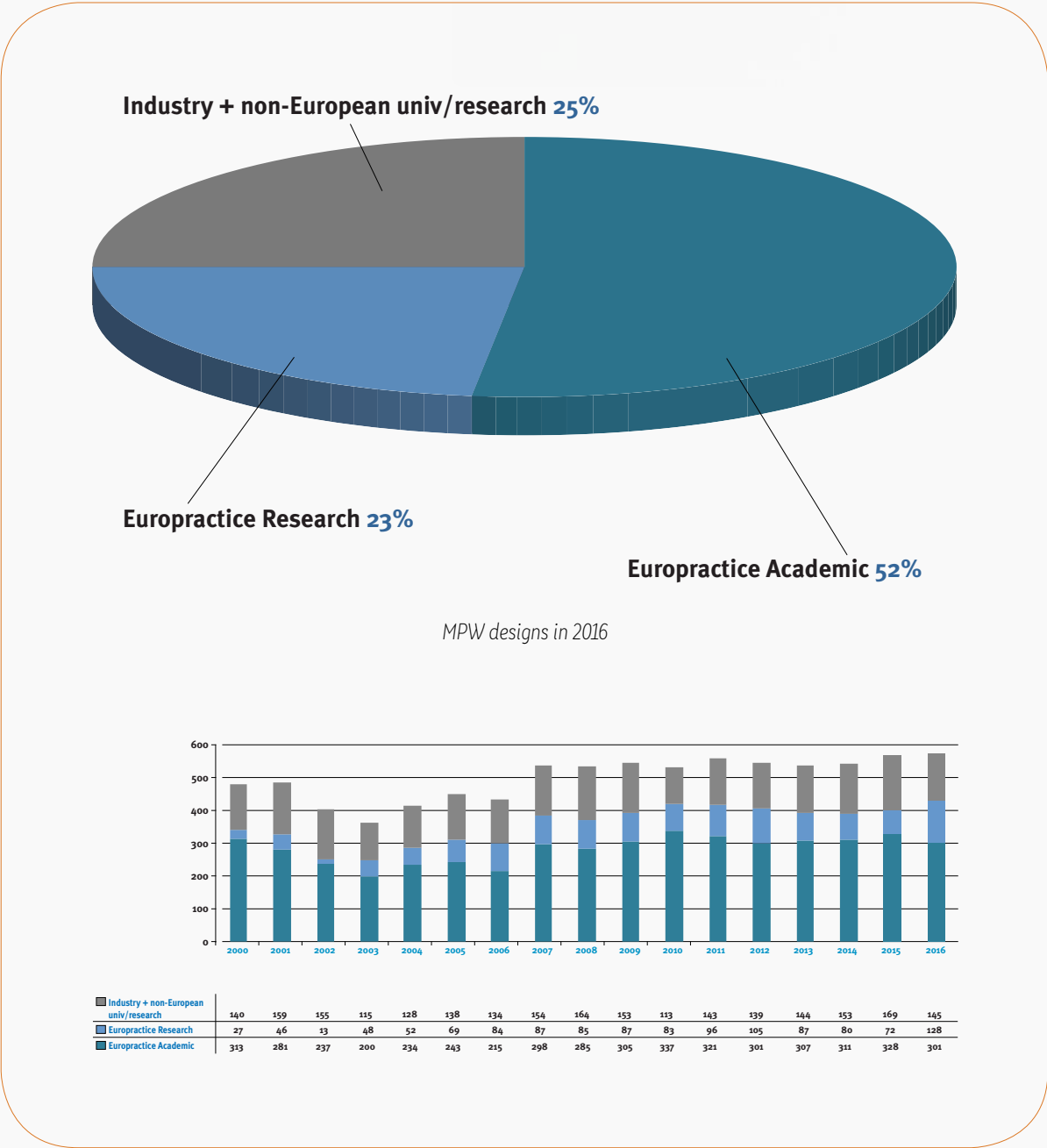


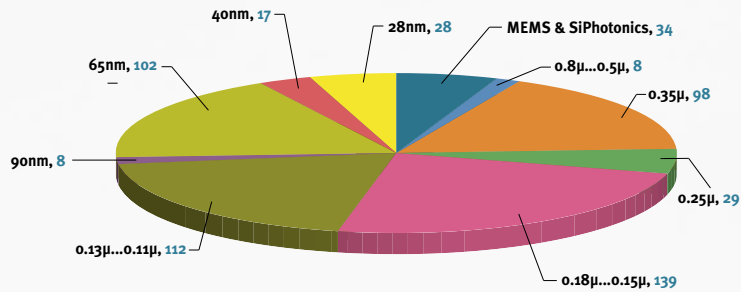
- The IC technology / fabrication web site (www.europractice-ic.com) is hosted and maintained by IMEC and is regularly updated with the latest news on MPW offering, schedule and pricings.



RESULTS

MPW PROTOTYPING SERVICE



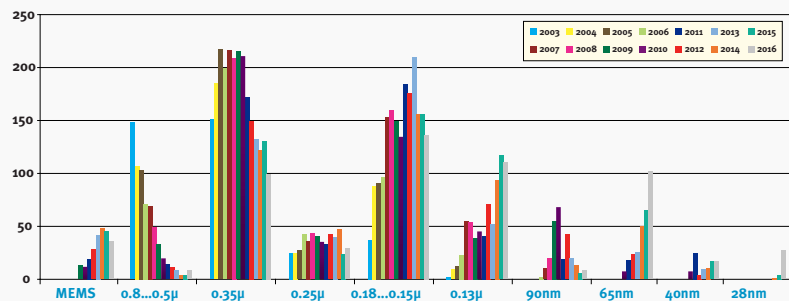


MPW designs in 2016: technology node and number of designs

ASICS PROTOTYPED ON MPW RUNS

In 2016, a total of 575 designs have been prototyped, a small increase compared to 2015.

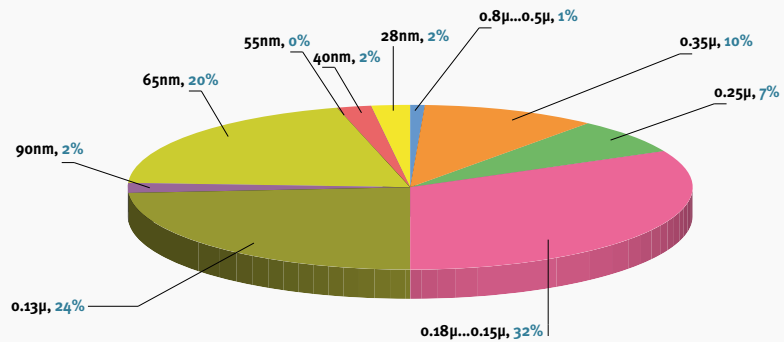
75% of the designs are sent in by European universities and research institutes while the remaining 25% of the designs is sent in by non-European universities and commercial companies world-wide.



Geometry mix

GEOMETRY MIX

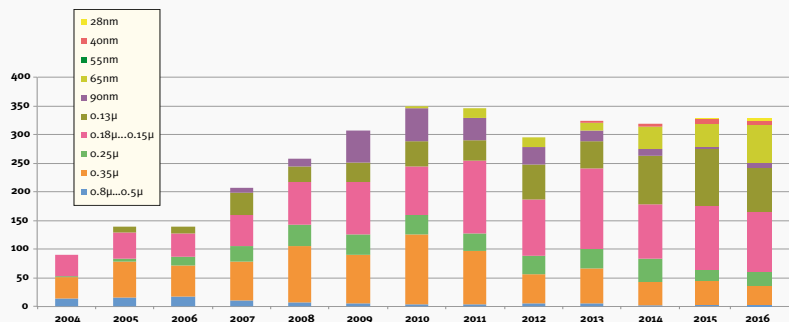
Year over year a shift towards more advanced technologies can be observed. Also in 2016 a similar trend occurred and is shown in the bar graphs. Especially the advanced technology use increased significantly to a record-high of 65nm and 28nm designs. However, the 0.18μ / 0.15μ and 0.13μ / 0.11μ technologies still represent almost half of the total designs. Finally, the number of designs in Silicon Photonics and MEMS (indicated as MEMS) has decreased a bit compared to 2015.

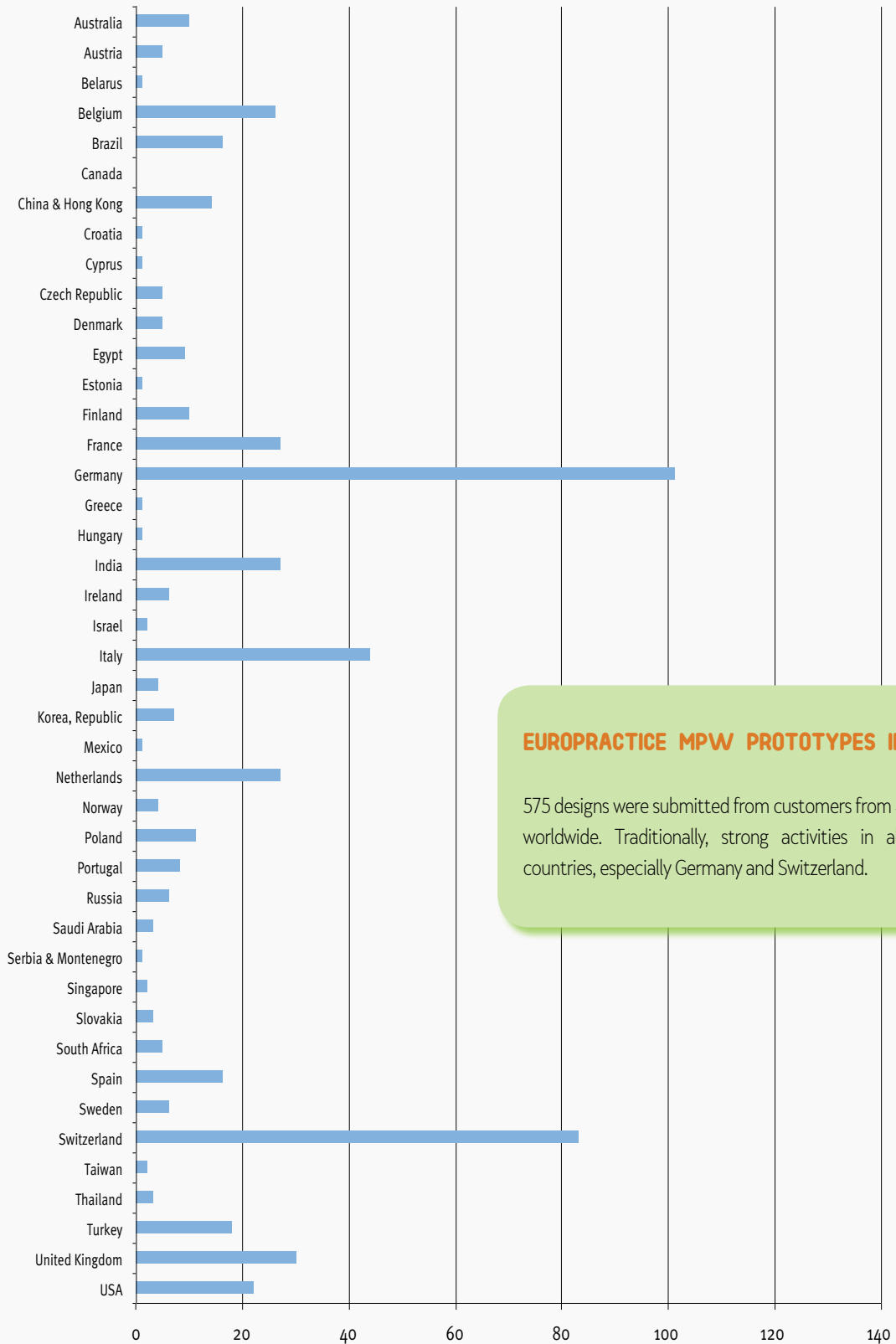


mini@sic designs per gatelength in 2016

MINI@SIC

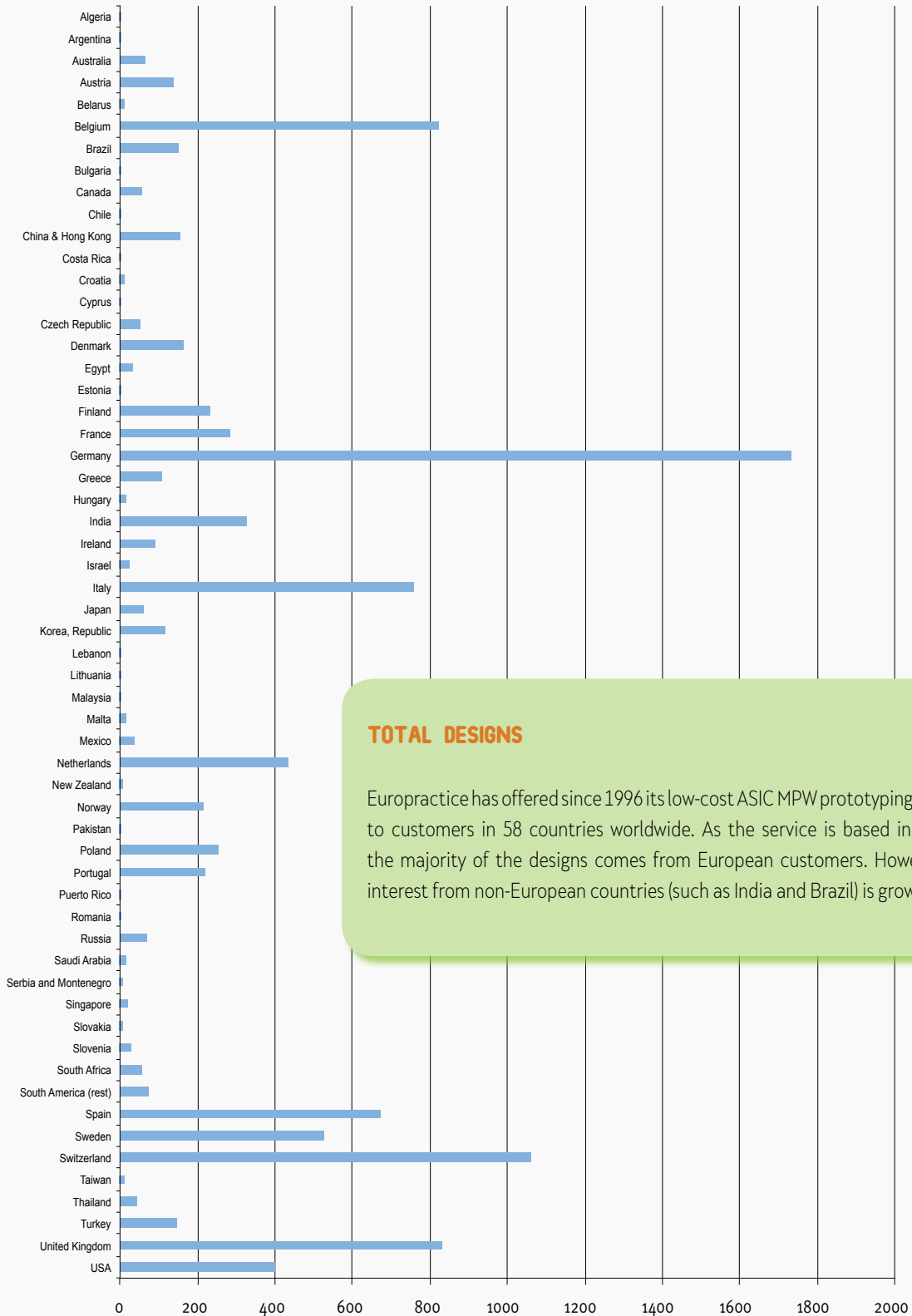
The mini@sic concept continues to be used extensively by universities in 2016. Especially, the older technology nodes (0.13μ and above) are very popular, thanks to the affordable pricings. Also, the mini@sic 28nm offering grew significantly compared to last year.





EUROPRACTICE MPW PROTOTYPES IN 2016

575 designs were submitted from customers from 43 countries worldwide. Traditionally, strong activities in all European countries, especially Germany and Switzerland.



TOTAL DESIGNS

Europractice has offered since 1996 its low-cost ASIC MPW prototyping services to customers in 58 countries worldwide. As the service is based in Europe, the majority of the designs comes from European customers. However, the interest from non-European countries (such as India and Brazil) is growing fast.

EXAMPLES OF PROJECTS FUNDED THROUGH STIMULATION ACTION

Custom Integrated Circuit Design for Portable Ultrasound Scanners

A36040 / Denmark Technical University, Department of Electrical Engineering - Kgs. Lyngby (Denmark)

Student: Pere Llimos Muntal (PhD study)

Supervisor: Ivan Harald Holger Jørgensen

Email: ihhj@elektro.dtu.dk

Technology: TSMC 65nm CMOS LP MS/RF

Die size: 2000 x 2000 μm

Description

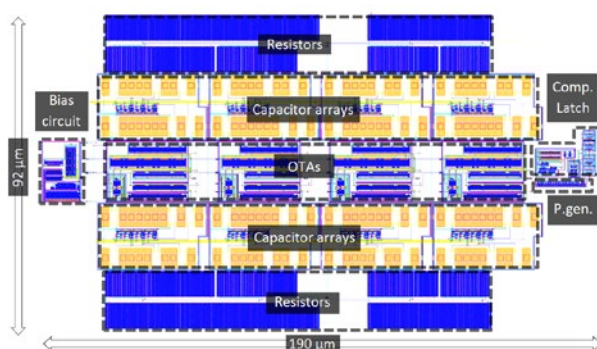
The integrated circuit fabricated using the stimulation program was done in a 65nm process and is part of the PhD project “Custom Integrated Circuit Design for Portable Ultrasound Scanners” at the Department of Electrical Engineering at the Technical University of Denmark (DTU). The die contains receiving circuitry for portable scanners including a low noise amplifier (LNA) and an analog-to-digital converter (ADC).

Results

The LNA has a gain of 15.3dB, a bandwidth of 13.2MHz and an input referred noise of $1.6\text{V}/\sqrt{\text{Hz}}$, consuming 1.6mW and occupying a die area of 0.0072mm^2 .

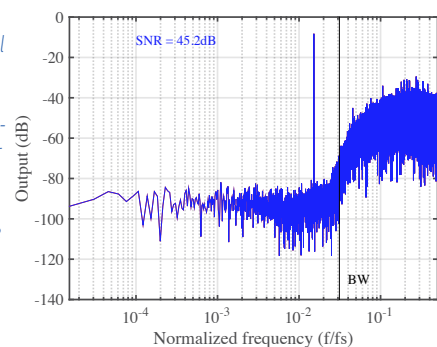
The ADC is implemented as a fully differential fourth-order 1-bit continuous-time delta-sigma analog-to-digital converter (CTDS ADC). The bandwidth (BW) of the CTDS ADC is 10MHz, and the sampling frequency (f_s) used is 320MHz leading to an oversampling ratio (OSR) of 16. The supply voltages are 0V and 1.2V, and the maximum stable amplitude (MSA) of the ADC is 0.6V.

The fourth order loop filter is implemented with operational amplifier based RC integrators and simple switch-based voltage digital-to-analog converters (DACs). The integrating capacitors are implemented with an adjustable capacitor array in order to compensate for corners and variations. The quantizer contains a pulse generator, a speed-enhanced clocked comparator and a pull-down clocked latch. The layout of the CTDS ADC is shown in Fig. 1, and it occupies approximately 0.0175mm^2 . The die picture under a microscope is shown in Fig. 2.



◀ Fig.1: Layout of the fully differential fourth-order 1-bit continuous-time delta-sigma analog-to-digital converter (CTDS ADC).

▶ Fig.2: Microscope picture viewing a part of the fabricated die containing the CTDS ADC.



The frequency response of the CTDS ADC using the MSA of 0.6V at an input frequency of 5MHz is shown in Fig. 3. The BW of 10MHz is marked with a vertical black line. The fourth order noise shaped response can be easily observed. The maximum signal-to-noise ratio (SNR) obtained is 45.2dB, and the power consumption is 0.587mW.

The CTDS ADC design has been published in^[1] and it has received an invitation for an extended version submission to the “Analog Integrated Circuits and Signal Processing” Springer Journal.

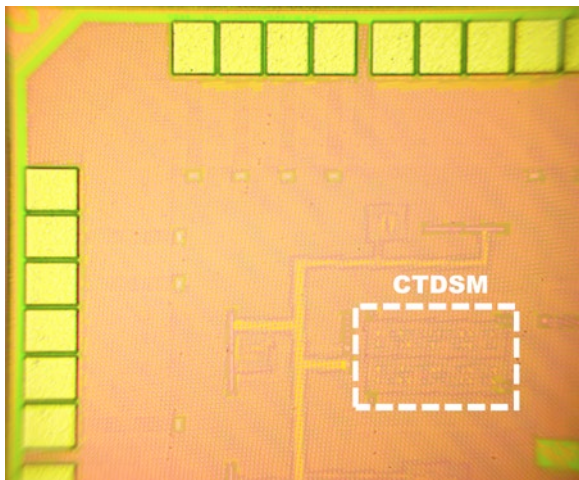


Fig.3: Frequency response of the CTDS ADC with an input amplitude of 0.6V.

Experience with Europractice First User Stimulation action

During the three years of this PhD project, we have been using EURO PRACTICE as part of the integrating circuit fabrication, bonding and packaging process. Furthermore, three different processes have been used, both in standard and high-voltage processes. EURO PRACTICE has been always provided an effective and fast service. As the first user of the stimulation program we have to note that it has been an extremely positive experience, and we believe that it really helps universities to get access to more advanced processes and facilitate the integrated circuit fabrication.

Reference

^[1]P. Llimós Muntal, I. H. H. Jørgensen, and E. Bruun, “A 10 MHz Bandwidth Continuous-Time Delta-Sigma Modulator for Portable Ultrasound Scanners,” in 2016 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), 2016.

Spread-Spectrum Clock Generator (SSCG) Supporting Highly Discontinuous Frequency Modulations

A12370 / University of Napoli Federico II – Italy

Designers: D. De Caro, N. Petra, E. Napoli, A.G.M. Strollo

Email: dadecaro@unina.it

Technology: UMC L65N Logic/MM/RF

Die size: 1875 x 1875 μm

Motivation

The continuous growing in modern system on chips (SoCs) speed and complexity results also in increased difficulties in mitigating the electromagnetic interference (EMI) produced by the IC. An established approach to reduce EMI in digital circuits is using a spread-spectrum approach, in which the frequency of the clock signal is slightly and slowly varied in a predefined frequency range in order to spread the energy of each clock harmonic over a given bandwidth in order to reduce power peak emissions (modulation gain).

In a digital system-on-chip there can be also the need of subsystems where clock spreading is not allowed (e.g. digital to analog and analog to digital converters, critical peripherals, ...). Inevitably a synchronization problem arises when subsystems clocked with a frequency modulated clock need to communicate with subsystems where frequency spreading is not allowed. A simple pair of registers can be used to solve this problem (by avoiding complex FIFO systems) by imposing a synchronization timing constraint between modulated and unmodulated clock signals^[1]. Unfortunately a very low modulation gain, not higher than 8dB can be achieved with currently known modulation waveforms (e.g. triangular, sawtooth, optimized frequency continuous^[2], optimized frequency discontinuous^[3]).

Project objective

This project is aimed to design in an advanced CMOS technology a novel all-digital spread-spectrum clock generator supporting novel, highly discontinuous, modulation waveforms, able to achieve modulation gains higher than 8dB under the above-mentioned synchronization timing constraint.

To that purpose, we have developed novel highly discontinuous modulation waveforms. The following figure compares the modulation gain achievable by novel highly discontinuous waveforms, with previous modulations (as a function of mod-

ulation frequency f_m). It can be observed that increasing the number of discontinuity points per modulation period (Ndis) from 18 to 44 increases the modulation gain. A modulation gain as high as 19.3dB is achieved with Ndis=44, compared to the highest modulation gain of only 7.7dB achieved by the best of previous modulations.

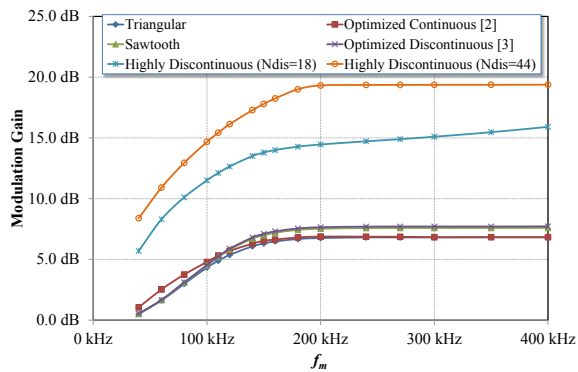


Fig.1: Comparison of modulation gain achievable by novel highly discontinuous waveforms.

Description of the design

Developed Spread-Spectrum Clock Generator (SSCG) uses an all-digital approach that is the best suited to generate output waveforms with as high as 44 discontinuity points per modulation period. The circuit includes two synchronized output clock: one with frequency spreading capability and one at a fixed frequency. This will allow the experimental verification of the synchronization between the two signals.

The top-level schematic of the circuit is shown in the following figure:

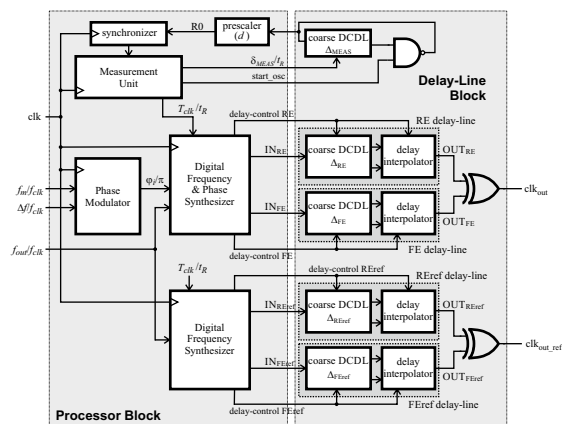


Fig.2: Block diagram of the designed circuit

The modulated output clock signal clk_{out} is obtained by using a Phase Modulator, which evaluates instantaneous phase deviation due to modulation (ϕ_i/π) and a Frequency & Phase Synthesizer, which receives as input also the desired center output frequency f_{out}/f_{clk} . A couple of delay-lines and a XOR gate produces the signal clk_{out} . The reference output clock signal $clk_{out,ref}$ requires only a Frequency Synthesizer, a couple of delay-lines and a XOR gate. Note that maintaining the synchronization between the two output clocks necessary requires the employ of a Phase Modulator and a Frequency & Phase Synthesizers for the modulated clock generation. In fact, the phase is the integral of the frequency and the employ of a simple (and well-known) Frequency Synthesizer for the modulated clock generation would inevitably lead to a de-synchronization between the two signals clk_{out} and $clk_{out,ref}$ over time. The two blocks Phase Modulator and a Frequency & Phase Synthesizers have been developed in this project for the first time and represents an additional scientific contribution of this work.

A third scientific contribution of this project is the development of novel digitally-controlled delay line (DCDL) topology. DCDL circuits are the most critical blocks of the SSCG, since output clock edges timing is finely controlled by these circuits. In our previous experience ([4],[5]) we have seen that these components are responsible for the largest component of the power dissipation of the SSCG and their non-linearity effects translates in output clock jitter. In this context we have developed a novel DCDL topology which about halves the number of transistors with respect to previous solution. In addition we have developed a novel two-stage delay interpolator which reduces non-linear load effects and improves the INL. The following table reports a comparison (post schematic simulations) between previous state-of-the-art solution (using a NAND-based coarse DCDL [6] and a single Flip-flop driving circuit [7]) and novel DCDL:

	Power (μW/MHz)	t_{min} (ps)	t_r (ps)	Max INL (ps)
Interpolated NAND-based DCDL [6] with Single Flip-Flop driving Circuit [7]	4.09	166	0.60	1.40
Novel NAND-based DCDL	1.83	188	0.60	1.45

It is interesting to observe that both solutions achieve a resolution t_r as low as 0.6 ps. In the novel solution, however, the power dissipation is reduced by more than two times with

respect to previous one. The INL is comparable between the two circuits. Please note, however, that novel DCDL requires a 64 steps interpolator (compared to the 32 steps interpolator of previous DCDL) and that in this circuit a INL as low as 1.45 ps is only possible thanks to the developed two stage delay interpolation strategy.

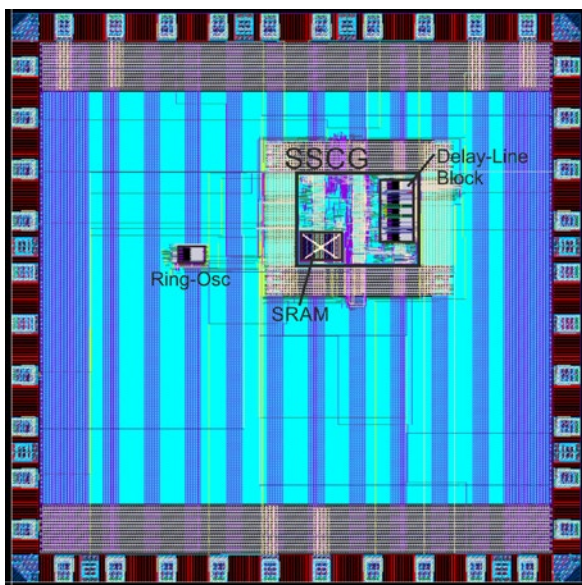


Fig.3: Final test chip layout in UMC 65nm CMOS technology

The SSCG includes also a SRAM, which allows to implement arbitrary and frequency discontinuous modulations. An on-chip Ring Oscillator is included in the test chip to easy the measurement of the SSCG maximum clock frequency.

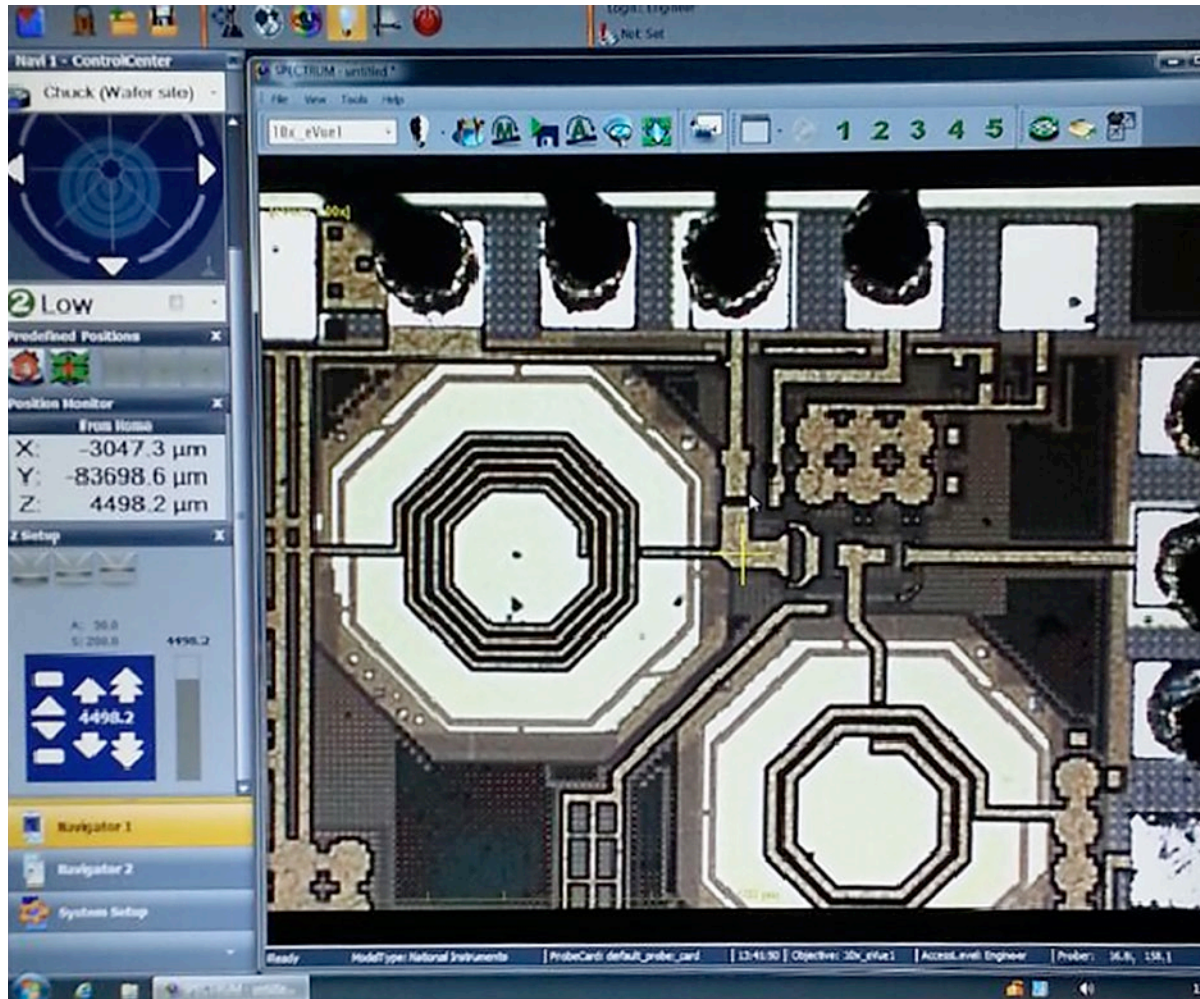
Added value of this project

The development of this project has been extremely challenging and, similarly to our previous works^{[4][5]}, has required a work at many different levels, from the most theoretical aspects of the frequency spreading law and parameters, through the RTL description of the Frequency & Phase Synthesizer and Phase Modulator, to the transistor level full-custom layout and simulation of the DCDL and the Delay-Line Block. In our Electronic Engineering Master of Science Degree, in our University, our students are already trained to cadence full-custom (Virtuoso) and standard-cells flows (RTL Compiler, SoC Encounter), thanks to Europractice classroom teaching licenses. This allowed us to dedicate two graduating students that, with the help of our PhD Students (G. Castellano and D. Esposito) have completely designed the novel SSCG and integrated the final chip layout.

Note that in this project the required output frequencies (higher than 1GHz), the timing critical behavior, the mismatch effects and reduced output jitter requirements (e.g. below 5psrms) involve the employ of an advanced technology (65nm) to really validate novel solutions and compare with existing the state-of-the-art. This has also represented the possibility for our graduating students and PhD students to face for the first time with a challenging mixed-signal design scenario in an advanced CMOS technology. We thank Europractice First User Stimulation Programme for the funding support to this activity.

References

- [1] D. De Caro, M. De Martino, N. Petra, A.G.M. Strollo, "Analysis of spread-spectrum clocking modulations under synchronization timing constraint", *Lecture Notes in Electrical Engineering*, vol.351, pp.153-159, 2016.
- [2] Y. Matsumoto, K. Fujii, A. Sugiura, "An Analytical Method for Determining the Optimal Modulating Waveform for Dithered Clock Generation," *IEEE Trans. on Electromagnetic Compatibility*, vol.47, no.3, pp.577-584, Aug.2005.
- [3] D. De Caro, "Optimal Discontinuous Frequency Modulation for Spread-Spectrum Clocking", *IEEE Trans. on Electromagnetic Compatibility*, vol.55, no.5, pp.891-900, Oct. 2013.
- [4] D. De Caro, C.A. Romani, N. Petra, A.G.M. Strollo, C. Parrella, "A 1.27GHz, All-Digital Spread Spectrum Clock Generator/Synthesizer in 65nm CMOS", *IEEE Journal of Solid-State Circuits*, vol.45, no.5, pp.1048-1060, doi: 10.1109/JSSC.2010.2043461, May 2010.
- [5] D. De Caro, F. Tessitore, G. Vai, N. Imperato, N. Petra, E. Napoli, C. Parrella, A.G.M. Strollo, "A 3.3GHz Spread-Spectrum Clock Generator Supporting Discontinuous Frequency Modulations in 28nm CMOS", *IEEE Journal of Solid-State Circuits*, vol.50, no.9, pp.2074-2089, doi: 10.1109/JSSC.2015.2423977, Sept. 2015.
- [6] D. De Caro, "Glitch-free NAND-based Digitally Controlled Delay-Lines", *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol.21, no.1, pp.55-66, doi: 10.1109/TVLSI.2011.2181547, Jan. 2013.
- [7] D. De Caro, F. Tessitore, G. Vai, G. Castellano, E. Napoli, N. Petra, C. Parrella, A.G.M. Strollo, "Single Flip-flop Driving Circuit for glitch-free NAND-based Digitally Controlled Delay-Lines", *Circuits, Systems & Signal Processing*, doi: 10.1007/s00034-016-0369-5.



The granted application of Technion – Israel Institute of Technology, Dept. of Electrical Engineering contained two small designs fitted in one mini@sic block. Below the realized silicon is shown together with a detailed description of the ICs.

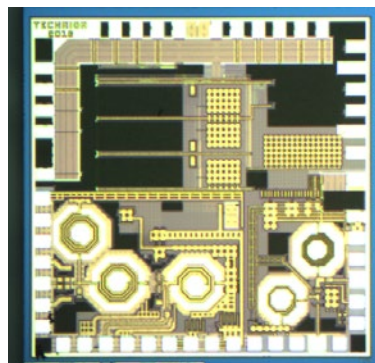


Fig1: Microscope picture of the fabricated designs

Design 1: Switched Capacitors readout circuits for CMOS Sensors

Technion - Israel Institute of Technology - Haifa (Israel)

Designers: Alex Zviagintsev, PhD student

Email: alehan99@gmail.com

Supervisors: Prof. Yael Nemirovsky, Dr. Ilan Bloom

Technology: TSMC 0.18 μm mixed signal process

Die size: 1600 x 800 μm

Description

ISFET (Ion-sensitive Field Effect Transistors) was invented over 50 years ago. The sensor is similar to a MOS transistor but instead of a regular gate, the analyzed solution or liquid is the gate. ISFETs have been fabricated in semimanual processes, which influence its cost, reliability and uniformity. In addition, the measurement of the output signal requires complex readout circuitry, which results in additional cost, noise and calibration complexity. The need for individual calibration of each ISFET has been the most significant barrier to commercialization as a commodity.

Thus, while regular MOS transistors are the most successful electronic devices in terms of business and consumer products, ISFETs are still an R&D field. Technion ISMOS (2011 patent application) is addressing the mentioned problems and allows implementation of low-cost, simple sensor with minimal calibration requirements. In particular, ISMOS is implemented in standard CMOS technology. By using strictly CMOS technology and adding few steps as post-processing, a significant reduction in cost is anticipated while the performance and reproducibility is enhanced. Hence, the term ISMOS, Ion Sensitive MOS. The circuit which has been designed includes several operation amplifiers, sensors, ESD circuits. The latter is particular important because of the interaction with the solution. The design includes less than 700 transistors.

Results

This is part of a system on chip research, where the sensors are fabricated in CMOS technology. Accordingly, ISFETs are dubbed ISMOS. The current demo (part of a PhD thesis) includes sensors fabricated by CMOS-SOI-NEMS technology, Readout circuits (TSMC), Printed Circuit Board (PCB), and Software support for final results processing. We are still waiting for the final manufacturing of the PCB board in order to characterize the TSMC die.

Design 2: High linear transceiver for operation in 5GHz band for IoT applications

Technion - Israel Institute of Technology - Haifa (Israel)

Designers: Avi Sayag, Nimrod Ginzberg, Yanir Schwartz, PhD and MSC students

Email: avi_sayag@hotmail.com, nimrod@tx.technion.ac.il, yanirs@tx.technion.ac.il

Supervisors: Prof. Emanuel Cohen

Technology: TSMC 0.18 μm mixed signal process

Die size: 1600 x 800 μm

Description

In the modern receiver, the antenna is connected to the LNA, which requires designing a high frequency linear device with good NF (Noise Figure) and low power consumption. By skipping the LNA, and connecting the antenna directly to the mixer, we can save chip space, high demanding design in the RF path and to transfer the design issues into the LO (local oscillator) path. The added complexity of the LO design is preferred due to the saturated design, which is favorite in simplicity and power consumption.

By using novel circuit techniques, a design at high frequency close the F_t/F_{max} parameter of the transistor can be achieved with better performance compared to existing solutions and much smaller size. The low noise design and higher interferer immunity receiver while preserving low power consumption will enable also wide bandwidth and multiple receiver integration in the same die for the future standards of wireless communication.

Results

We are currently designing a designated PCB for our chip to prove our design concepts.

Experience with Europractice First User Stimulation action

As a first project with Europractice and TSMC, we would like to express our appreciation to anyone involved. We appreciate the well-organized PDK and documentation. Also, thanks to the supporters for their quick response and availability to our questions which arose during the design flow. Looking forward to more successful projects in the future.

Acknowledgements

In addition please allow me to reiterate the words of thanks we sent to the TSMC design support team. "We at the Technion would like to thank you all very much and express our sincere appreciation for all the support you gave us this last month which enabled us to meet the deadline for this tape-out. We are looking forward to working with you again in the future."

EXAMPLES OF SPECIAL PROJECTS

Dedicated Engineering Run for Neural Microsystems, Lab-on-Chip, and Wearable Sensory Systems

Centre for Bio-Inspired Technology, Imperial College London
(in collaboration with Newcastle University), UK

Contact: Timothy Constandinou, Yan Liu, Song Luan

Email: t.constandinou@imperial.ac.uk, yan.liu06@imperial.ac.uk, s.luan@imperial.ac.uk

Designers: Timothy Constandinou, Matt Douthwaite, Peilong Feng, Pantelis Georgiou, Sara Ghoreishizadeh, Dorian Haci, Ermis Koutsos, Nishanth Kulasekeram, Yan Liu, Song Luan, Dora Ma, Michal Maslik, Federico Mazza, Khalid Mirza, Nikolaos Miscourides, Nicolas Moser, Adrien Rapeaux, Katarzyna Szostak, Chris Toumazou, Ian Williams (in collaboration with Ahmed Abd-El-Aal, Patrick Degenaar, Fahimeh Dehkhoda, Reza Ramezani at Newcastle University)

Technology: ams 0.35µm 2P4M HV CMOS (H35B4S1)

Die size: 16mm x 16mm

Run: Dedicated engineering run, started July 2016

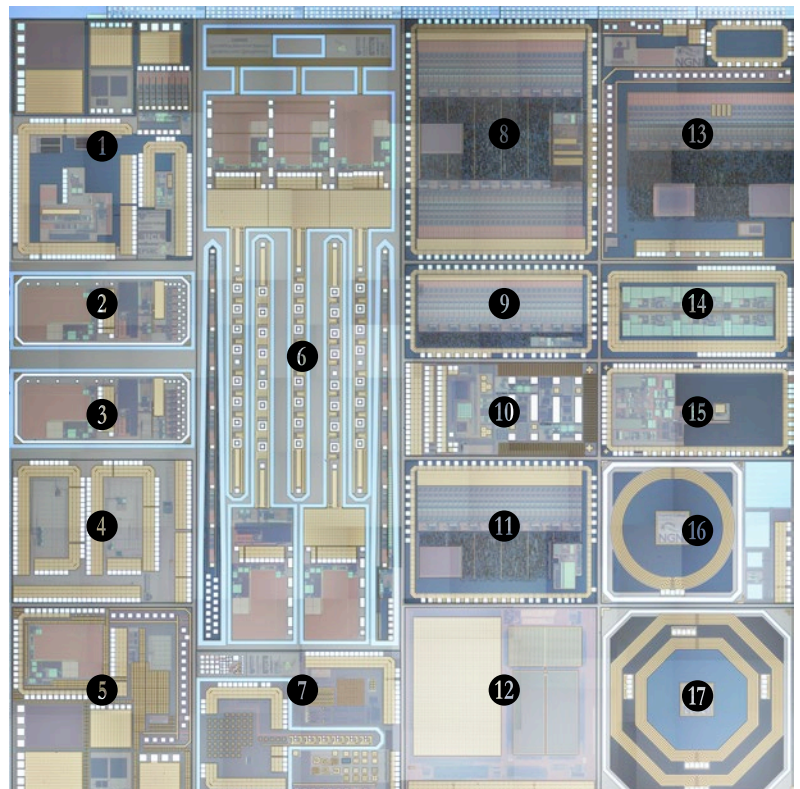


Fig.1: 16mm x 16mm reticle floorplan including 17 designs fabricated via a dedicated engineering run in ams H35B4S1 technology.

Fig.2: Manufactured 200mm engineering wafer with 95-repetitions of each design (diced reticle shown on right).

Description

The microelectronics design effort at the Centre for Bio-Inspired Technology (Imperial College London) has been particularly productive this past year. With a number of our key projects requiring integrated circuit prototyping, we have coordinated (with the support of Europractice/Fraunhofer IIS) an internal multi-project wafer through a dedicated engineering (single die tooling) run in AMS 0.35µm HV CMOS technology. This design has involved the effort of over 20 researchers, resulting in 15 unique SoCs (system on chips) and 6 test chip designs, all for biomedical applications. These have been organized as 17 dies occupying a 16mm x 16mm reticle. Details of the chip designs are provided in Table 1.

ID	Die Size	Purpose
1	3.7mm x 4.9mm	CANDO test chip for
2	3.8mm x 1.6mm	CANDO head-only SoC
3	3.8mm x 1.6mm	CANDO h
4	3.7mm x 2.9mm	CANDO test chip for optoelectronic stimulation,
5	3.7mm x 3.9mm	CANDO test chip for 4-wire intrabody comm
6	4.2mm x 12.8mm	CANDO implantable optrodes for controlling abnormal network dynamics
7	4.2mm x 3.0mm	CANDO test chip including probe design for
8	3.9mm x 4.9mm	iPROBE 64-channel
9	3.9mm x 1.9mm	iPROBE 32-channel
10	3.9mm x 1.9mm	Current-based circuits for pH-
11	3.9mm x 2.9mm	iPROBE
12	3.9mm x 3.9mm	Chemical sensing array
13	3.9mm x 4.9mm	SenseBack 32-channel bidire
14	3.9mm x 1.9mm	I2MOVE multichannel PNS interface for treatment of obesity
15	3.9mm x 1.9mm	Wearable EMG monitor for muscle fatigue detection
16	3.9mm x 2.9mm	ENGINI
17	3.9mm x 3.9mm	ENGINI chip

Table 1. Individual die design details/purposes

For further project details see:

CANDO – www.cando.ac.uk

SenseBack – www.senseback.com

iPROBE – www.imperial.ac.uk/neural-interfaces/research/projects/iprobe/

ENGINI – www.imperial.ac.uk/neural-interfaces/research/projects/engini/

I2MOVE – www.imperial.ac.uk/a-z-research/i2move/

chemical sensors – www.imperial.ac.uk/bio-inspired-technology/research/metabolic/isfets/

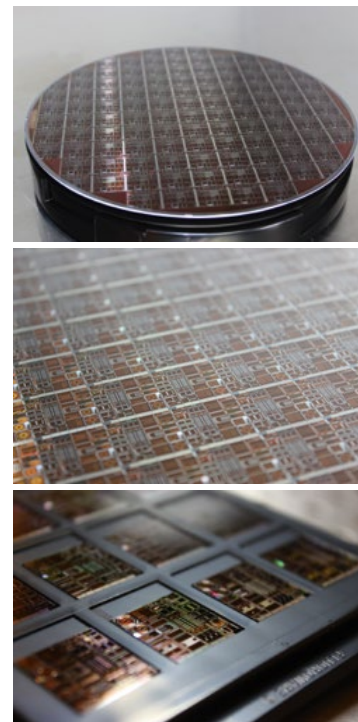


Fig. 2

Why Europractice?

Europractice provides us an invaluable resource, at present, and for over the past 2 decades. We have relied on Europractice for licensing, support, and training of our high-end EDA (electronic design automation) CAD tools, in addition to providing an affordable integrated circuit fabrication service. This also includes access to technology documentation, design kits, coordinating multi-project wafers (MPWs), tape-out, and post-fabrication support. We have enjoyed the benefit from working with the Europractice teams at: STFC (UK), IMEC (Belgium), and particularly over this past year Fraunhofer IIS (Germany).

Acknowledgement

This work is funded by UK EPSRC (Engineering and Physical Sciences Research Council) grant references: EP/M020975/1, EP/M025977/1, NS/A000026/1, EP/K015060/1 and the Wellcome Trust.

Microchips from the Open Hardware PULP project

ETH Zurich, Integrated Systems Laboratory (IIS), Switzerland

Contact: Luca Benini,

Frank K. Gurkaynak

Email: lbenini@iis.ee.ethz.ch,
kgf@iis.ee.ethz.ch

Technologies: UMC65LL 1P8M,
GF28SLP 1P8M

Description of the project

At ETH Zürich in collaboration with the University of Bologna, we have been working on parallel, ultra-low power processing systems (PULP) using an open source approach. Our goal is to make all source code that we develop in this project freely available for others to use and build on. As a first step, we have already released PULPino (<http://pulp-platform.org>) a silicon-proven single-core microcontroller that implements the open RISC-V architecture (<http://riscv.org>) by Berkeley using a permissive Solderpad license (<http://solderpad.org/licenses>) derived from the Apache v2.0 license explicitly to support open source hardware. Our release includes all source code, verification scripts, examples and support tools that are necessary to develop applications on this system. In the near future, we will also release our multi-core PULP systems (once the code is mature enough for a wide release) as well as updates to the single core PULPino systems.

Releasing our work using open source licenses was a strategic decision with many important benefits for us. The open nature of our project allows us great freedom in our collaborations with both industry and academia. Collaborations with

external partners can start immediately as we do not burdened by negotiations and limitations on our platform. Furthermore, our partners are not confined to our design decisions; the open source releases give them the freedom to change and adapt our designs as they see fit. In the long run, we also hope to benefit from contributions from other groups that use our platform. Open hardware platforms are great for benchmarking as everyone will have access to identical environment, improving the quality of results. Finally, usable open source hardware has the potential to lower the entry costs for integrated circuit design for some SMEs and allow them to be more competitive, hopefully creating more business and employment opportunities.

An important aspect of our work is that we have already manufactured and tested multiple chips in a variety of technologies. The next PULP system we are working on is already the 20th chip that will be related to the PULP project, and the code that we publish benefits from this experience. Users tend to have more confidence in designs they know have already been manufactured and tested.

Results

All in all, we have manufactured and tested four chips from the PULP project within 2016 through Europractice.

	Imperio	Phoebe	Fulmine	Honey Bunny
Technology	UMC65LL	UMC65LL	UMC65LL	GF28SLP
Area	1.56 mm ²	1.56 mm ²	6.90 mm ²	3.00 mm ²
Package	QFN40	QFN40	QFN64	QFN56
# Cores	1	4	4	4
ISA	RISC-V	OpenRISC	OpenRISC	RISC-V
Memory	52 kB	64 kB	256 kB	324 kB
Max. Clock	500 MHz	300 MHz	420 MHz	660 MHz
Specialty		Shared LNU Shared Vector LNU	CNN Accelerator Crypto Accelerator	

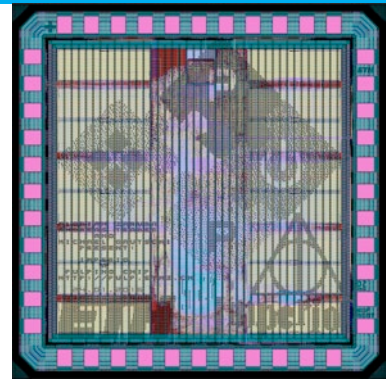


Fig. 1

1) IMPERIO (UMC65LL 1P8M)

Imperio is the first PULPino implementation to be taped out. PULPino is derived from the larger PULP family of systems, but it is a single core microcontroller and combines this with the peripherals we have developed for the PULP platform. Imperio uses our custom RISC-V core that supports the RV32IMC specification and includes several custom instructions to improve the performance for digital signal processing applications^[2]. The source code of this chip is currently freely accessible over the <http://pulp-platform.org> website. It was verified to run up to 500 MHz, achieves 3.19 Coremark per MHz and consumes 15 microWatts per MHz when running at 0.9V supply voltage.

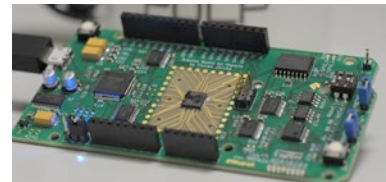


Fig. 2

Table 1: Comparison table of the four chips manufactured in the PULP project



Fig. 3

2) PHOEBE (UMC65LL 1P8M)

In a multi-core system such as PULP that features small and efficient processor cores, adding larger computation blocks such as floating point units can be quite costly. One solution is to share such blocks among several cores. We have then investigated alternative methods for calculating floating numbers and have developed a computation unit that is able to calculate with floating point numbers expressed in so called logarithmic format where the number is stored as a fixed-point, power of two. Our experiments have shown that we can achieve the same numerical accuracy as IEEE single precision floating point format within reasonable hardware overhead. Unlike a traditional floating point number unit (FPU), a logarithmic number unit (LNU) is more amenable to sharing as several complex operations (such as floating point multiplication and division in logarithmic format) can directly be calculated within the integer ALU of the cores. Phoebe is a small test chip that contains a complete PULP system that shares 1 LNU among 4 OpenRISC cores. It actually contains two LNUs, one full size version that operates on 32-bit numbers with 4 cycle latency and a vectorial LNU that contains two 16-bit LNUs with 2 cycle latency. The LNU also contains support for trigonometric extensions in the LNU (sin, cos, atan), fused multiply/divide add/sub operations (fma, fda, fms, fds) as well as the following vector LNU operations (add, sub, mul, div, sqrt, casts, trig, fma, dotp). All LNUs in total have a complexity of about 72 kGE. The results of this work were recently published ^[1] at the ARITH-2016 conference.

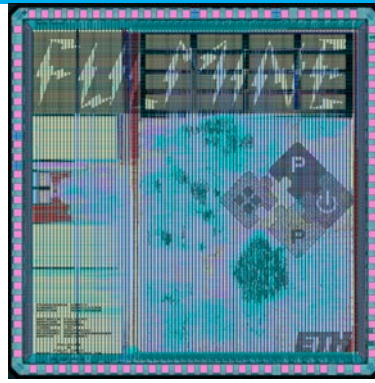


Fig. 4

3) FULMINE (UMC65LL 1P8M)

Fulmine (Italian for lightning) is a four core PULP system using the third generation of our customized OpenRISC cores. The cores feature many improvements targeted towards digital signal processing including new instructions for vector processing and fixed point arithmetic using Q15 and Q31 format. These instructions include dot product and accumulate between vectors, multiply, accumulate and shift instructions, clip, shuffle and various bit manipulation instructions. The chip also features an I/O DMA that allows the system to directly copy data from peripherals to memory without CPU intervention. The real strength of this system lies in the two dedicated accelerators that have direct access to the level-1 data memory used by the four cores. The first accelerator is a hardware convolution engine optimized for convolutional neural networks and allows vectorized convolutions with reduced precision weights achieving a near linear speedup when the calculations involved can tolerate the reduced accuracy. The second accelerator is specialized for cryptographic functions, and is able to perform a wide variety of functions, including en/de-cryption using ECB and XTS modes, authenticated encryption and hash generation using the Keccak algorithm ^[3]. Overall the system can run at 84MHz consuming only 27 mW while running a complex secure CNN application involving both accelerators. The system has been tested extensively and we are currently supplying academic partners with development boards with Fulmine.

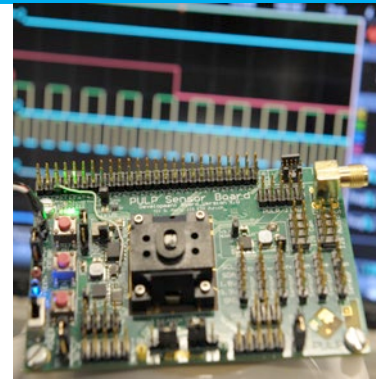


Fig. 5

4) HONEY BUNNY (GF28SLP 1P8M)

During the initial phases of the PULP project, we relied on OpenRISC cores for our systems. We have started to support RISC-V cores in our recent systems, and Honey Bunny (named after a character from the Quentin Tarantino movie Pulp Fiction) is the first four core PULP system to be based on our own RISC-V cores called RI5CY. This chip was designed to be used as a development platform for embedded IoT applications. It has an internal FLL allowing it to run from an external 32 kHz crystal oscillator up to 660 MHz. Honey Bunny has in total 324 kBytes of on-chip SRAM allowing it to be used for a wide number of applications.

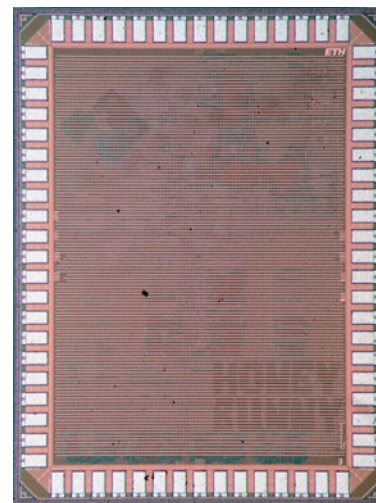


Fig. 6

Fig.1: Full layout view of Imperio testchip

Fig.2: PCB board, compatible with Arduino shields

Fig.3: Full layout view of Phoebe testchip

Fig.4: Full layout view of Fulmine testchip

Fig.5: Functional board with Fulmine chip

Fig.6: Microscope view of fabricated Honey Bunny chip.

Why Europractice?

As ETH Zurich, we have enjoyed a long and fruitful relationship with Europractice IC service resulting in over 150 chips in the last 10 years. As part of our research it is important to have easy access to state of the art technologies, and this year we were able to use the Globalfoundries 28nm process in addition to UMC65nm and for the coming year we are already planning to make use of Globalfoundries 22nm FDSOI and UMC55nm eFlash technologies.

We firmly believe in the open source movement, and we are trying to disclose as much design data as we can within the limits of the non-disclosure agreements we have signed. At the moment, data from the foundries and basic IP such as memory compilers, standard cell and I/O libraries are not yet openly accessible. This is where we believe Europractice IC service plays a key role by allowing universities and startup companies in Europe easy access to the same technology data and standard cell libraries that we use for most of our PULP series of chips. This way, other groups can replicate our results more directly and have more confidence knowing that they are using the same libraries as we have used during the design of our own chips.

References

- ^[1] Michael Schaffner, Michael Gautschi, Frank K. Gurkaynak, Luca Benini, “Accuracy and Performance Trade-offs of Logarithmic Number Units in Multi-Core Clusters”, 23rd IEEE Symposium on Computer Arithmetic (ARITH 2016), Santa Clara USA, DOI: 10.1109/ARITH.2016.10
- ^[2] Florian Zaruba, “Updates on PULPino”, In Proc. 5th RISC-V Workshop, November 29-30, 2016, Mountain View California
- ^[3] Frank Gurkaynak, Robert Schilling, Michael Muehlberghuber, Francesco Conti, Stefan Mangard, Luca Benini, Pasquale Davide Schiavone, Davide Rossi, Antonio Pullini, Michael Gautschi, Igor Loi and Germain Haugou, “Multi-Core Data Analytics SoC with a Flexible 1.76 Gbit/s AES-XTS Cryptographic Accelerator in 65nm CMOS”, In Proc. Third Workshop on Cryptography and Security in Computing Systems (CS2-2017), Stockholm, 24th of January 2017.

Acknowledgements

VeloPix ASIC: R. Ballabriga, X. Llopart, W. Wong, J. Schipper, S. Miryala, J. Buytaert, M. Campbell, M. van Beuzekom, K. Wyllie

Testing, measurements and readout system development: Marco Daldoss, Jerome Aloyz, Bas van der Heijden, Henk Boterenbrood, Edgar Lemos Cid, Pablo Vasquez

IP-block contributions: Stefano Michelis, Pedro Miguel Vicente Leitao and Rui De Oliveira Francisco.

VeloPix engineering run

PH Electronics group – ESE / Microelectronics section (ME), CERN, Switzerland in collaboration with Nikhef-CERN Business Incubation Center (BIC), Amsterdam, the Netherlands

Contact: Tuomas Poikela, Kostas Kloukinas

Email: tuomas.poikela@cern.ch

Technology: TSMC 130nm

Die size: 14 x 14 mm (65 kpixels)

Run: Dedicated engineering run

Introduction

VeloPix, a 130 nm CMOS technology chip with data driven and zero suppressed readout, will be used as a readout chip for the hybrid pixel system of the LHCb Vertex Locator (VELO) upgrade. Figure 1 depicts the final application for VeloPix. The chips (shown in red in the figure) are placed very close to the beamline. The upgrade, scheduled for LHC Run-3, will enable the experiment to be read out at 40 MHz in trigger-less mode, with event selection being performed in the CPU farm. The highest occupancy VeloPix ASICs will experience hit rates of more than 900 Mhits/s (equivalent to more than 15 Gbits/s of data), and the closest pixels are 5.1 mm from the LHC beams. This article is a brief introduction to the VeloPix ASIC.

Description

VeloPix is a full scale hybrid pixel readout chip measuring more than 14mm x 14mm and containing 65k pixels. The manufactured chip is shown in Figure 2 showing the top redistribution layer metal.

It was jointly developed by CERN in Switzerland and Nikhef in the Netherlands. It is a mixed-signal ASIC with digital logic occupying most (> 70%) of the chip area. In VeloPix, an analog front-end amplifies a current signal from a silicon sensor and digital front-end adds a time stamp to the pulse. Each pixel represents one bit of information. To implement the digital logic in the restricted area of a pixel region a custom made high-density digital standard cell library was developed. The digital library was properly characterized in order to use automated digital implementation tools.

The block diagram of the chip is shown in Figure 3. The pixels are grouped into regions of 2x4 pixels to share the timestamping and readout logic between 8 pixels. This reduces the amount of area taken by the logic. This common logic is connected to logic of the next pixel region, and these connections for the double column data bus, which transports the data to the End-of-

Column blocks. The ASIC includes four custom made high speed serialisers operating at 5.12 Gbps for data transmission. The ASIC also uses special radiation-hardened techniques such as triplication of the digital logic to mitigate the effect of SEUs (Single Event Upsets), and enclosed layout transistors in the analog front-ends to minimize the impact of TID (Total Ionizing Dose). To reduce the power consumption of the high density digital circuitry due to the TMR, high-Vt standard cell library and clock gating techniques were employed.

Results

The design was prototyped in a dedicated full-mask set on an 8-metal stack 130nm TSMC Cybershuttle run. The manufactured chips were received at CERN in August 2016. The testing of the ASIC has been a coordinated effort between CERN, Nikhef and the University of Santiago de Compostela, Spain. Analog front-end performance of the chip is adhering very well to the simulation results. Preliminary radiation tests for TID also confirm the performance is within specifications after the irradiation.

Power consumption of the chip is below the maximum required limit of 1.5 W/cm².

Testing of 5.12 Gbps high-speed, DLL-based serialisers has been a very challenging task. On-chip power supply noise and bond wire inductance issues had a big impact on the overall BER of the high-speed transmission links.

The required volume production for building the LHCb VELO detector is just 624 chips.

Why Europractice?

Europractice gives foundry access services to modern semiconductor processes of the worlds largest dedicated independent foundry, TSMC. Projects, such as VeloPix, with small volume production requirements would not have otherwise the possibility to access and benefit from the use of these advanced processes. The technical support that the project received from Europractice engineers was of very high standards facilitating the work of the designers. All technical questions were timely addressed and when necessary their resolution was escalated to TSMC engineers. Custom designed microelectronics components designed in advanced technologies are vital parts of today's complex scientific instruments. The services provided by Europractice are allowing a large community of physicists and engineers at CERN and in tens of collaborating Institutes working for these projects to use these technologies for the construction of such instruments with a centralized high quality support.

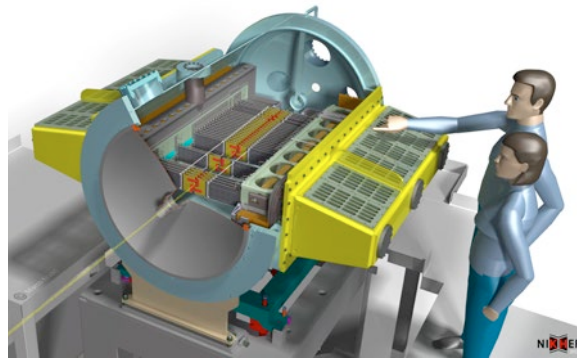


Fig. 1: Artist's impression of the upgraded VELO. (Image by Nikhef)

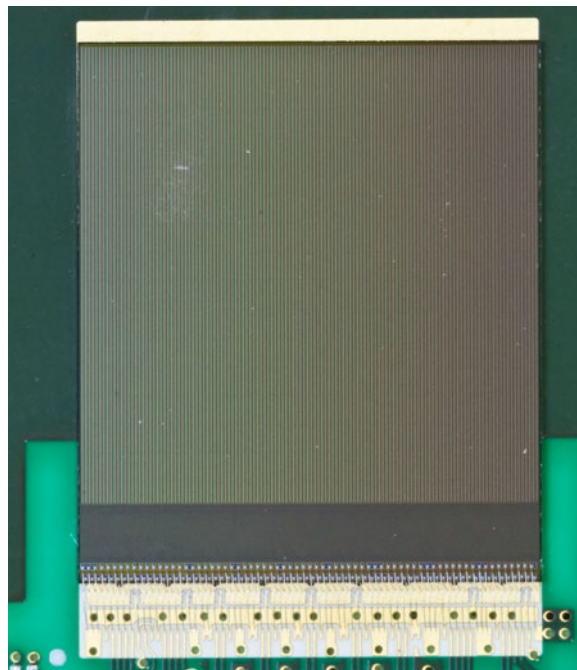


Fig. 2: VeloPix bonded to the chip board. (Image by Jérôme Aloyz, CERN)

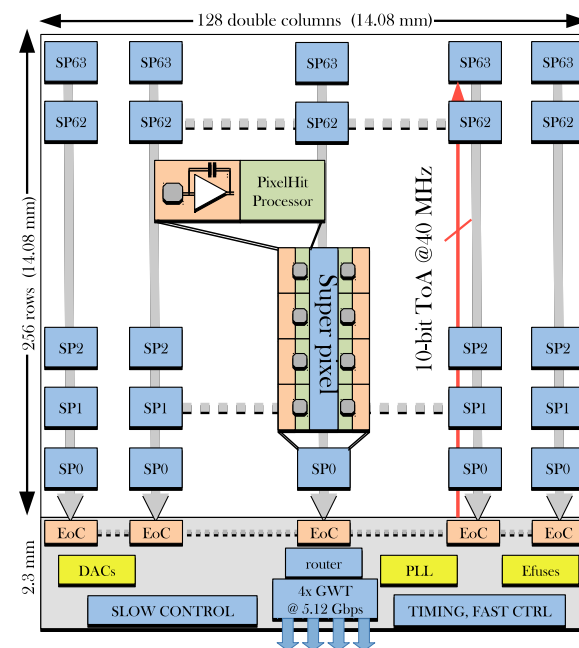


Fig. 3: VeloPix block diagram

EXAMPLES OF ASIC PROJECTS

A Single-chip 2048×1080 Resolution 32fps 380mW Trinocular Disparity Estimation Processor

Microelectronic Systems Laboratory (LSM), Ecole Polytechnique
Fédérale de Lausanne (EPFL), Lausanne, Switzerland

Contact: Jonathan Narinx, Tugba Demirci, Abdulkadir Akin, Prof. Yusuf Leblebici

Email: jonathan.narinx@epfl.ch

Technology: TSMC 28nm CMOS LOGIC HPM ELK Cu 1P8M 0.9/1.8V

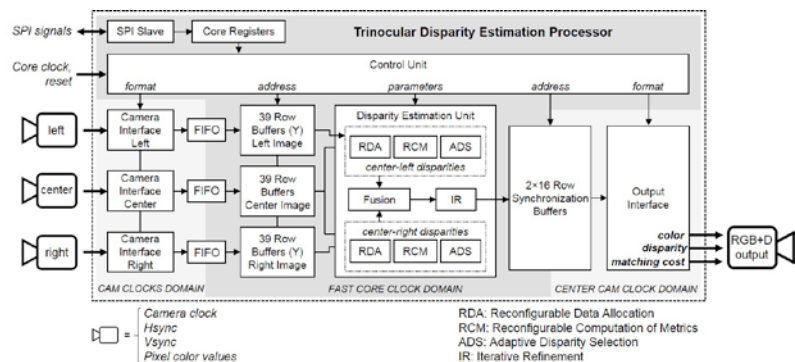
Die size: 2.07mm × 2.88mm

Description and Results

With the increasing prominence of real-time streaming video platforms, the demand for high-quality and real-time depth imaging devices has considerably increased in a wide variety of video processing applications where the 3D information has become essential, such as in autonomous vehicles, robotics, Virtual Reality (VR), etc. Depth estimation can be performed by exploiting different techniques, e.g. structured light projection, Time-of-Flight (ToF) or Disparity Estimation (DE) using stereo cameras. Unlike other techniques, DE is based only on passive image sensors, which enable High-Resolution (HR) depth maps at low-power, even in outdoor conditions (direct sunlight), and without any interference with other systems. Furthermore, the depth map quality of binocular configuration can be enhanced by using additional cameras, which prevent most of the erroneous depth estimations. However, achieving high-quality DE in real-time on HR video and at low power is challenging due to the high-computational complexity of this process and its need of large off-chip and on-chip memory size and bandwidth.

The developed single-chip trinocular disparity estimation processor is capable of computing in real-time up to 2K pixels resolution depth maps at 32fps with up to 256-pixel disparity range using two/three CMOS camera sensors. The most important feature of the design is that the ASIC is based on a trinocular adaptive window matching process that requires very limited on-chip memory, and completely avoids the usage of any external memory. Moreover, it features a stream-in/out interface to be easily integrated in existing vision systems requiring 3D data, without additional overhead, and offers a dynamically scalable tradeoff between throughput, resolution and disparity range.

Fig.1: Block diagram of the Trinocular DE Processor.



A block diagram of the DE processor is shown in Fig. 1. The chip is designed to receive the pixel-streams and their synchronization signals directly from three conventional RGB image sensors, and to stream-out the synchronized RGB values of pixels together with their computed disparity values (D) and synchronization signals of the center camera. The processor has a core operating frequency of up to 300MHz and outputs the color and depth data at the same frequency as the input camera clocks. Internally, two disparity maps are computed from the center-left and center-right camera pairs and then merged together to obtain the final trinocular disparity map of the center image. An SPI interface is provided to configure all the key parameters of the chip, such as the video resolution (up to 2K), disparity range (up to 256) and two- or three-camera configuration. In this way, the system behaves exactly as a RGB-D camera sensor.

The trinocular DE processor is fabricated in TSMC 28nm CMOS technology. The chip micrograph highlighted with the different memory blocks, and the bonded chip-on-board are shown in Fig. 2. The die area is 5.96mm² with 244 staggered pads. The core contains 3.2M CMOS logic gates and 582.5kB of internal SRAM blocks located around it. The system has been verified in real-time operation with three camera sensors at different resolutions, e.g. 90fps at XGA, 34fps at Full-HD and 32fps at 2K at 128 disparity range at 300MHz while consuming 380mW. Fig. 3 shows an example of a raw trinocular depth map computed on one real-world scene. The power consumption can be decreased by slowing down the core clock frequency, at the price of a lower throughput. The input-to-output latency at Full HD and 256 disparity range is measured to be 2.59ms (at 300MHz). As such, this single-chip solution provides the highest reported resolution and disparity range capability at the lowest power consumption and highest frame rate, while computing high-quality disparity results.

Why Europractice?

EPFL has been a very active academic member of the Europractice program since its beginning, and has always ranked among the top institutions in terms of the number of annual design submissions to the MPW service. Europractice IC services provide access to some of the most advanced technology nodes (such as the 28nm CMOS technology) for MPW fabrication, as well as expert advice and comprehensive guidance for using state-of-the-art design kits, libraries, and design software.

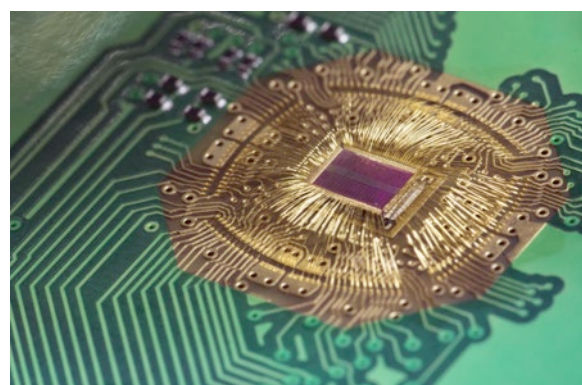
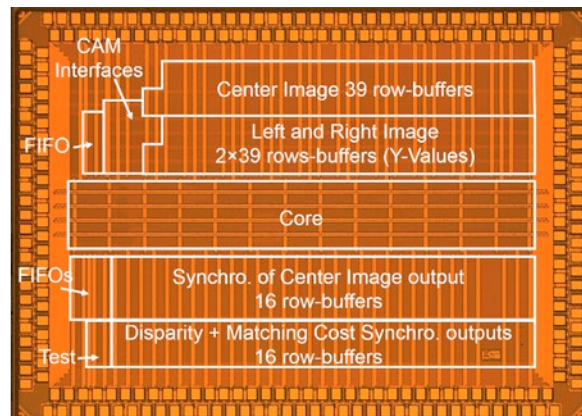


Fig. 2: Die micrograph of the chip and bonded COB, with a total of 244 pads in staggered configuration.

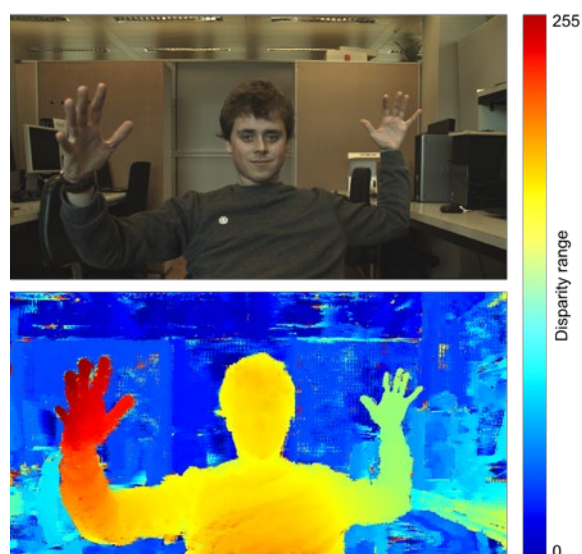


Fig. 3: Trinocular depth map raw output example.

Processing-error-tolerant fully-parallel turbo decoder

Electronics and Computer Science,
University of Southampton, UK

Contact: Dr Robert G Mauder

Email: rm@ecs.soton.ac.uk

Technology: TSMC 40nm LP 1P8M5X2Z

Die size: 1920x1920 μ m

Description

Turbo decoder circuits are used in many wireless communication systems to correct the transmission errors that are caused by noise, interference and poor signal strength. Turbo decoders are popular, since they facilitate reliable communication at high transmission power efficiency and high transmission throughput, which closely approach the theoretical limits. However, the overall power efficiency and overall throughput may be limited by the power efficiency and throughput of the turbo decoder circuit itself, unless this is carefully designed. The processing power efficiency and processing throughput of the turbo decoder circuit can be significantly improved by using voltage and clock scaling techniques, although this increases the likelihood of processing errors. However, turbo decoders have an inherent error correction ability. In this project, we exploit this inherent error correction ability to correct not only transmission errors caused by noise, interference and poor signal strength, but also processing errors caused by voltage and clock scaling. In this way, we can jointly optimize the overall power efficiency and overall throughput.

This tape out includes two turbo decoder circuits, as well as some isolated sub-components for testing purposes. One of the turbo decoder circuits employs several novel techniques for reducing the likelihood and impact of processing errors. The turbo decoder circuits employ a fully-parallel decoding algorithm and architecture, which have been jointly designed to allow the turbo decoding process to be completed within tens of clock cycles, rather than hundreds or thousands of clock cycles, as in conventional architectures. Owing to this, the fully-parallel turbo decoder offers 10 times better processing throughput and latency than the previous world record (<http://eprints.soton.ac.uk/386016>). This project has proven the fully-parallel turbo decoder and has led to its commercialization by AccelerComm Ltd (<http://www.accelercomm.com>)

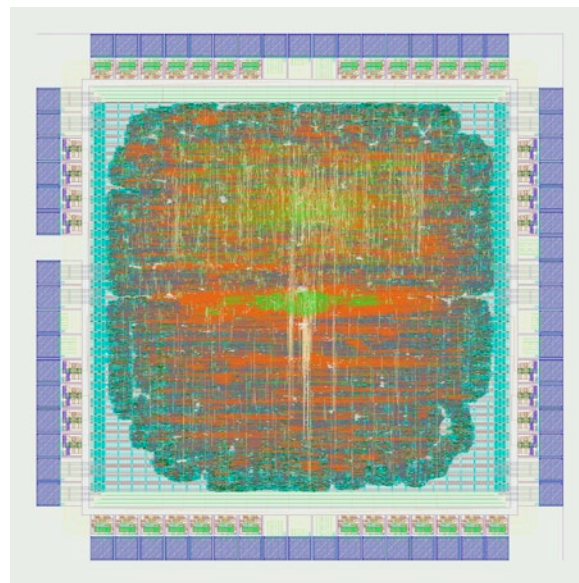


Fig.1: Layout view of the TURBO_2016_CHIP

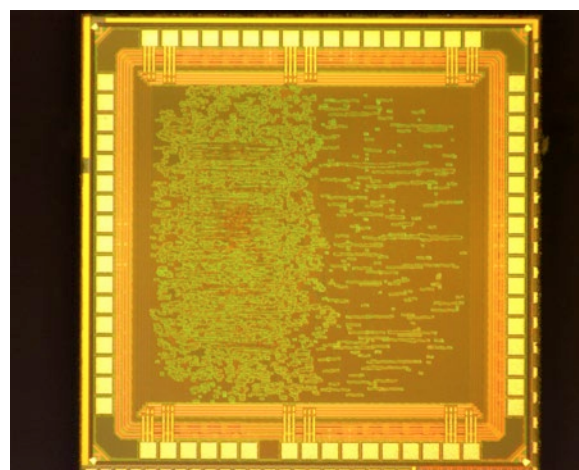


Fig.2: Microscope view of the fabricated chip

Why Europractice?

The University of Southampton has worked with Europractice on TSMC fabrication for many years. We have benefitted from Europractice's excellent technical support for dummy fill, chip submission and chip packaging. Europractice has given us affordable access to frequent multi-project wafer fabrication runs.

Acknowledgement

The financial support of the EPSRC, Swindon, UK under the grants EP/J015520/1 and EP/L010550/1 is gratefully acknowledged.

An Intrinsically Linear Wideband Digital Polar PA Featuring AM-AM and AM-PM Corrections Through Nonlinear Sizing, Overdrive-Voltage Control, and Multiphase RF Clocking

Delft University of Technology, ELCA Group, The Netherlands
Ampleon, Nijmegen, The Netherlands

Contact: Mohsen Hashemi, Leo de Vreede

Email: m.hashemi@tudelft.nl, L.C.N.deVreede@tudelft.nl

Technology: TSMC 40nm CMOS LP technology

Die size: 2795 μ m x 1184 μ m

Description

To fully benefit from the progress in CMOS technology, it is desirable to completely digitize the TX, replacing its final stage with a digitally-controlled PA (DPA). The DPA consists of arrays of small sub-PAs that are digitally controlled to modulate the output amplitude, thus operating as an RF-DAC. DPAs are normally designed in switched-mode (Classes E/D/D⁻¹, etc.) to achieve high efficiency while using high sampling rate to attenuate and push the spectral images to higher frequencies. However, they suffer from high nonlinearity in their AM-code-word (ACW) to AM and ACW to PM conversion. To correct for such nonlinearities, digital pre-distortion (DPD) of the input signal is often used, typically implemented by look-up tables (LUT). Unfortunately, DPD approaches suffer from large signal BW expansion due to their inherently nonlinear characteristics. This combined with the already present BW regrowth in a polar TX on the AM and PM paths yields significant hardware speed/power constraints when the signal BW becomes large. For a Cartesian TX, the use of LUT-DPD is even more compli-

cated since a full 2-D LUT is typically required. To relax the overall system complexity, it is highly desirable to have a PA with maximum inherent linearity without compromising the power or efficiency. In this work, ACW-AM correction based on nonlinear sizing along with controlling the peak voltage of RF clocks (overdrive voltage tuning) and ACW-PM correction based on multi-phase RF clocking are introduced to linearize the characteristic curves of a Class-E Polar DPA with intent to avoid any kind of predistortion. This work has been presented and published at ISSCC 2017.

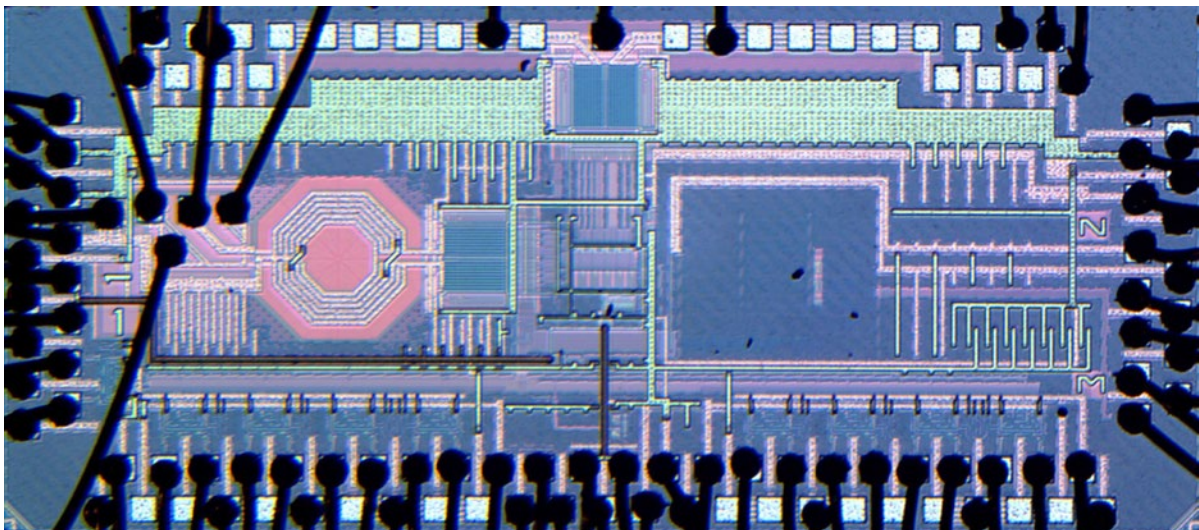
Why Europractice?

The Europractice MPW service allows affordable access to state-of-the-art technology such as the 40nm CMOS technology used in this work.

Acknowledgement

The authors acknowledge Atef Akhrouk from TU Delft and the imec/Europractice IC service team for their unlimited and high quality support, the people of Ampleon and NXP for their encouragement and advices, the projects SEEDCOM (STW) and EAST (RVO/Catrene) for the financial support.

Fig.1: Micrograph of the fabricated chip



CMOS Driver Array for a Segmented Mach-Zehnder Modulator

Ghent University – imec, IDlab,
Department of Information Technology, Belgium

Contact: Michael Vanhovecke, Xin Yin, Johan Bauwelinck

Email: michael.vanhovecke@ugent.be

Technology: TSMC 40nm CMOS LP technology

Die size: 3300 μ m x 1650 μ m

Description

Coherent technology has emerged as the backbone of optical networks in the past decade. As the demand for data traffic keeps on rising, higher-order modulation provides the path to further exploitation of the inherent capacity of optical fiber links, requiring components capable of introducing flexibility in the modulation format and spectral utilization.

In recent years, segmented transmitter architectures implementing an electro-optical digital-to-analog conversion (DAC) functionality have shown to be a promising candidate for the efficient generation of high-speed multi-level optical signals. A segmented electrode Mach-Zehnder Modulator (MZM) is paired with a dedicated driver IC to generate multi-level optical signals from multiple binary electrical drive signals.

The electronics in this work are designed to drive an InP MZM at 20 GBaud. The array of output driving stages utilizes voltage mode CMOS inverters to maximize the swing and to minimize the power consumption. The (pseudo-)differential output swing of 2.2V combined with a 3.3mm interaction length allows to fully drive the modulator. A tunable bidirectional timing architecture is implemented to apply the output signals sequentially to the modulator and as such match the optical velocity. For this purpose an on-chip transmission line is designed to propagate a full-rate clock signal that is used to re-time the incoming data signals. Additionally, several types of tunable delay structures ensure a proper timing of the outputs. An encoder circuit is included to match the input binary word to the segment configuration of the modulator. As a result, a 5 bit electro-optical DAC is realized with a total power consumption of 1W.

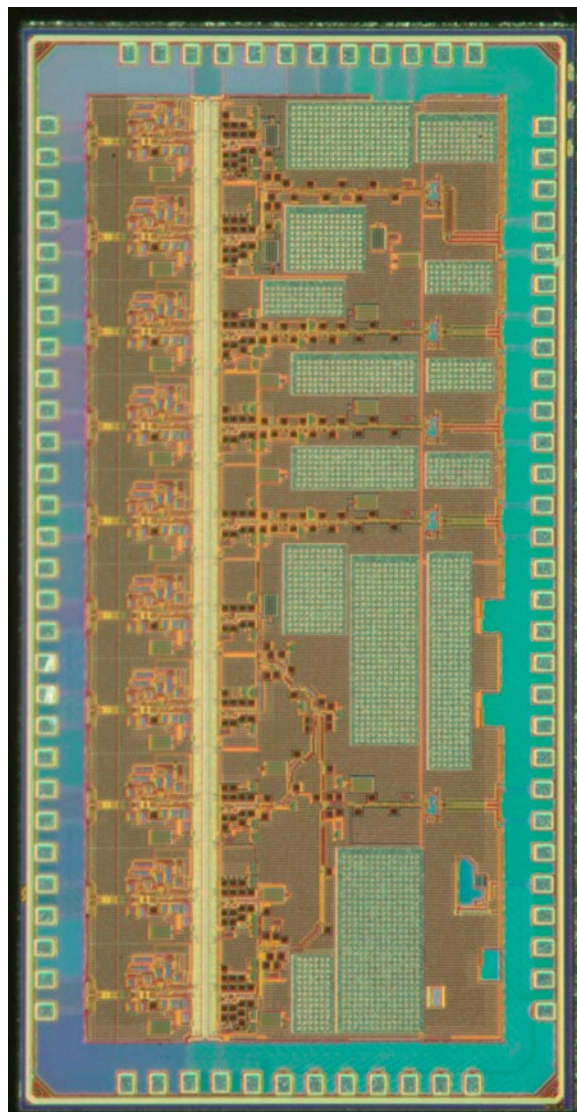


Fig.1: Microscope view of the fabricated chip

Why Europractice?

The Europractice MPW service allows affordable access to state-of-the-art technology such as the 40nm CMOS technology used in this work.

Acknowledgement

This work has been funded by the FP7 project SPIRIT and by Flanders Innovation & Entrepreneurship.

Bouncing Pixels for LoC Applications

Federal University of Minas Gerais (UFMG),
Laboratory for Optronics and Microtechnologies
(OpMA Lab), Brazil

Contact: Davies W. de Lima Monteiro

Chief designer: Pablo N. Agra Belmonte

Email: davies@ufmg.br

Technology: TSMC 180 nm CMOS technology

Die size: 1570 x 1570 μm

Description

An optical sensor/pixel capable of detecting a very wide range of input signals is generally said to feature a High Dynamic Range (HDR). Sensors with such ability are capable of detecting from the smallest signal up to a very large one, in which other regular sensors would have been saturated, missing input information. HDR operation is widely employed in Imaging Systems, from consumer to industrial applications, providing the ability to sense both dark and bright spots on the same image. Many techniques have been used, and one of the most popular are the logarithmic sensors that compress the signal response range to a rather small, but measurable voltage swing, with a loss in sensitivity as compared to the traditional linear pixels. However, both HDR and high sensitivity are desirable in order to sense the small variations of the input signal, which in some applications would be hidden by the background illumination. Among others, Lab on Chip (LoC) applications with fluorescence detection, can benefit considerably from HDR operation and high sensitivity.

We have developed a novel pixel in this IC project, that we named the Bouncing Pixel. This pixel prevents signal from saturating when the output voltage reaches VDD. Instead, the signal bounces and re-bounces within a pre-defined voltage range, swinging back and forth until the end of the integration time. The information of the number of bounces and the output voltage is combined to provide HDR operation, and very high sensitivity. This allows that even the smallest signal embedded in a large background be sensed. The project consists of a Mixed Signal system, comprising an 1024x1024 pixel array, a comparator block, and an 8-bit counter and shift-register. Although LoC applications may require only linear arrays, we have employed a squared array capable of being tested as an image sensor, allowing the comparison with

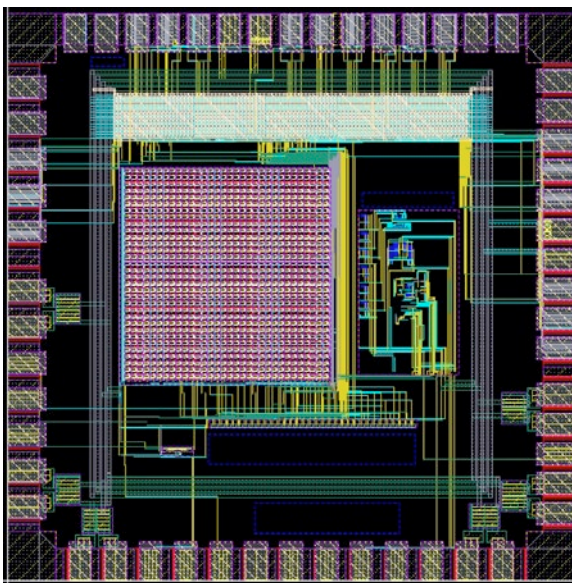


Fig.1: Layout view of the designed chip

conventional designs for HDR operation. Also, as a prototype, a squared array offers much more flexibility to be tested for other applications, besides providing more information, for instance, of Fixed Pattern Noise due to the mismatch of transistors in each pixel.

Why Europractice?

Europractice through the *mini@sic* program offers an excellent opportunity for prospective access to mature technologies, such as the CMOS TSMC 180 nm, with technical know-how to assist the designers throughout the tape-out phase. The program allows low-cost prototyping of innovative ideas, a crucial aspect for promoting microelectronics research in the academic environment.

Acknowledgement

This project has been supported by the "Brazilian National Institute of Science and Technology for Semiconductor Nanodevices" (INCT-DISSE), CNPq, CAPES and FAPEMIG.

Design of an IoT Edge Device with Power Domain Separation based on the HF-RISC Processor presenting the Crypto-SoC

GAPH and GSE research groups from Faculty of Informatics at the Pontifical Catholic University of Rio Grande do Sul, Brazil – PUCRS

Contact: Sergio J. Filho, Leandro S. Heck, Ricardo A. Guazzelli, Felipe T. Bortolon and Ney L. V. Calazans

Email: neycalazans@pucrs.br

Technology: TSMC 180 nm CMOS technology

Die size: 1550 x 1550 μm

Description of the chip and the application

HF-RISC^[1] is a 32-bit processor proposed by Sergio Johann Filho during his graduate studies (M. Sc. and Ph. D.). It has been validated in FPGAs and it currently used in several academic embedded applications and as a resource in PUCRS undergraduate course. The CSoC design objective was to employ this processor as the core of a prototype IoT edge device, showing its capability to achieve the performance^[2] of a 32-bit programmable processor associated with a potential for low power consumption^[3].

This is the second of a series of prototypes. The first prototype, SSoC, was a fully digital implementation of HF-RISC with associated ROM, RAM and a minimum set of peripherals for communication with the external world.

This second implementation of HF-RISC Crypto-SoC (CSoC), is a 32-bit architecture with a 3-stage pipeline compatible with the MIPS-I ISA, 16 KB of SRAM and 4 KB of ROM containing a bootloader software. CSoC could operate at 200 MHz but for simplicity the design target was set at 50 MHz. In addition to the SSoC hardware blocks, CSoC contains an XTEA cryptographic core. Also, the chip comprises test mode support through a scan chain and 8 extra pins for IO. Previous design issues detected in the SSoC prototype were fixed in CSoC. The block power domains are now fully split in three regions (processor core, XTEA and memories) to enable easy power consumption measurements. The reset circuit was improved to become more robust a problem detected in SSoC. To allow for a low cost IoT edge device CSoC is a chip with low pin count. While SSoC had 24 pins, CSoC is originally available in a 40-pin package. An evaluation printed circuit board developed to validate SSoC was enhanced to accept CSoC as well as SSoC DIP packages. As SSoC, CSoC can be programmed and debugged through an USB connection and its software is built using a modified versions of the GNU gcc compiler and libraries.

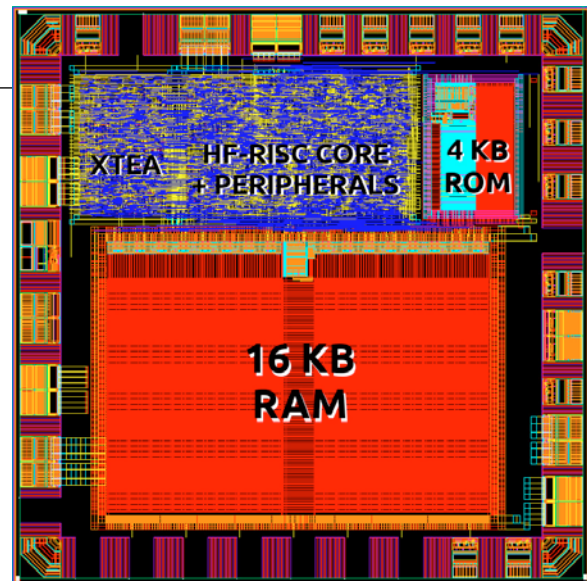


Fig.1: Layout view of the designed chip

Results

CSoC is an improvement of SSoC. Initial validation tests were conducted using the mentioned evaluation platform. The chip is now target of ongoing works that include: (1) Interfacing the CSoC chip with a FPGA board, to make it operate in test mode under the control of a host; (2) Conducting a detailed power consumption of the IC, both at the chip and at the block levels, employing the chip custom-designed power supply regions.

Why Europractice?

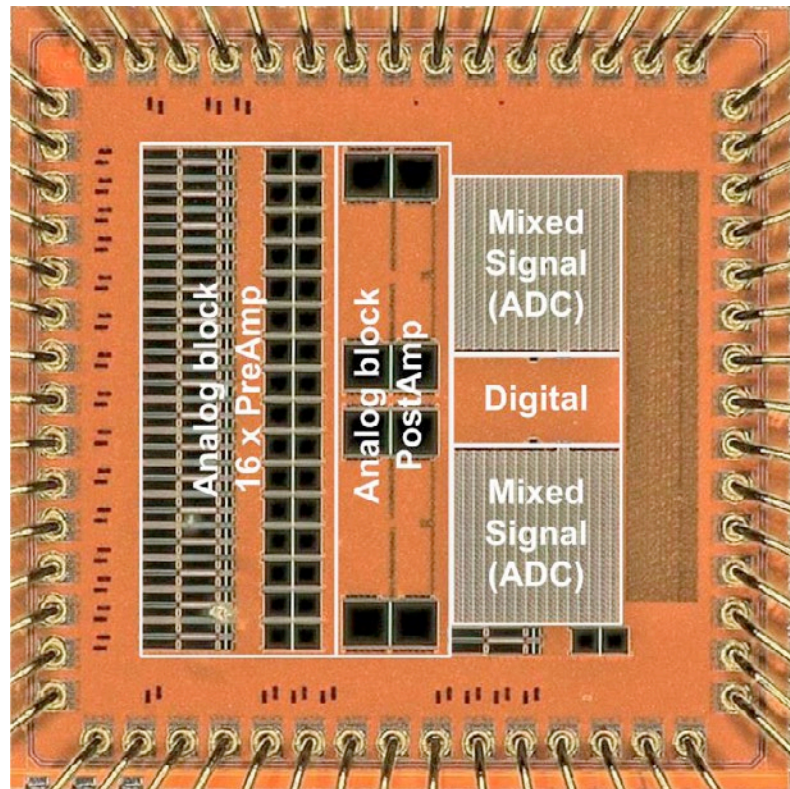
Europractice offers an opportunity for M. Sc., Ph. D. and Postdoctoral students to have contact with real IC design and fabrication processes through the *mini@sic* runs, which has proved to be an invaluable asset for our research groups. Moreover, the Europractice staff provides an excellent design support service, which has been crucial for achieving successful designs as we did, especially in the design closure phases before fabrication.

Acknowledgements

This effort has been partially supported by the Brazilian government research funding agency CNPq under grants 312556/2014-4 and 385885/2014-8 and CAPES/PROSUP project. Authors also thank the initiative and support of Prof. Jacobus Swart to this project.

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Neural Recording Integrated Circuit for the Recording of Brain Signals from Neonatal Mice

**Institute of Nano- and Medical Electronics,
Hamburg University of Technology, Germany**

Contact: Andreas Bahr, Lait Abu Saleh, Dietmar Schroeder and Wolfgang H. Krautschneider

E-mail: a.bahr@tuhh.de

Technology: UMC L130 Mixed-Mode/RF

Die size: 1520 x 1520 μm

Introduction

In the research of the development of the brain and in the research of treatments for diseases like epilepsy or autism spectrum disorders the analysis of brain signals from neonatal mice plays a critical role. The signals are analyzed during the maturation of the brain and during treatments for diseases. This enables the observation of the development processes and conclusions regarding the efficiency of a treatment. For this analysis, the brain signals are amplified and recorded. For the special case of recordings from neonatal mice a very small integrated circuit has been developed, that records the brain signal in close proximity to the brain.

In future, this circuit will be used for chronic recordings from neonatal mice during the adolescence. It will enable new insights into the development and maturation of the brain and support the development of treatments for severe diseases.

Description/application of the circuit

The integrated circuit is designed for the recording of biomedical signals from the brain. It is optimized for the neural acquisition from neonatal mice. Neonatal mice have a size of only 2-3 cm and a weight of 3–5 g. Thus, the circuitry is optimized for low area consumption and has a size of only 1.5 x 1.5 mm².

The neural signals from the brain have an amplitude range from a few micro volts up to several millivolts. Thus, very sensitive analogue circuitry is required. The bandwidth of the signals is in the range up to 10 kHz.

16 channels with analogue low noise preamplifiers amplify the signals by 34 dB. The 16 channels allow the spatial reconstruction of the source of the signals, e.g. in a depth profile from the cortex. The analog channels are connected with a multiplexer to a post-amplifier. The post-amplifier has configurable gain and a high driving capability. It charges the capacitances of the analogue-to-digital converter for the digitization of the signals. The ADC is implemented as a 10-bit successive-approximation-register (SAR) ADC. A parallel structure out of two post-amps and two ADCs, each connected to 8 channels, is used to meet the high timing requirements. For the configuration of the chip and for data transfer a digital Serial Peripheral Interface (SPI) with Reed Solomon Error Correction Coding is implemented.

The integrated circuit has been successfully taped out and used for in-vivo measurements with an adult anesthetized head fixed mice. In future, it will enable chronical recordings of the brain signals of neonatal mice. This will enable new insights into the development of the brain and support the development of treatments for many diseases.

Why Europractice?

Europractice's design kit services and organized MPW, mini@sic runs are crucial for a research project demanding small volume production at an affordable price. The Europractice staff, both at the Fraunhofer Institute and IMEC, provides excellent service and information in each stage of the chip design process. Thanks for the support!

Acknowledgement

This work was supported by the German Research Foundation, Priority Program SPP1665.

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<http://www.abstractsonline.com/pp8/index.html#!/4071/presentation/32779>

Why Europractice?

The chip tape-out was part of the research project “Mi-Soc: Multi-Source Energy Management for Self-Powered Biosensors”. Europractice offers great prototyping conditions for universities and research groups involved in such projects through their *mini@sic* concept.

Acknowledgement

The authors would like to thank the Swedish Research Council (VR) for funding this work.

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A Multi-Source Energy Harvesting Interface for Glucose Biofuel Cells and Thermoelectric Generators

KTH Royal Institute of Technology, School of Information and Communication Technology, Integrated Devices and Circuits Department, Stockholm, Sweden

Contact: Janko Katic and Prof. Ana Rusu

E-mail: katic@kth.se, arusu@kth.se

Technology: UMC L180 Mixed-Mode/RF

Die size: 1525 x 1525 μm

Description/application of the circuit

The chip is a dual-source energy harvesting interface that combines the energy from glucose biofuel cell and thermoelectric generator in order to power an implantable biosensor. The interface is based on a single-inductor dual-input dual-output boost converter that extracts the maximum possible power from both sources simultaneously, efficiently transfers that power to the load and converts the input voltages to higher levels at the same time. The converter is highly reconfigurable and can operate in different modes of operation depending on the connected harvesters. The dual-output feature allows reducing the supply voltage of the control circuit and, consequently, its power consumption [1]. The control circuit of the boost converter incorporates intensive digital functionality in order to achieve perfect switch timings and minimize the losses within the converter [2]. The chip is designed for implants, with a goal to enable reliable self-powered implantable biosensors. Therefore, the input power/voltage levels are extremely low. The combined input power extracted from the harvesters is below 70 μW , while the input voltages are less than 250 mV.

Results

The chip is implemented in a 0.18 μm CMOS process. The circuit layout and die photo of the chip are shown in Fig. 1, while the evaluation board is shown in Fig. 2. The measurement results show that the converter achieves a high conversion efficiency of more than 80% for combined input power levels above 9 μW and that it can operate from input voltages as low as 10 mV.

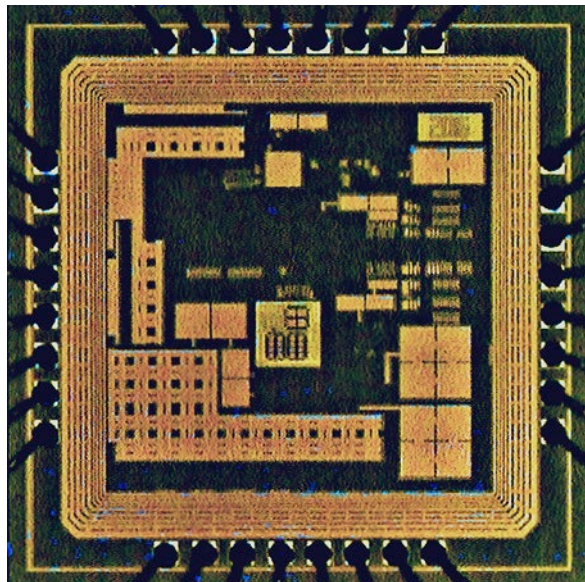
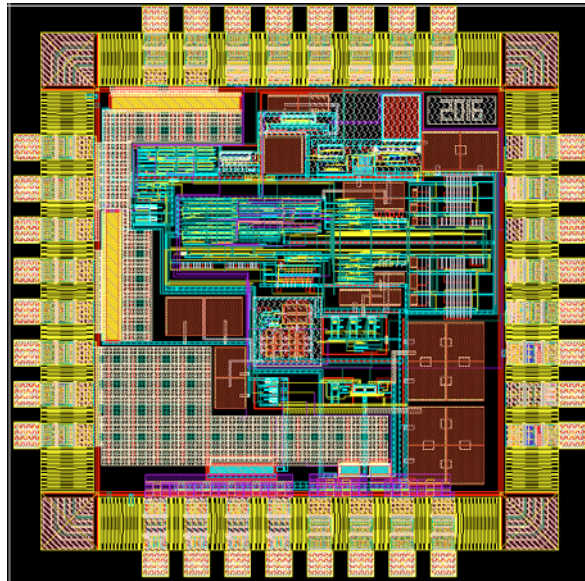


Fig.1: Layout view of test chip (top) and microscope picture of fabricated chip (bottom)

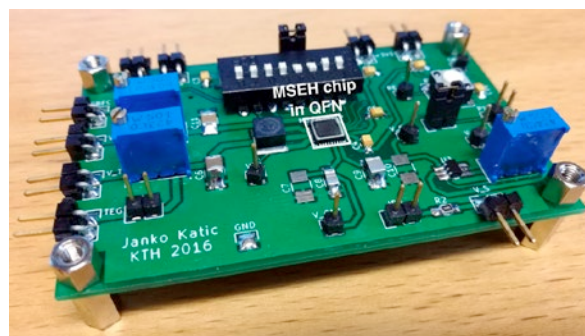


Fig.2: Evaluation board and testchip in QFN package

Highly adjustable triangular wave generator for (UWB) FMCW applications

KU Leuven Technology Campus Geel, Faculty of Engineering, Advanced Integrated Sensing lab (AdvISe)

Contact: Prof. Paul Leroux, Bram Faes and Stijn Cuypers

E-mail: paul.leroux@kuleuven.be

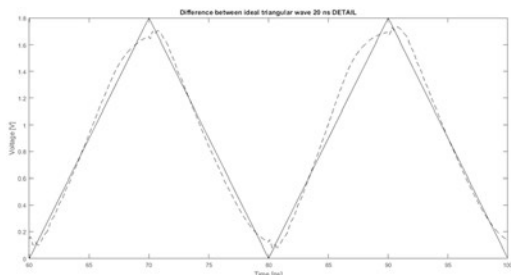
Technology: UMC L180 Mixed-Mode/RF

Die size: 1525 x 1525 μm

Description/application of the circuit

The aim of this master thesis was the design of a highly flexible rail-to-rail triangular wave signal generator. This generator can be used in highly accurate frequency modulated continuous wave (FMCW) ranging and imaging applications. To allow for the use in these applications, the design focused on the high linearity and constant pulse shape on the output. Maintaining this even when reaching the power supply or ground.

The highly linear triangular wave is created by integration of a periodic positive and negative constant current. Following this a linear increasing and decreasing function is generated. Due to charge accumulation in the active CMOS integrator, the output common mode signal may drift. This results in a decreasing linearity and clipping to one of the rails. The integrator was therefore extended with a common mode feedback circuit which prevents any clipping and loss in linearity.



The integrator's constant input current is generated by a charge pump (CP). Depending on the input frequency, this CP provides a continuous stream of half period positive or negative current. The output rise and fall times are made adjustable by altering the output current generated by the CP. Thus, altering the integration constant. A 6 bit binary word adjusts the output period between 20 ns and 200 ns, giving a 2.8 ns step size.

The entire design (charge pump + integrator) has a maximum power consumption of 18.7 mW drawn from a 1.8 V power supply.

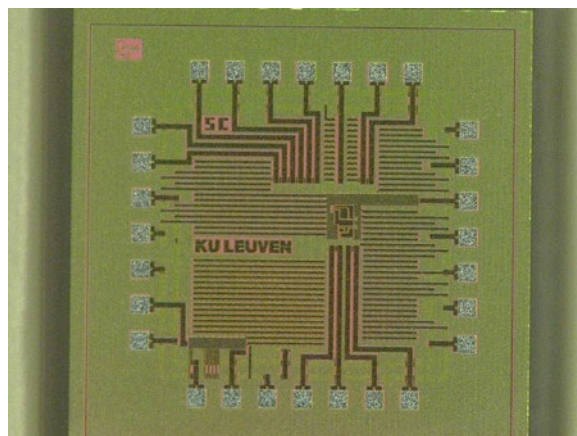


Fig.2: Microscope picture of the fabricated chip.

Results

The triangular wave generator was measured under normal operation conditions and showed a good match between simulations and measurements. The measurements showed a good linearity of the output signal with clipping starting from ± 200 mV from each rail. The table below shows the results of the rise and fall times from the 2 extreme clock periods.

Period	T_{rise}	T_{fall}
20 ns	180 MV/s	160 MV/s
200 ns	33 MV/s	28 MV/s

Why Europractice?

EUROPRACTICE offers the possibility of affordable prototyping for research. They give students of master in industrial sciences the opportunity to participate on a *mini@sic* with the UMC L180 Mixed-Mode/RF technology. This gives students a unique chance to go through the complete design process of making an ASIC.

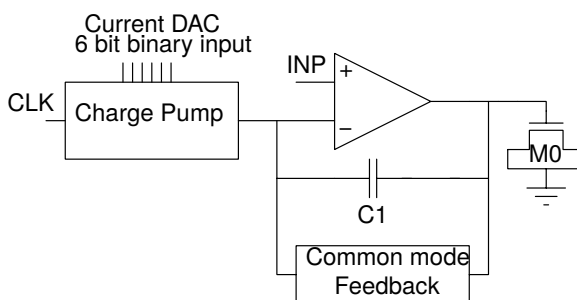


Fig.1: Basic block diagram of the circuit

All Digital PLL and 9-bit SAR ADC in GF40nm for Ultra-Low Power Wireless Systems

Imec ULP Wireless Program – Holst Centre, Eindhoven, The Netherlands

Contact: Paul Mateman, Li Huang, Christian Bachmann

Technology: Globalfoundries 40 nm CMOS technology

Die size: 1500 x 1500 μm

Introduction

Low power wireless functionality is one of the key enablers of the Internet-of-Things (IoT). The research on ULP wireless technology has resulted in a 10-fold improvement in the power consumption of these radios as compared to earlier state-of-the-art, resulting in single-digit mW power consumption figures in active transmit/receive mode for short range radio protocols such as Bluetooth Low Energy (BLE). Two critical building blocks for these ultra-low power radios are the phase locked loop (PLL) for frequency generation as well as analog-to-digital convertor (ADC) for signal quantization.

Design Description

The test chip design contains two modules required for ULP radios: A 1.8-2.6GHz fractional-N all digital PLL (ADPLL) and a 9bit, 16MSps analog-to-digital converter (ADC).

All-digital PLLs enable a smaller footprint compared to traditional analog PLLs, better control and testability, and improved scaling to advanced process technology nodes. This 1.8-2.6GHz fractional-N all digital PLL design features a new DTC with better linearity and dynamic phase selection to achieve good fractional spur performance. Several calibrations are implemented to ensure robust ADPLL operation.

The ADC employs a successive approximation (SAR) topology and features a clock-boosted sampling switch to sample the analog input signal on the DAC capacitors. The SAR algorithm, implemented with asynchronous dynamic logic, uses a dynamic comparator and a charge redistribution DAC to approximate the sampled analog input signal. The use of conversion redundancy within this SAR ADC helps to both improve the conversion accuracy and to reduce power consumption.

Fig2: Final test chip for ADPLL and ADC on evaluation board

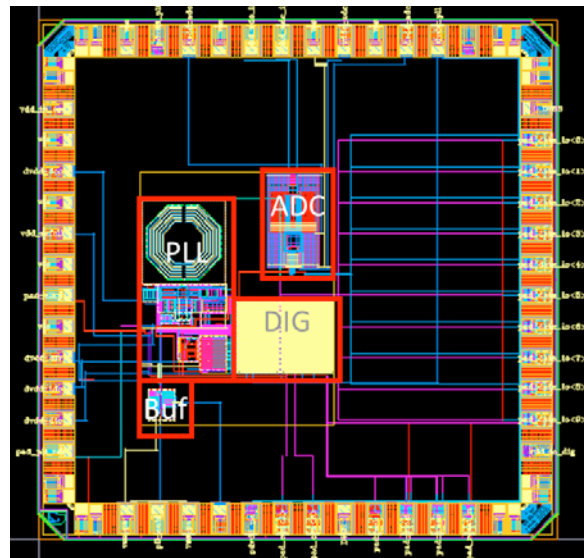


Fig.1: Top level layout of ADPLL and ADC test chip

Results

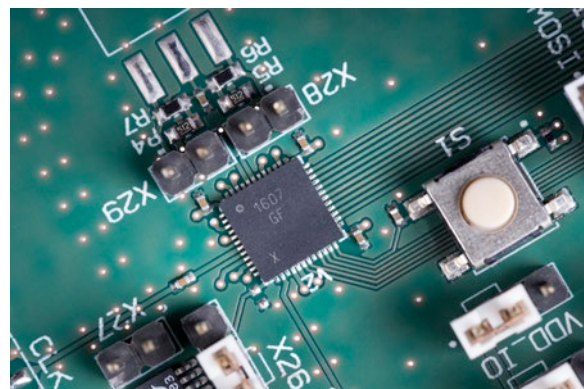
In this project imec has successfully designed, implemented and evaluated these two modules in Globalfoundries 40nm technology. The performance of the implemented designs has been verified with silicon measurements.

The 9bit, 16MSps SAR ADC achieves an ENOB of 8.29b within Nyquist frequency, while only consuming 58 μW of power. This very low power consumption of the ADC can help to significantly reduce the overall power budget of the radio in active receive mode.

The 1.8-2.6GHz fractional-N all digital PLL achieves an RMS jitter smaller than 2.3ps and in-band fractional spur lower than -48dBc, while only consuming 1.07mW of power. These good performance numbers pave the way for a more widespread industrial use of all-digital PLLs as an attractive alternative to traditional analog PLLs.

Why Europractice?

The Europractice staff, both at imec and Fraunhofer, provide excellent tape out support services and knowledgeable feedback that is crucial for a successful chip design and tape out.



9x18 array of multi-channel digital SiPM with 432 column-parallel 48ps 17b TDCs for endoscopic time-of-flight PET

Delft University of Technology, Delft, The Netherlands

Contact: Prof. Dr. Edoardo Charbon

E-mail: e.charbon@tudelft.nl

Technology: ams CMOS H18 6M

Die size: 2900 x 1740 μm

Description/application of the circuit

The application of the 9x18 array of multichannel digital SiPMs is time-of-flight (TOF) positron emission tomography (PET). This sensor can timestamp multiple light photons produced during a gamma-photon scintillation event in order to estimate the gamma photon timemark with an accurate coincidence resolving time. Particularly because of the high miniaturization level, the sensor can be integrated into a probe of an endoscopic PET scanner. (<http://endotofpet-us.web.cern.ch/endotofpet-us/>)

The sensor is a digital SiPM that features 432 time-to-digital converters (TDCs) on chip. The photon detection area is composed of an array of 67,392 (144x468) single-photon avalanche diode (SPAD) cells. In addition, the multi-channel digital SiPM (MD-SiPM) is equipped with a fast readout and photon counting logic. An optional high-voltage generator that biases the SPADs is also integrated into the die.

Each SPAD cell comprises a masking memory that allows deactivating any SPAD cells in order to suppress the cells that have higher dark count rate DCR. In addition, the SPAD cells have a passive quenching and active recharge circuit in order to operate the SPAD. Furthermore, a 1-bit memory is integrated into the SPAD cell in order to store a photon detection before is read out by the photon counting logic. The SPAD cell array is divided into subunits called MD-SiPMs and each subunit has 416 SPAD cells. The dimensions of the array of MD-SiPMs are 9x18.

The sensor has 432 TDCs on chip shared through column-parallel lines. In other words, each column of 18 MD-SiPMs shares 48 TDCs. The TDC array is controlled by a global PVT compensated VCO. The TDC LSB value is 48.5ps and the TDC range is 17 bits. The fast readout and photon counting logic has two modes of operation. The first mode allows operating the sensor as a frame-based SPAD camera; therefore, in this mode every on-cell memory can be read out along with the 432 TDC values.

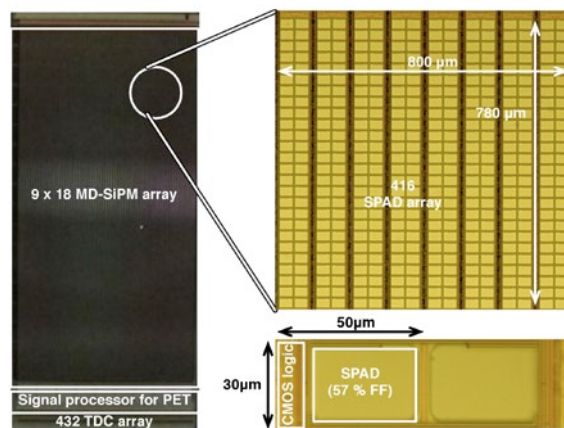


Fig.1: Microscope picture (and zoom-in) of 9x18 array of multichannel digital SiPMs.

The second mode allows operating the chip in an event-driven mode, so the sensor is read out only when there is a valid gamma-photon detection. This second mode of operation reduces significantly the dead time of the sensor. In addition, in this mode the photon counting logic is activated so the information sent from the chip corresponds to the total number of activated cells within an MD-SiPM subunit. Subsequently, the amount of transferred information is significantly lower compared to the first mode of operation.

Why Europractice?

Europractice allows our group to access state-of-the-art CMOS technologies. Therefore, we can design and implement cutting-edge technology sensors with new key features that expand the capabilities of medical imaging systems. To our knowledge and in the particular case of this sensor, this is one of the only three existing digital SiPMs that were successfully designed and implemented.

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Application of IHP's SiGe-Technology for very fast data processing

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Technology: IHP SG13 0,13µm SiGe:C

Die size: 1.4 x 2.3 mm²

Introduction

The EuRISCOSi project (Extensible ultra-fast RISC-based Operational node by using a SiGe-technology) is supported by a German BMBF programme (support code 03FH069PX3) and has been started at autumn 2014. For very fast data processing in real-time applications, at first we had to evolve a library with very fast logical gates. The name of this library is called Common_ECL. It contains ECL- and CML-based cells with propagation delays down to 5ps. Basing on this library and in cooperation with our project partners we have designed different macro blocks up to a simple operation node. The final goal of this project is to get a set of solutions for very fast data processing with clock frequencies up to 35GHz. Application fields can be:

- Interfaces for very high data rates up to 100Gbit per second
- Pattern generation with rates up to 35GSamples per second
- Encrypting / decrypting high-rate data streams and pattern detection
- Time measurements with picosecond resolutions
- Real-time data processing running a complete program in a few nanoseconds

Description

Similar as a simple CPU, our operation node consists of a control unit and a registered ALU. Data for the program and for the LUT memories will be boot-loaded from external sources by a serial CMOS based interface with lower speed up to 100MB/s. After the boot loading, the control unit contains the complete program memory for very fast operations in the directly used microprogramming format. Convenient to this, the ALU contains 8 registers, each combined with a special operation unit. In our first design, the following 8-Bit-operations are addressed:

Address	Operation
0	Read input / Write output ports
1	Addition / Subtraction
2	Logical operations (NOR, AND, XOR etc.)
3	Shift / Rotate
4	Increment / Decrement
5	Full 8Bit lookup table
6	First 8 Byte memory stack register
7	Second 8 Byte memory stack register

All the operation units can work simultaneously, therefore the ALU is able to execute up to 8 micro-instructions at the same clock period. Not used operation units can be switched off to reduce the power consumption from about 2,6W (all the units in action) down to 1,36W (only control unit is in action).

This moderate generation of heat could be reached by a new combination of ECL- and CMOS-based structures. The program memory, the LUT and the stack memories will raise the power consumption only during the fast access cycles, in which the SiGe bipolar HBTs are involved. In the off-state, data in the memory stack registers are forwarded to their CMOS sections, where the data is stored in SRAM cells. For further processing the data has to get back to the ECL-section of the register. All the other operation units only can latch their last output data during the off-state. They do not have any CMOS memories.

The data communication between all the ALU units is realized by a full multiplexed bus configuration. It means, all the units are able to receive data from any other unit at any time. The basic structure of the whole operation node is shown in Fig. 1.

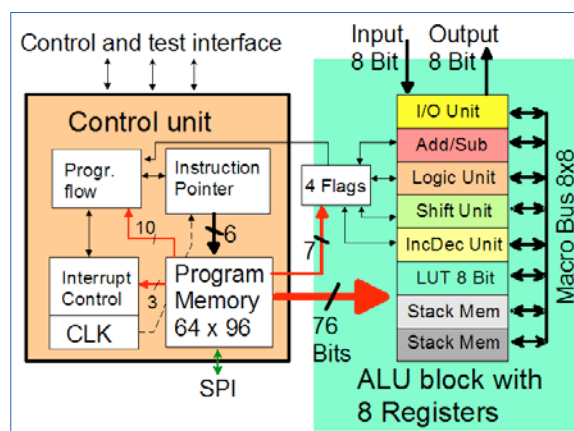


Fig. 1: Basic architecture of the Operational node

The control unit contains a program memory that generates a long instruction word of 96 Bits. A subset of 76 Bits are branched off to the ALU and register block. By this way, the ALU may pass some load-, store- and processing operations at the same cycle, while the control unit simultaneously may execute a jump instruction, a flag manipulation and an interrupt handling during the same clock-cycle.

The clock generator is able to deliver the clock in a wide frequency range of 1GHz minimum and 35GHz maximum. It is directly connected to the instruction pointer. Therefore, every clock cycle is identical with one instruction cycle.

All the operation units get their separated clocks directly from the program memory. The data of all operation units will be stable until the next rising program clock edge comes in. Furthermore, every unit can be separately switched-off by the program whenever its special operation is not required. So, one can see that a lot of different control signals are needed. The development of the design was made manually because all the high-speed signals must be wired full differentially. Due to the application of a hierarchical design flow with up to eight levels, the complexity was manageable. In the result, we were surprised that the occupied chip area was limited by the number of needed bond pads, not by the area of the library cells! The result of the total chip design is shown in Fig. 2.

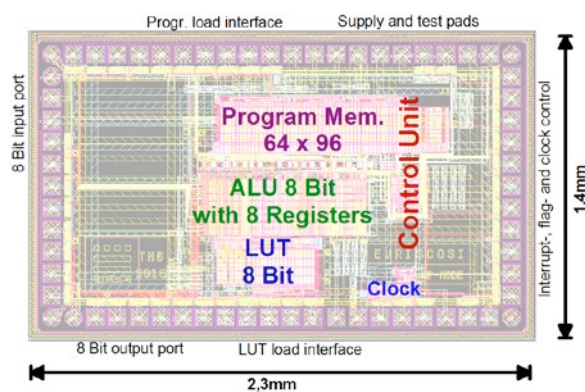


Fig. 2: Placement and chip size of the EuRISCOSi operation node

The design of the operation node was finished in December 2016 and first samples will be available in April 2017. Main structures, e.g. clock generation, memory blocks and some operation units were already tested in former designs on silicon. The goal of the next tests will be to evaluate how fast the control unit and the components of the ALU will operate in practice.

Next steps in the EuRISCOSi project are measurements and the evaluation of the practical results. The design was optimized to get very differentiated information about the real internally working speed of the components. In the future, some pads for testing may be replaced by other functions. For further developments, the following steps are planned:

- inclusion of a fast serial interface with 8Bit/10Bit conversions,
- improvements of the control unit, e.g. involving more stack levels for the instruction pointer and optimization of the microcode,
- integration of more operation units, e.g. a multiplier

If a special application requires a specific configuration of operation units, it is quite easy to replace one component of the ALU by another.

Why Europractice?

For the THB as an education institution, the Europractice way is the most practicable way for design and prototyping. Furthermore, this offers a choice of the best technologies for a given application to reach outstanding performances. Needed CAD tools are available and a good support in design is given. So we could involve some students into this project. The *mini@sic* program also was a very good way for packaging our chips. Our team acknowledges the support granted by the Fraunhofer's Europractice staff.

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- Kell, G., Schulz, D.: EuRISCOSi Presentation and booth at the Hannovermesse, 24.-29. April 2016

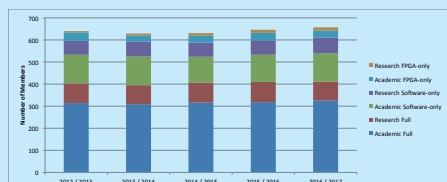
EUROPRACTICE MEMBERSHIP

The funding requested from the EC is far from sufficient to offer the EUROPRACTICE high quality service to >600 European universities and research institutes. Membership Fees pay for extra staff supporting this requested stimulation activity for academic institutions (not fully paid by the EU). The annual Membership Fee is collected by STFC on behalf of the EUROPRACTICE project partners.

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Allowing access to FPGA tools only e.g. Altera, Xilinx, and Synopsys Synplify.

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R21350	Centre Algérien de Développement des Technologies Avancées
Austria	
A00500	Fachhochschule Kärnten
A13020	Fachhochschulstudiengänge Oberösterreich
A13470	Technische Universität Wien Institute of Telecommunications
A14240	Fachhochschule Technikum Wien
A14480	Fachhochschule Joanneum
A15350	Fachhochschule Wiener Neustadt
A15640	Universität Innsbruck
A15880	Johannes Kepler Univ, Linz (NTHFS)
A15980	Höhere Technische Bundeslehr- und Versuchsanstalt Rankweil
A35090	Technische Universität Wien
A36470	Technische Universität Graz
A38430	Johannes Kepler Universität Linz
R21070	AIT Austrian Institute of Technology
R21210	Österreichische Akademie der Wissenschaften - Wien
R21590	Österreichische Akademie der Wissenschaften - Graz
R22330	Joanneum Research Forschungsgesellschaft mbH
Belarus	
A47630	Belarusian State University of Informatics and Radioelectronics

 Belgium	
A15890	Université de Liège
A35651	Université Catholique de Louvain
A35880	Universiteit Gent
A37190	Universiteit Antwerpen
A37210	Vrije Universiteit Brussel
A37220	Katholieke Universiteit Leuven
A38160	Université de Mons
A38190	Université Libre de Bruxelles
R00040	imec
R21440	Studiecentrum voor Kernenergie - Centre d'Etude de l'énergie Nucléaire


 Bulgaria	
A40090	Technical University of Sofia

 Croatia	
A47680	University of Zagreb
A47920	J.J. Strossmayer University of Osijek

 Cyprus	
A07090	University of Cyprus

 Czech Republic	
A40060	Czech Technical University in Prague
A40070	Technical University of Brno
R47460	Institute of Physics, Academy of Sciences
R49000	Ústav teorie informace a automatizace AV CR

 Denmark	
A13030	Københavns Universitet
A14520	University of Southern Denmark
A15510	Aarhus Universitet
A35060	Aalborg Universitet
A36040	Danmarks Tekniske Universitet

 Egypt	
A14550	Ain Shams University
A14670	Cairo University
A15090	The German University in Cairo
A15160	The American University in Cairo
A15170	Egypt-Japan University of Science & Technology
A15590	Military Technical College
A16020	Zewail City of Science & Technology

 Estonia	
A40110	Tallinn Technical University

 Finland	
A15740	Satakunnan ammattikorkeakoulu
A15800	Lappeenranta teknillinen yliopisto
A35040	Aalto University
A35610	Tampere University of Technology
A35820	University of Oulu
A37000	Oulu University of Applied Sciences
A39360	University of Turku
R14360	Helsinki Institute of Physics
R21240	VTT Technical Research Centre of Finland
R21730	Finnish Meteorological Institute FMI

 France	
A00100	ISAE - Institut Supérieur de l'Aéronautique et de l'Espace
A13260	ENSMM - École Nationale Supérieure de Mécanique et des Microtechniques
A13800	Université de Lorraine
A14410	École des Hautes Etudes d'Ingénieur
A14440	Laboratoire de Physique Corpusculaire de CAEN
A15600	Université Pierre et Marie Curie - Institut de la Vision
A35020	Université Pierre et Marie Curie - L2E
A35290	Université de Montpellier 2
A35370	École Nationale Supérieure de l'Electronique et de ses Applications
A35800	Institut Supérieur d'Electronique et du Numérique
A36061	Centre Interuniversitaire de Microélectronique et de Nanotechnologies
A36311	Institut National des Sciences Appliquées de Lyon
A36312	École Supérieure de Chimie Physique Électronique de Lyon
A36410	Atelier Interuniversitaire de Microélectronique
A37470	Université de Strasbourg
A37590	Aix Marseille Université
A37670	Laboratoire de Physique Nucléaire et de Hautes Energies
A37710	Télécom Bretagne
A37950	Université Claude Bernard Lyon 1
A37980	Université Joseph Fourier
A39060	Laboratoire d'Annecy-le-Vieux de physique des particules
A39400	Université Blaise Pascal
R00210	Laboratoire d'Analyse et d'Architectures des Systèmes
R14140	ICube Laboratory
R15140	XLIM Université de Limoges
R20490	European Synchrotron Radiation Facility
R20810	Station de Radioastronomie de Nançay, Observatoire de Paris
R20980	Laboratoire des Plasmas et de Conversion d'Energie (LAPLACE)
R21010	Laboratoire de Physique et Chimie de l'Environnement et de l'Espace
R21020	Synchrotron SOLEIL
R21030	Institut Matériaux Microélectronique Nanosciences de Provence
R21140	Institut Laue-Langevin
R21170	Laboratoire de l'Accélérateur Linéaire
R21270	Commissariat à l'Energie Atomique (CEA-IRFU)
R21290	Spintronique et Technologie des Composants
R21380	Laboratoire de Physique des Plasmas
R21410	Laboratoire Leprince-Ringuet
R21420	Office National d'Études et de Recherches Aérospatiales - Châtillon
R21560	Office National d'Études et de Recherches Aérospatiales - Toulouse
R21960	Institut de recherche en astrophysique et planétologie
R22060	Institut d'Astrophysique Spatiale
R22130	Observatoire de Paris - LESIA
R22190	LSIS - Laboratoire des Sciences de L'Information et des Sciences
R22210	Centre de Microélectronique OMEGA

R22220	Commissariat à l'énergie atomique et aux énergies alternatives - Grenoble
R22240	Le Laboratoire PROcédés, Matériaux et Énergie Solaire
R22280	Institut de Recherche sur les Composants logiciels et matériels pour l'Information et la Communication Avancée
R22310	Grand Accélérateur National d'Ions Lourds
R22320	Laboratoire Hubert Curien
R22360	IRT SAINT-EXUPERY
R37850	Laboratoire de l'Accélérateur Linéaire
R38290	Laboratoire de l'Intégration du Matériau au Système
	Germany
A00110	Johannes Gutenberg Universität Mainz
A00240	Fachhochschule Köln
A00510	Hochschule Konstanz für Technik, Wirtschaft und Gestaltung
A00670	Hochschule Bremen
A00850	Justus Liebig-Universität Gießen
A12140	Technische Universität München - Fakultät für Physik (Garching)
A12270	Hochschule Albstadt-Sigmaringen
A12410	Fachhochschule Schmalkalden
A12440	Hochschule Pforzheim
A12540	Brandenburgische Technische Universität Cottbus
A12840	Bergische Universität Wuppertal
A13050	Duale Hochschule Baden-Württemberg
A13060	Albert-Ludwigs-Universität Freiburg Institut für Mikrosystemtechnik (IMTEK)
A13610	Fachhochschule Aachen
A13650	Technische Universität Darmstadt - Institut für Halbleitertechnik und Nanoelektronik (IHT)
A13660	Universität Bremen - Informatik
A13680	Hochschule Aschaffenburg
A13880	Hochschule für Technik und Wirtschaft des Saarlandes
A13890	Technische Universität Berlin
A14130	Fachhochschule Brandenburg
A14740	Universität Kassel - Fachbereich Elektrotechnik/Informatik
A14920	Universität Konstanz
A15030	Universität Bielefeld
A15230	Hochschule für Angewandte Wissenschaften Hamburg
A15330	Carl von Ossietzky Universität Oldenburg - Energie und Halbleiterforschung (EHF)
A15410	Technische Hochschule Mittelhessen - Friedberg
A15500	Hochschule RheinMain
A15660	Ludwig-Maximilians-Universität München
A15840	Hochschule Rosenheim
A15930	Fachhochschule Südwestfalen
A15950	Beuth University of Applied Sciences
A16030	Rheinisch-Westfälische Technische Hochschule Aachen - Lehrstuhl für Integrierte Photonik (IPH)
A16040	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Stromrichtertechnik und Elektrische Antriebe (ISEA)
A16060	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Theoretische Elektrotechnik (ITHE)
A16090	Westfälische Hochschule

A16100	Hochschule fuer Technik und Wirtschaft Berlin (HTW Berlin)
A35320	Technische Universität Hamburg-Harburg
A35400	Hochschule Ulm
A35420	Georg-Simon-Ohm Hochschule Nürnberg
A35430	Karlsruher Institut für Technologie
A35450	Technische Universität Darmstadt - Integrierte Elektronische Systeme (IES)
A35500	Eberhard Karls Universität Tübingen
A35590	Johannes-Wolfgang-Goethe-Universität Frankfurt am Main
A35600	Technische Universität Braunschweig
A35620	Universität Bremen - Institut für Theoretische Elektrotechnik und Mikroelektronik
A35640	Rheinisch-Westfälische Technische Hochschule Aachen - Institute for Communication Technologies and Embedded Systems (ICE)
A35710	Hochschule Augsburg
A35810	Technische Universität Kaiserslautern
A35830	Universität Hamburg
A35990	Universität Duisburg-Essen
A36070	Carl von Ossietzky Universität Oldenburg - Informatik
A36440	Universität des Saarlandes
A37090	Technische Universität Dortmund
A37240	Hochschule Furtwangen
A37290	Leibniz Universität Hannover
A37310	Technische Universität Berlin
A37380	Friedrich-Alexander-Universität Erlangen-Nürnberg
A37390	Technische Universität München - Fakultät für Elektrotechnik und Informationstechnik
A37440	Universität der Bundeswehr München
A37450	Hochschule Esslingen
A37500	Universität Paderborn
A37510	Hochschule für Angewandte Wissenschaften München
A37530	Humboldt-Universität zu Berlin
A37540	Universität Ulm
A37760	Technische Universität Dresden
A37800	Hochschule Offenburg
A37810	Rheinisch-Westfälische Technische Hochschule Aachen - Fakultät für Elektrotechnik und Informationstechnik
A37880	Hochschule Aalen
A37920	Hochschule Ravensburg-Weingarten
A37930	Hochschule Mannheim
A38010	Hochschule Heilbronn
A38030	Hochschule Darmstadt
A38080	Ruhr-Universität Bochum
A38090	Otto-von-Guericke-Universität Magdeburg
A38220	Universität Siegen
A38240	Technische Universität Ilmenau
A38340	Technische Universität Chemnitz
A38390	Ruprecht-Karls-Universität Heidelberg - Mannheim
A38550	Ostfalia Hochschule für angewandte Wissenschaften
A38650	Fachhochschule Dortmund
A38890	Rheinische Friedrich-Wilhelms-Universität Bonn
A38940	Ernst-Abbe-Fachhochschule Jena
A39000	Technische Hochschule Mittelhessen - Gießen
A39110	Universität Stuttgart








A39220	Universität Rostock
A39250	Ruprecht-Karls-Universität Heidelberg - Heidelberg
A39260	Albert-Ludwigs-Universität Freiburg
A39320	Jade Hochschule
A39330	Hochschule Reutlingen
A39340	Martin-Luther-Universität Halle-Wittenberg
A39460	Christian-Albrechts-Universität zu Kiel
A39580	Hochschule Osnabrück
A39660	Friedrich-Schiller-Universität Jena
A39770	Universität zu Lübeck
R00150	Max-Planck-Institut für Physik
R00290	Karlsruher Institut für Technologie Campus Nord
R20300	Institut für Mikroelektronik- und Mechatronik - Systeme gemeinnützige GmbH
R20330	Deutsches Elektronen-Synchrotron
R20460	Institut für Mobil- und Satellitenfunktechnik GmbH
R20510	IHP GmbH - Leibniz-Institut für innovative Mikroelektronik
R20720	Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und -Systeme
R20880	GSI Helmholtzzentrum für Schwerionenforschung GmbH
R20890	Fraunhofer-Institut für Siliziumtechnologie
R20900	Fraunhofer-Institut für Biomedizinische Technik
R20920	Fraunhofer-Institut für Integrierte Schaltungen - Erlangen
R20930	Fraunhofer-Institut für Integrierte Schaltungen - Dresden
R21050	Max-Planck-Institut für Chemie
R21060	Forschungszentrum Jülich
R21090	Fraunhofer Heinrich-Hertz-Institut
R21120	Max Planck Institut für extraterrestrische Physik
R21150	Physikalisch-Technische Bundesanstalt
R21220	Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie
R21260	Hochschule für Technik und Wirtschaft Dresden
R21310	Fraunhofer-Institut für Photonische Mikrosysteme
R21320	Fraunhofer-Institut für Solare Energiesysteme
R21510	Deutsches Zentrum für Luft- und Raumfahrt - Berlin
R21530	Deutsches Zentrum für Luft- und Raumfahrt - Bremen
R21540	Max-Planck-Institut für biophysikalische Chemie
R21580	Deutsches Zentrum für Luft- und Raumfahrt IIP - Berlin
R21610	Helmholtz-Zentrum Berlin für Materialien und Energie
R21620	Fraunhofer-Einrichtung für Angewandte und Integrierte Sicherheit
R21630	Fraunhofer-Institut für Zerstörungsfreie Prüfverfahren
R21650	Fraunhofer-Institut für Hochfrequenzphysik und Radartechnik
R21660	Fraunhofer-Einrichtung für Systeme der Kommunikationstechnik
R21770	Konrad-Zuse-Zentrum für Informationstechnik Berlin
R21780	Deutsches Zentrum für Luft- und Raumfahrt - Wessling
R21790	NaMLab gGmbH
R21860	EWE-Forschungszentrum für Energietechnologie NEXT ENERGY e.V
R21900	Max-Planck-Institut für Radioastronomie
R21970	PNSensor gGmbH
R22020	European XFEL
R22080	Fraunhofer COMEDD

R22110	Physikalisch-Technische Bundesanstalt - Berlin
R22150	Fraunhofer Institute SIT
R22160	Halbleiterlabor der Max Planck Gesellschaft
R22260	Helmholtz-Zentrum Geesthacht
R22290	Fraunhofer-Einrichtung für Mikrosysteme und Festkörper- Technologien EMFT
R22300	Max-Planck-Institut für Informatik
R22340	Optotransmitter-Umweltschutz-Technologie e.V
	Ghana
A14770	Kwame Nkrumah University of Science & Technology
	Greece
A00530	University of Ioannina
A12451	Technological Educational Institute of Crete
A13550	University of Thessaly
A13690	Technological Educational Institute Stereas Elladas
A14150	Athens University of Economics and Business
A14340	University of the Peloponnese
A14700	University of Piraeus
A15110	Technological Educational Institute of Western Macedonia
A35140	National Technical University of Athens
A35960	University of Patras - Electrical and Computer Engineering
A37550	National and Kapodistrian University of Athens
A37680	University of Patras - Engineering and Informatics
A39280	Aristotle University of Thessaloniki
A39490	Technical University of Crete
R20790	Demokritos, National Center for Scientific Research
R21080	Foundation for Research and Technology Hellas
	Hungary
A40010	Budapesti Muszaki és Gazdaságtudományi Egyetem
A47540	Pázmány Péter Katolikus Egyetem
R22230	Magyar Tudományos Akadémia Atommagkutató Intézet
	Ireland
A12970	Limerick Institute of Technology
A13410	Institute of Technology, Carlow
A13440	National University of Ireland, Maynooth
A15730	University College Dublin
A35300	University College Cork
A36490	Trinity College, University of Dublin
A36510	University of Limerick
A39310	Institute of Technology, Tallaght
R21720	Tyndall National Institute
	Israel
A13330	Technion - Israel Institute of Technology
A13910	Ben-Gurion University of the Negev
A13920	Bar-Ilan University
A14070	Ort Braude College of Engineering
A14380	Tel-Aviv University
A14540	Kinneret College on the Sea of Galilee
A14690	Holon Institute of Technology
A15190	Jerusalem College of Technology



Italy

A00120	Università Politecnica delle Marche
A00520	Università degli Studi di Modena e Reggio Emilia - Modena
A00560	Università degli Studi di Siena
A00680	Università della Calabria
A00740	Università degli Studi di Perugia
A12000	Università di Bologna - DEIS
A12370	Università degli studi di Napoli Federico II - Dipartimento di Ingegneria Elettronica e delle Telecomunicazioni
A12390	Università degli Studi di Brescia
A12430	Università degli Studi Mediterranea di Reggio Calabria
A12530	Università degli Studi di Verona
A12640	Università degli Studi di Milano
A12770	Università del Salento
A12990	Università degli Studi di Bergamo
A13280	Università degli Studi di Udine
A14020	Università degli studi di Napoli Federico II - Dipartimento di Fisica
A14220	Università degli Studi di Trento
A14800	Università degli Studi di Milano-Bicocca
A14820	Università degli Studi di Salerno
A14860	Università degli Studi di Modena e Reggio Emilia - Reggio Emilia
A15070	Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna
A15750	Università Degli Studi di Cassino e del Lazio Meridionale
A15900	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Cesena)
A16130	Università degli Studi Roma Tre
A35210	Università degli Studi di Parma
A35530	Politecnico di Torino
A35660	Università di Pisa
A35690	Politecnico di Milano
A35910	Università degli Studi di Genova
A36380	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Bologna)
A37280	Università degli Studi di Pavia
A37460	Università degli Studi di Catania
A37520	Università degli Studi di Ferrara
A38380	Politecnico di Bari
A38620	Università degli Studi di Torino
A38840	Università degli Studi di Roma "La Sapienza"
A39200	Università degli Studi di Padova
A39410	Università degli Studi dell'Aquila
A39550	Università degli Studi di Firenze
A39550	Università degli Studi di Firenze
A39570	Università degli Studi di Cagliari
R00140	Fondazione Bruno Kessler
R00270	Istituto Nazionale di Fisica Nucleare, Sezione di Genova
R00300	Istituto Nazionale di Fisica Nucleare, Sezione di Pisa
R20310	Istituto Nazionale di Fisica Nucleare, Sezione di Roma
R20320	Istituto Nazionale di Fisica Nucleare, Sezione di Roma II
R20400	Istituto Nazionale di Fisica Nucleare, Sezione di Bologna
R20420	Istituto Nazionale di Fisica Nucleare, Sezione di Trieste
R20440	Istituto Nazionale di Fisica Nucleare, Sezione di Torino

R20450	Istituto Nazionale di Fisica Nucleare, Laboratori Nazionali di Frascati
R20470	Istituto Nazionale di Fisica Nucleare, Sezione di Padova
R20550	Elettra-Sincrotrone Trieste
R20560	Istituto Nazionale di Fisica Nucleare, Sezione di Roma III
R20580	Istituto Nazionale di Fisica Nucleare, Laboratori Nazionali di Legnaro
R20630	Istituto Nazionale di Fisica Nucleare, Sezione di Milano
R20670	Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari
R20710	Istituto Nazionale di Fisica Nucleare, Sezione di Bari
R20990	Istituto Nazionale di Fisica Nucleare, Sezione di Ferrara
R21100	Istituto Nazionale di Fisica Nucleare, Sezione di Napoli
R21160	Istituto Nazionale di Astrofisica, Osservatorio Astrofisico di Arcetri
R21190	Istituto Nazionale di Fisica Nucleare, Laboratori Nazionali del Gran Sasso
R21300	Consiglio Nazionale delle Ricerche, Istituto per la Microelettronica e i Microsistemi
R21450	Istituto Nazionale di Fisica Nucleare, Sezione di Pavia
R21570	Istituto Nazionale di Astrofisica, Istituto di Radioastronomia
R21600	Istituto Italiano di Tecnologia
R21800	Consiglio Nazionale delle Ricerche, Istituto per la Microelettronica e i Microsistemi Roma
R21940	The Abdus Salam International Centre for Theoretical Physics
R22010	INAF - Osservatorio Astronomico di Cagliari
R22040	INAF Milano
R22070	Istituto per lo Studio dei Materiali Nanostrutturati
R22120	INAF - IRA Radiotelescopi di Medicina
R22200	Radio Analog Micro Electronics srl
	Jordan
A15990	Princess Sumaya University for Technology
A16080	Yarmouk University
A16140	Jordan University of Science & Technology
	Kazakhstan
A48080	Nazarbayev University
	Lebanon
A15720	Lebanese American University
A47650	American University of Beirut
	Lithuania
A40230	Kauno Technologijos Universitetas
A47980	Vilniaus Universitetas
A48050	Vilnius Gediminas Technical University
	Luxembourg
A15780	Université du Luxembourg
	Malta
A38720	University of Malta
	Norway
A00840	Høgskolen i Sør-Trøndelag
A12750	Høgskolen i Sørøst-Norge
A13580	Norges teknisk-naturvitenskapelige universitet - Institutt for datateknologi og informatikk

A37360	Universitetet i Oslo
A37560	Norges Teknisk Naturvitenskapelige Universitet - Institutt for elektroniske systemer
A37820	Universitetet i Bergen
R21460	SINTEF Stiftelsen for industriell og teknisk forskning

Poland

A40100	Uniwersytet Zielonogórski
A40120	Politechnika Warszawska
A40130	Politechnika Łódzka - Mikroelektroniki i Technik Informatycznych (DMCS)
A40140	Akademia Górniczo-Hutnicza im. Stanisława Staszica
A40150	Henryk Niewodniczanski Institute of Nuclear Physics (PAN)
A40160	Politechnika Wroclawska
A40530	Politechnika Slaska
A47300	Politechnika Gdanska
A47400	Politechnika Poznanska - Inzynierii Komputerowej
A47580	Wojskowej Akademii Technicznej
A47670	Politechnika Poznanska - Radiokomunikacji
A47740	Politechnika Łódzka - Pólprzewodnikowych i Optoelektronicznych
A47940	Lublin University of Technology
R40030	Instytut Technologii Elektronowej
R49030	Instytut Podstawowych Problemów Techniki PAN (IPPT-PAN)
R49050	Bioinfobank Institute
R49080	Centrum Badan Kosmicznych PAN

Portugal

A12310	Universidade Nova de Lisboa
A12550	Universidade do Minho
A13710	Instituto Superior de Engenharia de Lisboa
A35540	Universidade do Porto
A35670	Universidade de Aveiro
A35970	Instituto Superior Técnico
A37230	Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento
R14120	Instituto de Telecomunicações - Lisboa
R21710	Laboratório de Instrumentação e Física Experimental de Partículas
R21750	International Iberian Nanotechnology Laboratory
R21890	Instituto de Telecomunicações - Aveiro
R22170	Instituto de Sistemas Robótica (ISR-UC)

Romania

A15520	Universitatea Politehnica din Bucuresti
A16070	Universitatea Transilvania Brasov
A48070	Universitatea Tehnica din Cluj-Napoca
R49010	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Nuclear Hadrons
R49060	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Particle Physics

Russia

A40240	Vladimir State Technical University named after Alexander and Nikolay Stoletovs
A47330	St. Petersburg State Polytechnical University
A47520	National Research University of Electronic Technology (MIET)
A47790	St. Petersburg State University of Aerospace Instrumentation
A47800	N.I. Lobachevsky State University of Nizhni Novgorod
A47810	Lomonosov Moscow State University
A47850	Moscow Institute of Physics & Technology (MIPT) - Wireless Technologies
A47990	St. Petersburg Electrotechnical University "LETI"
A48030	Omsk State Technical University
A48040	Moscow Institute of Physics & Technology (MIPT) - Control Systems
A60020	State University-Education-Science-Production Complex
A60030	Tomsk State University
A60040	Tomsk State University of Control Systems and Radioelectronics
A60060	Mordovian State University named after N.P.Ogarev
A60080	Novosibirsk State Technical University
A60110	National Research Nuclear University MEPhI
A60140	MV Lomonosov Moscow State University
A60150	Moscow Institute of Physics & Technology (MIPT) - Cybernetics
A60160	Bauman Moscow State Technical University - Kaluga
A60170	Moscow State Technical University of Radioengineering, Electronics and Automation
A60190	Bauman Moscow State Technical University - Moscow
A60200	Rzhanov Institute of Semiconductors Physics
A60220	Voronezh State Academy of Forestry Engineering
A60230	Samara National Research University (Samara University)
R21930	Scientific Manufacturing Complex "Technological Centre" MIET (SMCTC)
R47900	Budker Institute of Nuclear Physics
R49070	Space Research Institute (IKI)

Serbia

A47510	Univerzitet u Nišu
A47600	Univerzitet u Novom Sadu
A48010	University of Belgrade

Slovakia

A40050	Slovenská technická univerzita v Bratislave
A47930	Technical University of Kosice

Slovenia

A40280	Univerza v Ljubljani
A47690	Institut "Jožef Stefan"
A47820	Univerza v Mariboru

South Africa

A14560	University of Pretoria
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Spain

A12320	Universidad Politécnica de Cartagena
A12470	Universidad Rey Juan Carlos
A12590	Universidad de Castilla - La Mancha
A13150	Universitat de València
A13340	Universidad de Alcalá
A13860	Universidad de Salamanca
A14080	Universitat Politècnica de Catalunya - departament de Ciències de la Computació (CS)
A14400	Universitat Politècnica de Catalunya - HiPICS
A14720	Universidad de La Laguna
A15100	Universitat Politècnica de Catalunya - Manresa
A15370	Universidad de Deusto
A16110	Universitat Politècnica de Catalunya - Arquitectura de Computadors
A35130	Universidad Politécnica de Madrid - Departamento de Ingeniería Electrónica
A35190	Universitat Politècnica de València
A35560	Universitat Politècnica de Catalunya - Departamento de Ingeniería Electrónica (Campus Sud)
A35870	Universidad de Sevilla - Instituto de Microelectrónica de Sevilla (IMSE-CNM)
A35891	Universidad de Cantabria
A36250	Universitat Autònoma de Barcelona
A36390	Universidad de Las Palmas de Gran Canaria - Instituto Universitario de Microelectrónica Aplicada (IUMA)
A37060	Universidad de Zaragoza - Dpto.Ingeniería Electronica y Comunicaciones
A37080	Universidad de Santiago de Compostela
A37330	Universidad Complutense de Madrid
A37580	Universidad de Malaga
A37690	Universidad del País Vasco
A38330	Universidad de Vigo
A38360	Universitat de les Illes Balears
A38580	Universidad de Sevilla - Ingeniería Electronica
A38590	Universidad de Granada
A38600	Universidad de Navarra
A38660	Universitat de Barcelona
A38780	Universidad de Las Palmas de Gran Canaria - Departamento de Informática y Sistemas
A38790	Universidad de Zaragoza - Facultad de Ciencias
A38820	Universidad Politécnica de Madrid - Centro de Electrónica Industrial
A39080	Universidad de Extremadura
A39100	Universidad Pública de Navarra
A39150	Universitat Politècnica de Catalunya - Departamento de Ingeniería Electrónica (Campus Nord)
A39180	Universitat Rovira i Virgili
A39300	Escola Universitària Salesiana de Sarrià
A39390	Universitat Autònoma de Madrid
A39540	Universidad Carlos III de Madrid
R00060	CNM - Instituto de Microelectrónica de Barcelona
R20700	Ikerlan
R20850	Centre Tecnològic de Telecomunicacions de Catalunya
R21230	Instituto de Física Corpuscular

R21520	Institut de Ciències de L'Espai
R21550	Institut de Ciències Fotòniques
R21740	Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
R21910	Centro de Acústica Aplicada y Evaluación No Destructiva
R22100	Barcelona Supercomputing Center



Sweden

A00260	Luleå tekniska universitet
A13720	Uppsala universitet
A37350	Linköpings universitet
A37370	Lunds universitet
A38180	Kungliga Tekniska högskola
A38670	Chalmers Tekniska högskola
A39840	Mittuniversitetet
R20690	Acreo Swedish ICT AB
R20910	Totalförsvarets forskningsinstitut FOI
R21990	European Spallation Source
R22050	Institutet för Rymdfysik
R22140	European Spallation Source ESS AB






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A05000	Scuola Universitaria Professionale della Svizzera Italiana
A12730	École Polytechnique Fédérale de Lausanne - Laboratoire de Physique des Hautes Energies
A12920	Universität Zürich
A13090	Università della Svizzera Italiana
A13630	Université de Genève
A14780	École d'Ingénieurs et d'Architectes de Fribourg
A14930	Haute École Spécialisée de Suisse Occidentale
A15050	Haute Ecole d'Ingénierie et de gestion du canton de Vaud
A15480	Universität Basel
A15530	Universität Bern
A36110	École Polytechnique Fédérale de Lausanne - Microelectronics Systems
A37340	École Polytechnique Fédérale de Lausanne - Neuchâtel
A38100	Hochschule für Technik Rapperswil
A38310	Eidgenössische Technische Hochschule Zürich - Zürich
A38410	Berner Fachhochschule
A38800	Eidgenössische Technische Hochschule Zürich - Basel
A39760	Haute école du paysage d'ingénierie et d'architecture de Genève
A39820	Fachhochschule Nordwestschweiz
R20350	Organisation Européenne pour la Recherche Nucléaire
R20680	Centre Suisse d'Electronique et Microtechnique - Neuchâtel
R20800	Paul Scherrer Institut
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich
R22180	Eidgenössische Materialprüfungs- und Forschungsanstalt



The Netherlands

A00170	University of Twente
A12010	Vrije Universiteit Amsterdam
A12650	Radboud Universiteit Nijmegen
A14510	Rijksuniversiteit Groningen
A15420	Erasmus University Medical Center Rotterdam
A15620	Stenden Hogeschool
A15960	University of Amsterdam

A35491	Universiteit Twente
A35701	Technische Universiteit Delft
A38050	Technische Universiteit Eindhoven
R00280	Nikhef
R20370	TNO-FEL
R20430	European Space Agency - ESTEC Microelectronics
R20520	ASTRON Netherlands Foundation for Research in Astronomy
R20540	European Space Agency - ESTEC Payload Technology
R21200	Stichting imec Nederland
R21250	SRON Netherlands Institute for Space Research
R21820	Stichting INCAS3
	Tunisia
A12930	École Nationale d'ingénieurs de Sfax
A15300	École Nationale d'ingénieurs de Tunis
	Turkey
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A14250	Yeditepe Üniversitesi
A14730	TOBB Ekonomi ve Teknoloji Üniversitesi
A15260	T.C. Okan Üniversitesi
A15280	Orta Dogu Teknik Üniversitesi Kuzey Kıbrıs Kampusu
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A15680	Yıldırım Beyazıt Üniversitesi
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A12480	University of Bath
A12860	Glasgow Caledonian University
A13480	Imperial College London
A13510	Royal Holloway University of London
A13520	University College London
A13620	University of Manchester
A14030	Staffordshire University
A14580	University of Lincoln
A14760	University of Leicester
A14980	Queen Mary College of London
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A15390	The Open University
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A15790	City University London
A15850	Nottingham Trent University
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A16000	Coventry University
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A35030	Sheffield Hallam University
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A35080	University of Manchester
A35160	Heriot-Watt University
A35180	University of Nottingham
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A35470	University of Sheffield
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A36120	University of Strathclyde
A36280	Brunel University
A36341	University of Liverpool
A36342	Liverpool John Moores University
A37300	University of Birmingham
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A37400	University of Huddersfield
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A37490	Queen's University of Belfast
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A47610	National Technical University of Ukraine, Kiev Polytechnic Institute
	United Arab Emirates
A15860	Heriot-Watt University - Dubai
A16120	Abu Dhabi University

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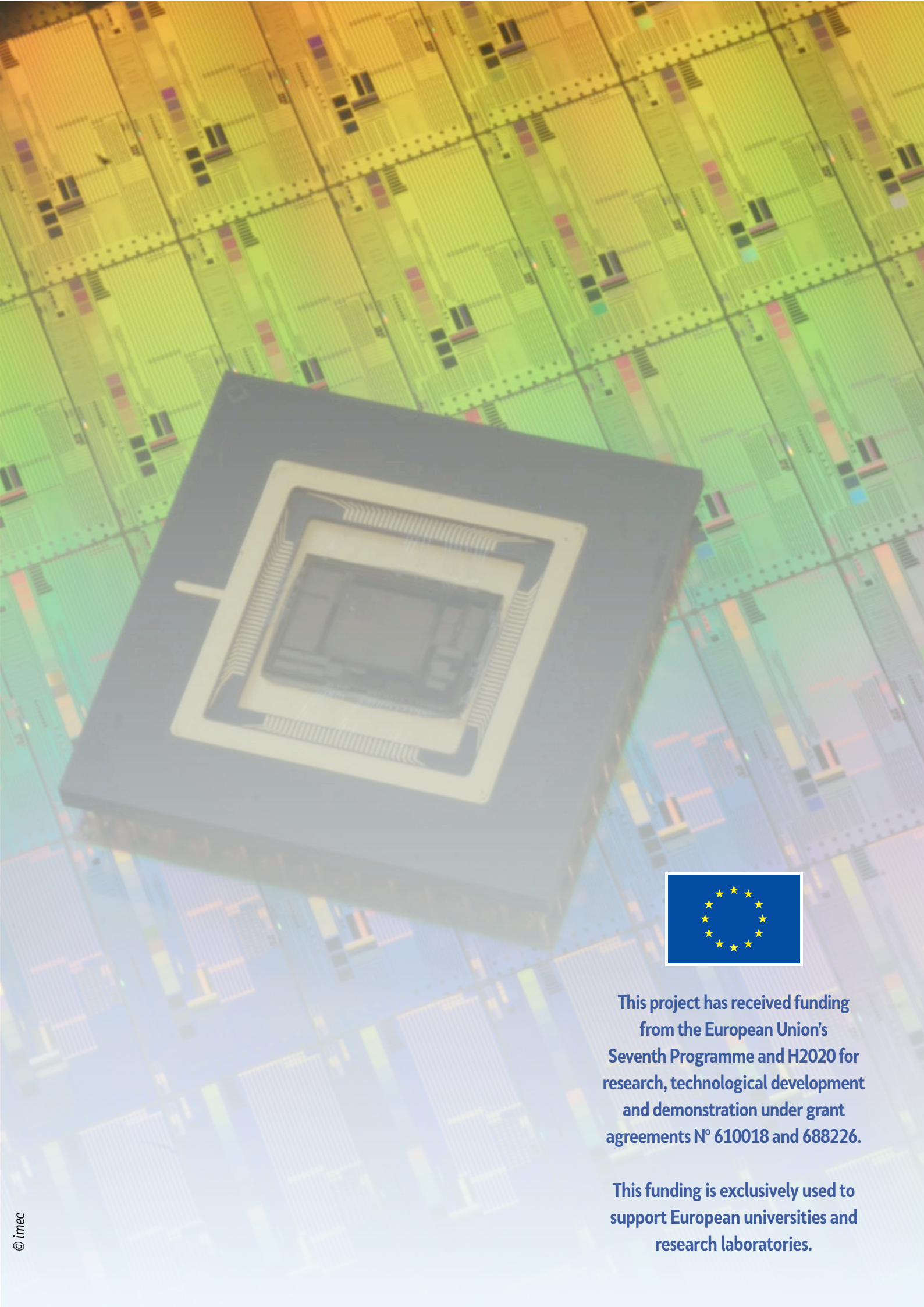
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