ASIC PACKAGE DESIGN RULES

The following rules should be respected:

1. Minimum size of a bondpad on metal level for single bonding: **62µm x 62µm**
2. Minimum size of a bondpad on metal level for double bonding: **124µm x 62µm**
3. Minimum pitch between two adjacent bondpads: **90µm**
4. Minimum distance between a corner bondpad: **120µm**

CONFIGURATION OF BONDPADS & BONDPINS

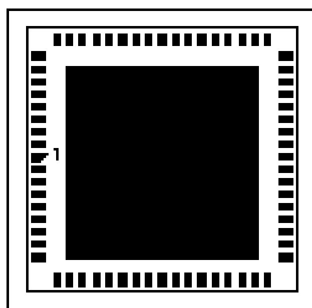
Definitions:

- **Bondpad:** Pad of the chip on which the wire will be bonded
- **Bondpin:** Areas of the package on which the wire will be bonded
- **DIL:** Dual-in-Line package
- **CLCC:** Ceramic Leadless Chip Carrier
- **JLCC:** J-Leaded Chip Carrier
- **CPGA:** Ceramic Pin Grid Array
- **CSOIC:** Ceramic Small Outline Integrated Carrier
- **OP_SOIC:** Open-Pak Small Outline Integrated Carrier
- **CQFP:** Ceramic Quad Flat Pack
- **OP_QFN:** Open-Pak Quad Flat pack No lead

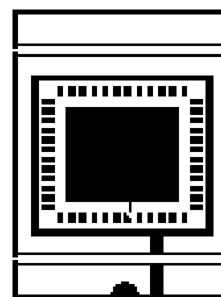
Note: Open-Pak are Pre-Molded Open-Pak (Air Cavity) Plastic Packages which have gold plated copper lead frames, exposed die pads, and meet JEDEC Outline and FootPrints. These packages are mechanically stable and have Electrical characteristics as totally encapsulated production parts.

Remarks

1. The bondpins are always distributed along the 4 sides of the cavity on which the chip will be mounted.
2. Position of bondpin #1
   In case of an odd number of bondpins on one side of the cavity (ex. 17 in case of a 68-pin chip carrier), pin #1 is in the middle of the row. In case of an even number of bondpins on one side of the frame (for ex. 48-pin DIL), pin #1 is the first pin counterclockwise from the middle of the row of pins. For the OP_QFNs, PGAs & QFPs bondpin#1 is located in the corner.
3. Bondpin #1 can be recognized by the beveled edge



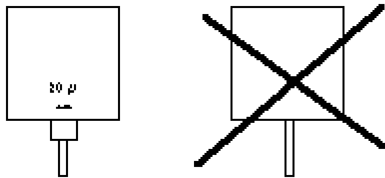
68-1d chip carrier



48-1d DIL

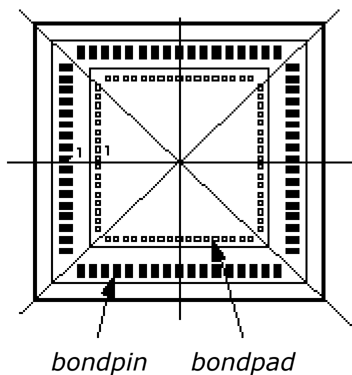
Rules

1. Bondpads have to be distributed equally along the four sides of the chip
2. Minimum ratio of length/width of the chip: 0.5
3. Max. size of the chip as designed (without scribes): (cavity size X - 900µ) x (cavity size Y - 900µ)
   The assembly house can choose the best cavity size to bond the circuit.
4. Keep the max. length of the bonding wires, from middle bondpad to middle bondpin as small as possible (normally 3 mm for industrial purpose). This rule may be ignored for prototyping ceramics.
5. Do not use minimum metal width for connection to the bondpad. Use 20µ width at least.



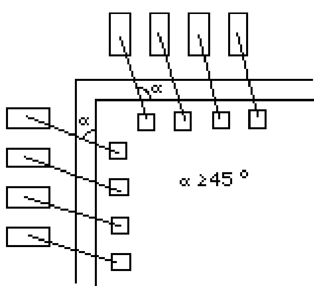
6. To determine the right position of the bondpads, it is advised to draw the chip together with the bondpins of the package. The chip has to be partitioned in equal segments (4 or 8). Bondpads and bondpins have to be located in the same segment

68-1d chip carrier



bondpin *bondpad*

7. Bondpad #1 has to be identified by means of the number 1 near the bondpad (size 50 microns).
8. Bondpad #1 has to be the middle one of the bondpads, except for OP_QFNs, PGAs and QFPs. Bondpads are numbered counter clockwise. <u>Bondpin#1 is not connected to the frame</u>. Chips are allways attached to the frame by <u>conductive die attach</u>. If the designer wants to have an extra connection from VSS (most negative voltage) to the substrate via the cavity, an extra bondwire has to be provided from the VSS bondpin to the cavity of the frame.
9. It is preferable to draw bondpads that do not have to be bonded in the form of an octagon.
10. Crossing of bonding wires is not allowed.
11. The angle between the edge of the die and the bondwire has to be minimum 45 degrees.



Generating a bonding scheme

It is preferable that the designer makes a clear bonding scheme. To generate a bonding scheme, follow the next steps:

- Convert the GDS file containing available packages within EUROPRACTICE.
  For cadence users there is also a "gds-number to layername conversion table" available:
  - ep_pack.layertable
  - EP_PACKAGES_08022018.gds.gz

  After you have read in this GDS file, you will have a library with a total of 37 different types of packages which can be used for all the available technologies.

- Create a **_PACK.**
- Add to this cell the desired package-cell (always use the _A4 or _A3 version!) and put your design in the middle of the package cavity (you may rotate your design if necessary).
- You can now connect the bondpads of the circuit to the bondpins of the package using a path of 30 micron wide (more or less). Use one of the available METAL layers to draw the connections.
- Fill in the necessary design information (lower (A4) or right (A3) side)
  - **Comments:** Fill in any comment you want to specify. (e.g. I/O -pads not to be connected).
  - **Lid: Taped [ ] Sealed [ ] Glued [ ] Glass [ ]** (mark with X)
  - **Qty Samples** (fill in the number of samples to be PACKAGED)
- Generate a GDS - file of your whole design library.
- Transfer the design data to imec.

Notes

Do not worry about warnings concerning the y* layers that are not translated to GDS format. Imec will fetch the necessary package cell from their own library. Only make sure that the wires and text are on a translated layer (ex. METAL)

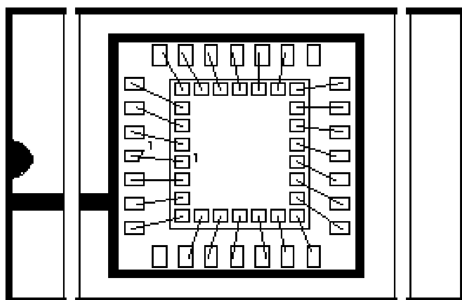
Note 2

If you have any questions, please check the cell in the gds-file called EXAMPLE_PACK.

IMPORTANT:

All the packages in this library have isolated cavities (This means that there is no prefabricated connection between the cavity and one of the package pins). The die is attached to the cavity with conductive glue. If you want to connect the lowest or most negative potential (VSS) to the backside of the die to achieve a better substrate contact, you may add a bond wire from the package pin to the cavity (see also EXAMPLE_PACK: pin nr. 1 & 5 in EP_PACKAGES_08022018.gds.gz).

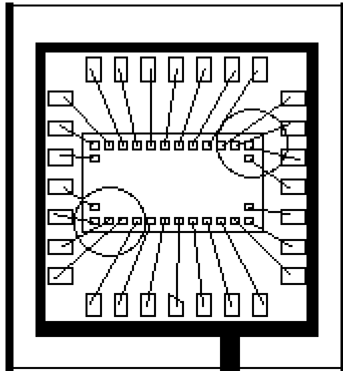
Example of good bonding diagram



Example of good bonding diagram of 26 pins chip in 28-1d DIL

Example of wrong chip design, causing bonding problems

A chip with 28 I/O pins has to be mounted in a 28-pin DIL. The shape of the chip is not designed with a minimum ratio of 0.5. It is not possible to do a correct bonding. Problems occur in the corners where the bonding wires are coming too close to each other.



Example of wrong bonding.
See problems in the circled areas.
The angles are not 45 degrees.

Note 3

For prototype assembly, we have to see the bonding diagram case by case to examine feasibility.