2019 *mini@sic* Europractice MPW runs Schedule and Prices

EUROPRACTICE IC SERVICE

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mini@sic

Through the *mini***@sic** program the EUROPRACTICE IC Service is offering special MPW prototyping conditions to stimulate Academia and publicly funded Research Institutes to prototype small ASIC designs for education or publicly funded research. Through Multi Project Wafer Services, the high cost of a prototype run (masks and wafers) is shared amongst several customers. However, for student education or PhD research programs the minimum prototyping charges are still too high. By introducing the *mini***@sic** concept on MPW runs EUROPRACTICE is offering considerably lower minimum prototyping charges for small ASIC designs. **Academia and Research Institutes will have the possibility to prototype small designs at low prices on selected MPW runs.**

ON Semiconductor	J	F	M	A	M	J	J	A	S	O	N	D
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	14		25			3		12		28		
ON Semi 0.7µ C07M-I2T100 100 V - 2M & 3M options	14		25			3		12		28		
ON Semi 0.35µ C035U 4M (3M & 5M optional) only thick top metal	28			15			1		16			2
ON Semi 0.35µ C035 - I3T25U 3.3/25 V 4M (3M & 5M optional) only thick top metal	28			15		2			16			2
ON Semi 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)	2			1			8			7		
ON Semi 0.35µ C035 - I3T50U (E) 50 V 4M - 3M optional (5M on special request)			4		27				2			2

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 3 weeks in advance.

IHP	J	F	M	A	M	J	J	A	S	O	N	D
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics				12						18		
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)					24							
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV		22				14		30				
IHP SG13C SiGe:C CMOS 7M/MIM		22				14		30				
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV		22				14		30				
IHP SG13G2Cu FEOL process SG13G2 together with Cu BEOL option										28		
IHP SG13SCu FEOL process SG13S together with Cu BEOL option										28		
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE			8									

Important Note:

- Dates are registration deadlines. DRC clean GDSII file must be submitted within 10 days after this date.
- Bumping available for all IHP technologies with extra charge, limited to 200 bumps.
- IHP SG25H4 MPW runs available on request for existing projects only. (Contact: virtual-asic@iis.fraunhofer.de for additional information).

X-FAB	J	F	M	A	M	J	J	A	S	O	N	D
XH018 0.18µ HV NVM CMOS E-FLASH				23						24		
XT018 0.18µ HV SOI CMOS			15								1	

options regular runs	Process modules included for 6 metal option
XH018 0.18µ HV NVM CMOS E-FLASH	LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO
XT018 0.18µ HV SOI CMOS	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, MET4, METMID, METTHK, HWC

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 2 weeks in advance.

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	23				29				11			
TSMC 0.18 CMOS High Voltage BCD GenII				9						23		
TSMC 65nm CMOS Low Power MS RF (reserve 4 months in advance)		13			15			21			20	
TSMC 40nm CMOS Low Power MS RF				24						2		
TSMC 28nm CMOS HPC RF (reserve 4 months in advance)			27							23		
TSMC 28nm CMOS HPC RF – Micro-block (reserve 4 months in advance)			27							23		

Important notes:

- Dates are <u>GDS submission</u> deadlines. The design registration has to be done at least 4 weeks in advance unless otherwise specified in above table.
- Contact eptsmc@imec.be if any of the following options are used: MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS
- Read below for 28 nm Micro-block conditions

options TSMC mini@sic runs	IO	MIM /um2	special remarks
TSMC 0.18μ CMOS MS/RF	3.3 V	2 fF	Metalscheme: 1P6M_4X1U with UTM (20kA) topmetal
TSMC 0.18 CMOS High Voltage BCD Gen 2 0.18 UM CMOS High Voltage Mixed Signal based General Purpose BCD Dual Gate FSG AL 1P6M [SALICIDE, NBL/PBL EPI, 1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5VV]		2 fF between M5 & M6	Metalscheme: 1P6M_4X1U with UTM (30kA) topmetal
TSMC 65nm CMOS LP MS RF	2.5V (1.8UD, 3.3OD)	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1Z1U_RDL Default : wirebond <u>with</u> 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 40nm CMOS LP MS RF – **No Triple Gate oxide**	2.5V (1.8UD, 3.3OD)	-	Core : 1.1 V, Metal scheme : 1P8M_5X2Z_RDL Default : wirebond <u>with</u> 14kA thick RDL. AP layer mandatory in bondpads.
TSMC 28nm CMOS HPC – High Performance Compact Mobile Computing, RF – also applies for Micro-block	1.8 V	-	Core : 0.9 V, Metal scheme : 1P8M_5X1Z1U UTRDL (28kA thick AP layer) Default: BEOL option 1, 11 mils backlapping

UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L65N Logic/Mixed-Mode/RF - LL		25					15				11	
UMC L130 Mixed-Mode/RF		11				17				28		
UMC L180 Mixed-Mode/RF	28			22			22		30			

options UMC mini@sic runs	Core	IO	MIM	topmetal	special remarks
UMC L65N Logic/Mixed-Mode-MODE65N/RF - LL - 1P8M1T0F1U - 1.2V/2.5V	1.2	2.5V/2.5V_OD3.3V	2fF	32.5kA	Metal-stack "26"
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	1.2V	3.3V	1fF	20kA	Possible combinations: HS, HS-LL (No SP possible)
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	1.8V	3.3V	1fF	20kA	

Important note: Dates are <u>GDS submission</u> deadlines. The design registration has to be done at least 3 weeks in advance.

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 130nm BCDlite			11						9			
GLOBALFOUNDRIES 55 nm LPe		11						12				
GLOBALFOUNDRIES 22 nm FDSOI			4						2			

Important Note:

- Dates are <u>registration</u> deadlines after which designs cannot enter this MPW run anymore. Final GDSII file must be submitted within 6 weeks after this date.
- We reserve the right to cancel mini@sic runs if the run is not economically feasible.
- Mini@sic participation possible only with mandatory metal stack.

* Dates in red are preliminary.

2019 *mini*@sic Europractice MPW runs – Pricelist

Accessible for universities, research institutes and companies
Prices and conditions may change at any time without prior notice
Prices valid for runs starting 1 January 2019.

STANDARD price applies to all non-European (not belonging to the countries of EUROPEAN price) universities and research institutes who submit designs for **educational or publicly funded research use only.**

DISCOUNTED price: only applies to EUROPRACTICE registered (who paid their annual full membership fee) Academic and Research Members from all 28 EU countries and Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine who submit designs for **educational or publicly funded research use only.**

Prices are given for the delivery of unpackaged, untested prototypes. Encapsulation and testing will be charged separately.

Number of prototypes
OnSemi > 20 samples
UMC : 0.18um, 0.13um : 25 samples
UMC : 65nm: 50 samples
IHP : 40 samples SG25 & SG13, 25 samples using TSV module, PIC, EPIC
XFAB : 50 samples
TSMC : 40 samples for 0.18u, 100 samples for 65, 28nm
GLOBALFOUNDRIES : 25 samples
If you need more prototype samples, please ask for a quotation

Plots
You can order plots/PDF of your designs
- first plot/PDF costs 50 euro
- next plots cost 20 euro each

Packaging : see separate prices and available packages

ALL PRICES IN EURO

ON Semiconductor (formerly AMIS)	STANDARD Price/mm²	DISCOUNTED Price/mm²
ON Semi 0.7µ C07M-D 2M/1P	300 [1]	270 [1]
ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	350 [1]	315 [1]
ON Semi 0.7µ C07M-I2T100 100 V - 2M	525 [1]	485 [1]
ON Semi 0.7µ C07M-I2T100 100 V - 3M	560 [1]	525 [1]
ON Semi 0.35µ C035U 4M (default) including analog options	720 [1]	670 [1]
ON Semi 0.35µ C035U 3M (optional) including analog options	700 [1]	650 [1]
ON Semi 0.35µ C035U 5M (optional) including analog options	800 [1]	750 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 3M	850 [1]	800 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 4M	925 [1]	875 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 5M	1050 [1]	995 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 3M	850 [1]	800 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 4M	925 [1]	875 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 5M	1050 [1]	995 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 3M (optional)	750 [1]	700 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 4M (default)	770 [1]	720 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 5M (optional)	800 [1]	750 [1]

IHP	STANDARD Price/mm²	DISCOUNTED Price/mm²
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	2125 [2]	2000 [2, 3]
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	3230 [2]	3040 [2, 3]
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics	6800 [2]	4620 [2, 3,14]
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)	3230 [2]	2660 [2, 3]
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV	5355 [2]	4410 [2, 3]
IHP SG13C SiGe:C CMOS 7M/MIM	3825 [2]	3600 [2, 3]
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV	6205 [2]	5110 [2, 3]
IHP SG13G2Cu FEOL process SG13G2 together with Cu BEOL option	5950[2]	5000[2, 3]
IHP SG13SCu FEOL process SG13S together with Cu BEOL option	5185[2]	4360[2, 3]
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV	850 [2]	800 [2, 3]
IHP SPECIAL SERVICES		
bumping (available for all IHP technologies)	One-off fee 6500 [7]	One-off fee 4700 [7, 3]
localized back side etching (available for all IHP technologies) not offered for EPIC/PIC runs	One-off fee 4250 [7]	One-off fee 2500 [7, 3]
TSV to ground (SG25H4/SG13S)	One-off fee 4250 [7]	One-off fee 2500 [7, 3]

X-FAB	STANDARD Price/block	DISCOUNTED Price/block
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, MET4, METMID, METTHK)	4065 [4]	3750 [4]
X-FAB XT018 0.18µ HV SOI CMOS (MET3, MET4, METMID, METTHK)	4145 [4]	3825 [4]

TSMC	STANDARD Price/block	DISCOUNTED Price/block
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	3610 [9]	3140 [9]
TSMC 0.18 CMOS High Voltage BCD Gen 2	5090 [16]	4470 [16]
TSMC 65nm CMOS LP MS RF	12890 [10]	12130 [10]
TSMC 40nm CMOS LP MS RF	17320 [8]	16300 [8]
TSMC 28nm CMOS HPC RF	19960 [15]	17510 [15]
TSMC 28nm CMOS HPC RF – Micro-block	11805 [17]	9600 [17]

UMC	STANDARD Price/block	DISCOUNTED Price/block
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V	3070 [5]	2570 [5]
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V	5020 [5]	4460 [5]
UMC L65N Logic/Mixed-Mode LL	9720 [6]	9140 [6]

GLOBALFOUNDRIES	STANDARD Price: see notes	DISCOUNTED Price: see notes
GLOBALFOUNDRIES 130 nm BCDlite	5900 [11]	4900 [11]
GLOBALFOUNDRIES 55 nm LPe	11900 [12]	9900 [12]
GLOBALFOUNDRIES 22 nm FDSOI	29900 [13]	24900 [13]

Notes

1) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 4 mm^2
2) Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 0.8 mm^2
3) These discount prices are only available for the **28 EU countries**
4) Price = per block of 1520x1520 microns needed to fit the design in. Adding two blocks together to one block is possible.
5) Price = per block of 1525x1525 microns needed to fit the design in. Adding two blocks together to one block is possible.
6) Price = per block of 1875x1875 microns needed to fit the design in. Adding two blocks together to one block is possible.
7) Price = per submitted design. For bumping (no size limit, limited to 200 bumps) final wafer thickness for TSV is 75um.
8) Price = per block of 1920x1920 microns (designed area – pre-shrink) needed to fit the design in, (on silicon area – after shrink = 1730x1730 microns) – see below
9) Price = per block of 1660x1660 microns needed to fit the design in
10) Price = per block of 2000x2000 microns needed to fit the design in
11) Price = per block of 1750x1750 microns needed to fit the design in. Adding two blocks together to one block is possible. The mentioned die size is referred to the Pre-Shrink die size
12) Price = per block of 1500x1500 microns needed to fit the design in. Adding two blocks together to one block is possible. The mentioned die size is referred to the Pre-Shrink die size.
13) Price = per block of 1250x1250 microns needed to fit the design in. Adding two blocks together to one block is possible. The mentioned die size is referred to the Pre-Shrink die size.
14) Special introductory price
15) Price = per block of 1570x1570 microns (designed area – pre-shrink) needed to fit the design in, (on silicon area – after shrink = 1413x1413 microns) – see below
16) Price = per block of 2500x2500 microns needed to fit the design in.
17) *Micro-block rules, applicable for TSMC 28nm*:
The Micro-block size is 1110 x 1110 microns (designed area – pre-shrink). On silicon area is 1000 x 1000 microns.
In case the design is larger than the Micro-block size, only option is a miniasic block.
Multiple Micro-blocks are possible on one run.
Micro-block and miniasic reservations/registrations should be done no later than 4 months before the deadline.
Withdrawal of the Micro-block or miniasic block later than one week before the deadline will be subject to a penalty of 50% of the amount due. (*)
In case of Micro-block, there is no commitment that the run will be launched in case of insufficient participations. (**)
In case of miniasic, there is always commitment that the run will be launched.
Combining miniasic and Micro-block on one run is allowed.
(*) *The amount can be recovered at the next participation. In case of 2 subsequent late withdrawals the fee cannot be recovered anymore.(**) A graphical picture of the run status will be available per request. An online tool is in preparation and soon online.*

UMC 0.18 and 0.13µ mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1525 x 1525 µm
- 2 sub-blocks : design may not be larger than 3240 x 1525 µm
- 3 sub-blocks : design may not be larger than 4960 x 1525 µm
- 4 sub-blocks : design may not be larger than 3240 x 3240 µm
- 6 sub-blocks : design may not be larger than 4960 x 3240 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

UMC 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1875 x 1875 µm
- 2 sub-blocks : design may not be larger than 3950 x 1875 µm

TSMC 65nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2000 x 2000 µm
- 2 sub-blocks : design may not be larger than 4000 x 2000 µm

TSMC 40nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1920 x 1920 µm (pre-shrink)
- 2 sub-blocks : design may not be larger than 3840 x 1920 µm
- These are designed dimensions. Fabricated designs (40nm) are shrinked during maskmaking in both X and Y directions by 0.9

TSMC 28nm mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1570 x 1570 µm (pre-shrink)
- 2 sub-blocks : design may not be larger than 3140 x 1570 µm
- These are designed dimensions. Fabricated designs (28nm) are shrinked during maskmaking in both X and Y directions by 0.9
- Micro-blocks

TSMC 0.18µ CMOS mini@sic rules

In this case however the standard block of 5x5 mm is subdivided into 9 regular square sub-blocks. Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 1660 x 1660 µm
- 2 sub-blocks : design may not be larger than 3320 x 1660 µm
- 3 sub-blocks : design may not be larger than 4980 x 1660 µm
- 4 sub-blocks : design may not be larger than 3320 x 3320 µm
- 6 sub-blocks : design may not be larger than 4980 x 3320 µm

TSMC 0.18µ HV BCD mini@sic rules

Users under the *mini***@sic** program can submit single or multiple of sub-blocks depending on the size of their design.

- single sub-block : design may not be larger than 2500 x 2500 µm
- 2 sub-blocks : design may not be larger than 5000 x 2500 µm

The price for prototyping is the number of sub-blocks your design needs to fit in, multiplied with the sub-block price.

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