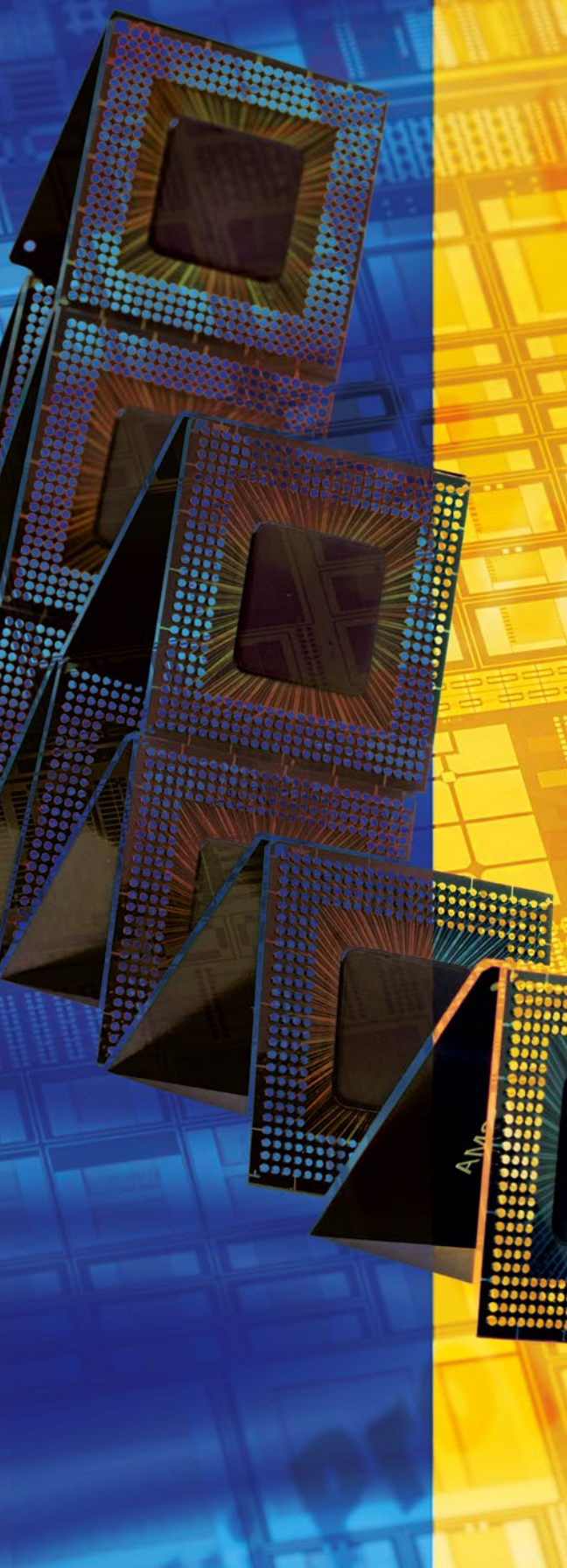
EUROPRACTICE
IC SERVICE

ACTIVITY REPORT 2015



EUROPRACTICE
IC SERVICE

EUROPRACTICE IC SERVICE

THE RIGHT COCKTAIL OF ASIC SERVICES

EUROPRACTICE IC SERVICE OFFERS YOU A PROVEN ROUTE TO ASICS THAT FEATURES:

- Low-cost ASIC prototyping
- Flexible access to silicon capacity for small and medium volume production quantities
- Partnerships with leading world-class foundries, assembly and testhouses
- Wide choice of IC technologies
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- RTL-to-Layout service for deep-submicron technologies
- Front-end ASIC design through Alliance Partners

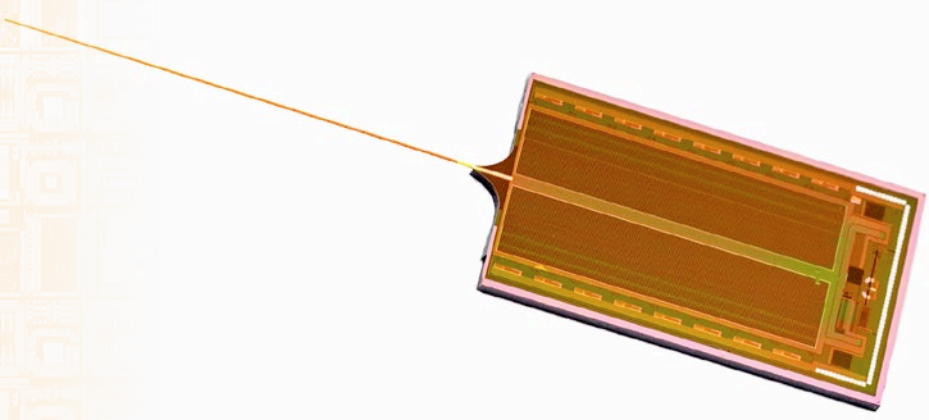
Industry is rapidly discovering the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who don't need always the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise that includes IC manufacturing, packaging and test. This you can get all from EUROPRACTICE IC service, a service that is already established for 20 years in the market.

THE EUROPRACTICE IC SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:

- imec, Leuven (Belgium)
- Fraunhofer-Institut fuer Integrierte Schaltungen (Fraunhofer IIS), Erlangen (Germany)

This project has received funding from the European Union's Seventh Programme for research, technological development and demonstration under grant agreement N° 610018.

This funding is exclusively used to support European universities and research laboratories.



FOREWORD

Dear EUROPRACTICE customers,

We are at the start of the "Internet of Things (IoT) Revolution", a new era in which "things" in the physical world, machines, cars, homes, wearables, ... will become "connected". "Things" will be able to sense information and communicate that to other smart things to generate real-time actions by humans or machines.
IoT is already happening today in the consumer space, as wearables, connected cars and health-tracking devices. There is a huge opportunity for European Small and Medium Enterprises (SMEs) to innovate and develop new products (hardware as well as software) as the potential IoT markets are relatively smaller and fragmented, the ideal playground of European SMEs.

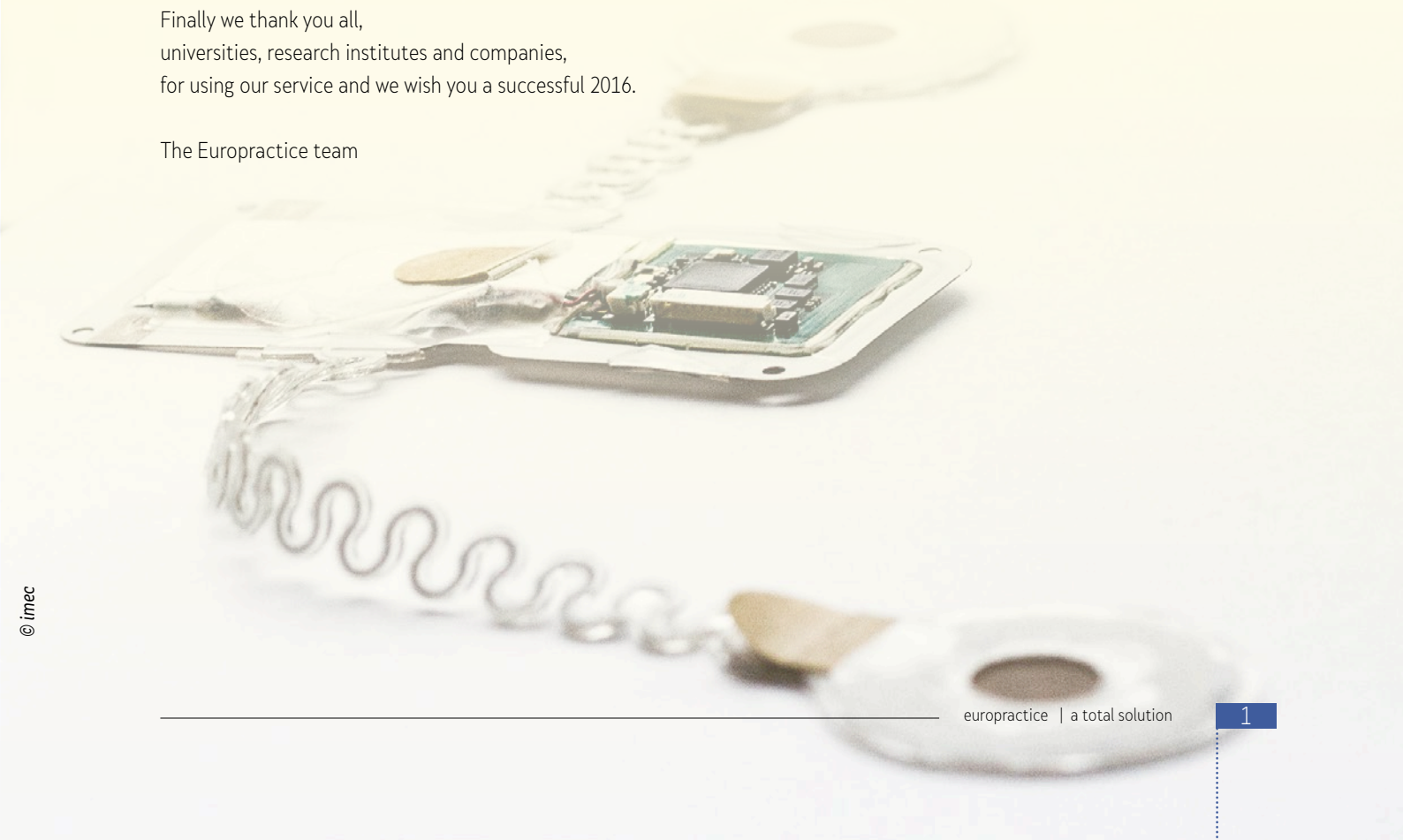
Of course the development of new IoT products needs design of new ASICs which needs good IC designers. Here the EUROPRACTICE service plays an important role towards the European universities by offering them affordable and well-supported access to EDA tools for IC design and to IC technologies for prototyping so that they can train students and do innovative research through their PhD programs. In addition the universities and research institutes can benefit from the EUROPRACTICE offered training courses on IC design flows.

In order to stimulate European universities to design a first IC in standard 0.18µ technology or to start a first IC in an advanced (90nm and below) technology, we have been able to launch a call for first-user applications in December 2015. From the 46 submitted applications, 20 first-user applications (10 in each category) have been selected early January 2016 by an independent committee for free or highly-reduced prototype fabrication (funded by the "EUROPRACTICE 2013" EC-funded project). A very successful stimulation action.

We thank the European Commission (DG Connect) for their continuous support. Although the current "EUROPRACTICE 2013" project will end on 30 September 2016, we signed last year with the EC the contract for the "EUROPRACTICE 2016" project that will run until 30 June 2018. As such our commitment to continue the EUROPRACTICE service towards the ~650 European universities is secured.

Finally we thank you all,
universities, research institutes and companies,
for using our service and we wish you a successful 2016.

The Europractice team



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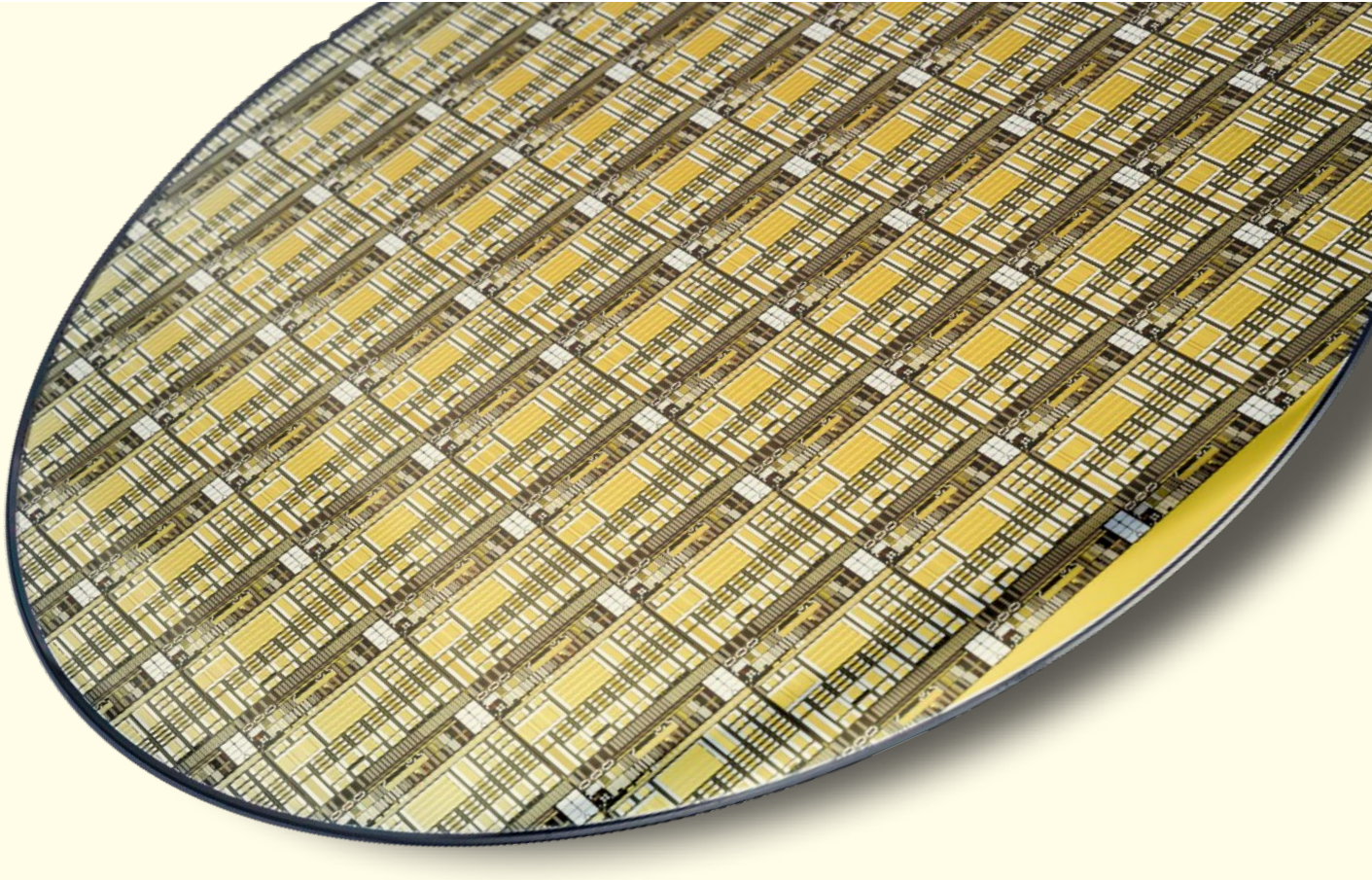

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EUROPRACTICE:
YOUR TOTAL AND TURN-KEY ASIC SOLUTION

EUROPRACTICE provides semiconductor and system companies with a total and turn-key ASIC solution including :

- easy access to foundry design rules, cell libraries and design kits
- deep submicron RTL-to-layout service
- low cost prototype fabrication service
- volume fabrication service including wafer fabrication, packaging and test
- ASIC qualification
- logistics
- technical customer support

New fables startup companies as well as small companies or companies having small ASIC volume products in niche markets experience huge problems to get access to foundries since their volume is too small.

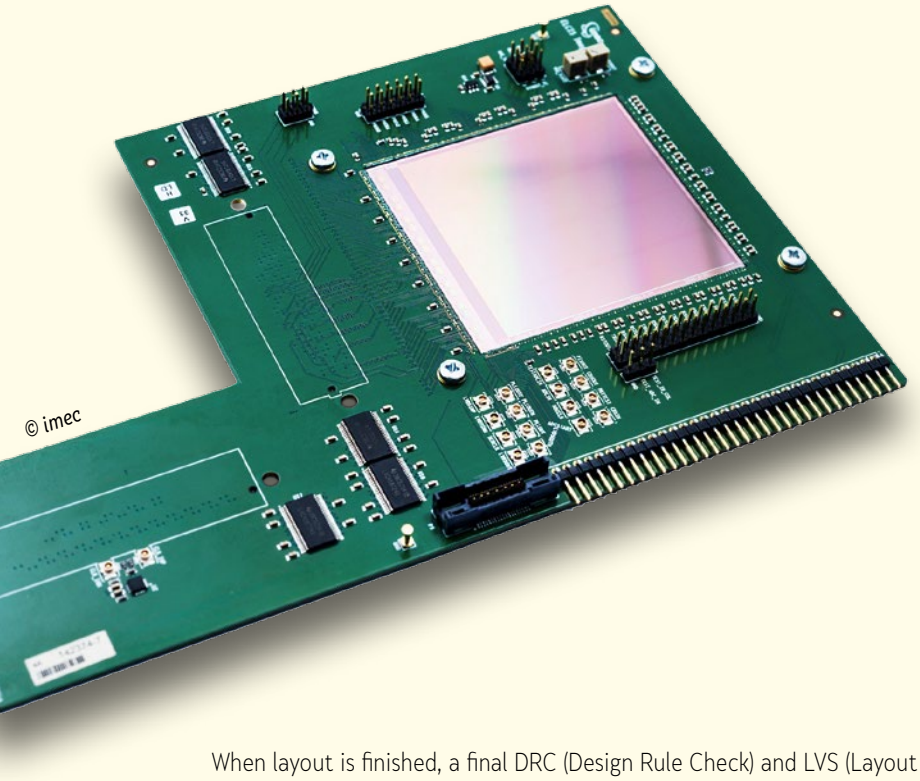
EUROPRACTICE has wafer foundry agreements with different leading suppliers, allowing to offer the most advanced as well as specific technologies to those customers. Our foundry partners acknowledge the EUROPRACTICE Service as the optimal solution to provide wafer capacity to smaller customers. Suppliers see EUROPRACTICE as one big customer representing about 650 universities, research centers and 300 companies world-wide. Through agreements with foundry partners, EUROPRACTICE is able to offer ASIC solutions ranging from a few wafers to thousands of wafers per year.

EASY ACCESS

Through its agreement with foundries and library partners, EUROPRACTICE is allowed to distribute foundry technology information and cell libraries upon simple signature of a standard Non-Disclosure Agreements or a Design Kit License Agreement. Those agreements can be downloaded from the EUROPRACTICE website. In this way you have access in a few days without having to go through a painful customer qualification procedure at the foundry. Foundry information includes design rules, spice parameters, design & layout manuals and DRC/ERC/LVS decks. Cell library information includes library manuals and design kits for most of the popular CAD tools (Cadence, Synopsys, Mentor Graphics, Tanner, etc.). This foundry and library information is distributed through our download servers.

ASIC DESIGN

When customers have received design rules, cell libraries, etc., they can start the ASIC design. ASIC design can be split up into front-end design and back-end design. Front-end design covers ASIC specification feasibility study and design including tasks such as schematic entry, VHDL description, scan insertion, simulation and synthesis. The front-end design can be carried out by the customer himself or can be subcontracted to a design house. During this design phase, Europractice offers technical support on technology, test, type of package, etc. Important know-how and feedback from the test house will be used to improve the DFT (Design For Testability). "State-of-the-art" CAD tools are used during the ASIC design phase.
When the netlist is ready the backend design activity starts including layout generation using state-of-the art layout tools. Deep submicron digital place & route tasks are in most cases not performed by the customers. For those customers that have not their own layout tools, EUROPRACTICE is offering such deep submicron layout service (see deep submicron layout service on page 7). After initial layout, timing verification is carried out by the customer using parasitic layout information and layout is iterated until timing is met. Verification of the design needs to be done in all technology corners.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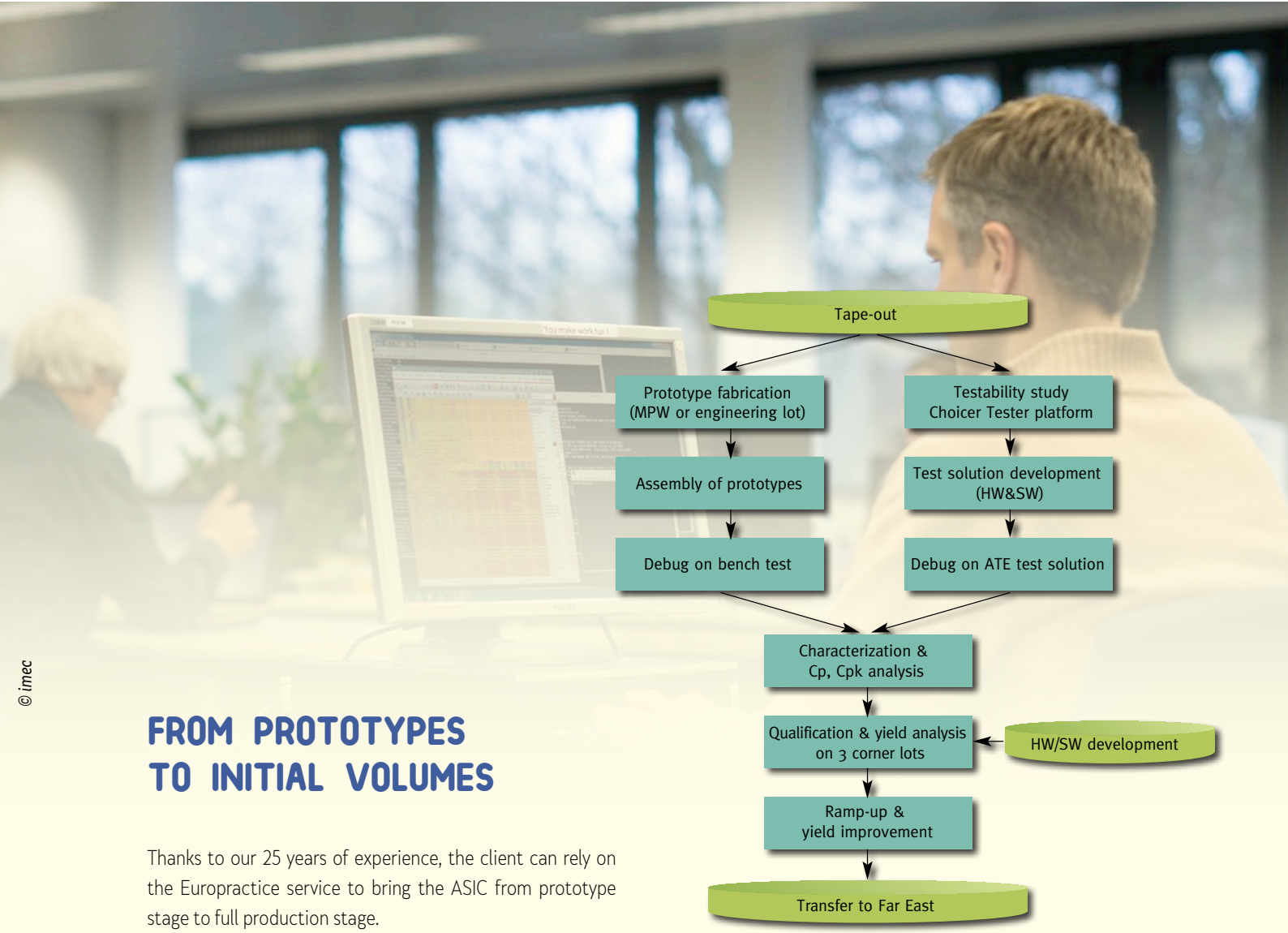
When layout is finished, a final DRC (Design Rule Check) and LVS (Layout versus Schematic) is performed on the GDS-II database in order to deliver a correct GDS-II to the foundry for manufacturing.

BACKEND OPERATION SERVICES THROUGH COOPERATION WITH CERTIFIED PARTNERS

A history of more than 25 years offering programs to microelectronics industry and academia endorse Europractice as the key partner to your ASIC's success. We embrace COT and turnkey business models to adapt to your requirements with a maximum level of transparency and flexibility. Side by side with world class partners and our long term agreements, Europractice boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.
Through these collaborative agreements our customers can benefit of working with highly recognized chip industry players. The most relevant companies involved in our semiconductor supply chain are listed below:

- **Foundry partners:**
  TSMC, UMC, ON Semi, ams, IHP, XFAB, GLOBALFOUNDRIES, memscap, imec, LETI
- **Ceramic assembly partners:**
  HCM, Systrel, Optocap, Kyocera
- **Plastic assembly partners:**
  ASE, Kyocera
- **Wafer bumping partner:**
  Pactech, ASE
- **Test partners:**
  ASE, Microtest, Delta, Rood Technology and Blue test
- **Failure analysis:**
  Maser Engineering
- **Library partners:**
  Faraday, ARM



FROM PROTOTYPES TO INITIAL VOLUMES

Thanks to our 25 years of experience, the client can rely on the Europractice service to bring the ASIC from prototype stage to full production stage.

PROTOTYPE FABRICATION

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. Europractice will produce the first prototypes for the customer and organize the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program.

The devices can be tested on both wafer level as well on packaged devices. The goal is to reduce the test time and to test the ASIC for manufacturing problems using the ATPG and functional patterns.

Europractice will support you during the development of single site test solution as well as with a multi-site test solution when high volume testing is required. Based on the test strategy followed diverse type of implementations can be realized.

DEBUG AND CHARACTERIZATION

Before going into production a characterization test program will check if all the ASIC specifications are met according to the customer expectations. Threshold values are defined for each tested parameter. The software will test all different IP blocks and the results will be verified with the bench test results.

A characterization at Low (LT), Room (RT) and High (HT) temperature will be performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be strong against process variations, the product qualification can start. Europractice can support you through the full qualification process using different kind of qualification flows ranging from Consumer, Industrial, Medical to Space according to the Military, Jedec and ESCC standards....

In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

Lot Acceptance tests

- Pre-cap inspection
- Destructive Physical Analysis (DPA)
- Electrical screening
- External and Internal visual inspection
- Cross sectioning: SEM
- Radiation tests (Tid, SEE)

Mechanical Acceptance tests

- Bond pull, Die shear
- Solderability
- Gross & Fine leakage tests
- PIND
- Marking resistance
- Mechanical shock
- Constant acceleration
- Vibration tests

Environmental tests

- Pre-conditioning
- TCT
- HTS
- HAST
- Autoclave, unbiased

Qualification tests

- Static or dynamic burn-in
- Operating life tests (HTOL)
- ESD & LU tests

Failure Analysis

- Non-destructive analysis: X-ray, SAM
- Electrical Failure analysis: Photo Emission Microscopy, probing, OBIRCH
- Physical analysis: SEM, TEM, FIB

FROM INITIAL VOLUMES TO FULL PRODUCTION

SUPPLY CHAIN MANAGEMENT

Europractice is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.

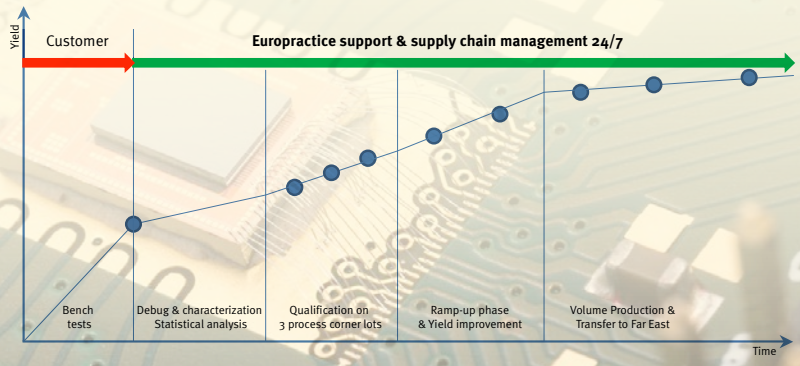
Customer products are treated internally as projects and followed closely by the imec engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. Europratice therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

YIELD IMPROVEMENT

Europractice can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the qualification of the device on 3 different corner lots, Europractice can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers will be analyzed to check for yield issues related to assembly or wafer production. Europractice is using the well proven tool Examinator™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.

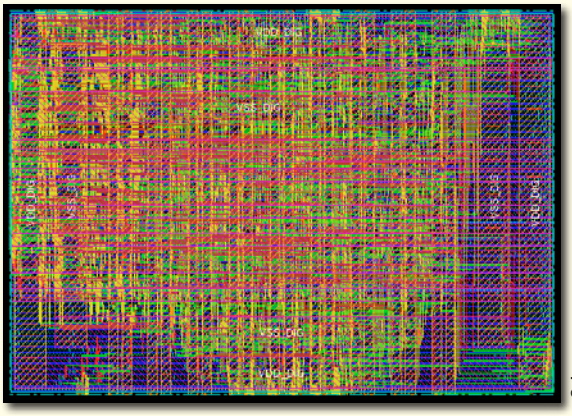
FROM PROTYPE TO PRODUCTION KEEPING COST UNDER CONTROL

Europractice supports you from production ramp up till volume production taking into account global project costs. In cases of certain high volume in test is achieved, we are able to transfer the production test solution to Far East. The replicated test solutions are developed in close relationship with the Far East test houses to be fully compliant with their tester platforms.



EUROPRACTICE OFFERS DEEP SUBMICRON DESIGN SUPPORT SERVICE

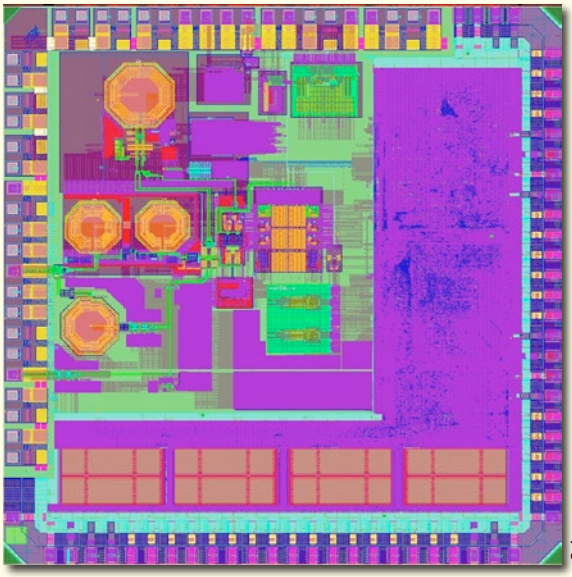
Synthesis and layout of deep submicron chips is not straightforward. You need a highly trained team of engineers equipped with expensive state-of-the art EDA tools to tape out first time right Silicon. The chips are growing in size while the technology dimensions are getting smaller and power specifications are becoming more stringent. Because of this, chip designers have to understand how to tackle issues like: hierarchical layout, clock skew, latencies of interacting clock domains, static and dynamic IR-drop on the power distribution, electro-migration and signal integrity, handling many metal layers in the back-end, incorporating IP blocks in the design, on-chip variation, design for packaging, design for manufacturing... And the list goes on.



Digital block for the analog Tx part of a mixed-signal chip in 28nm TSMC.

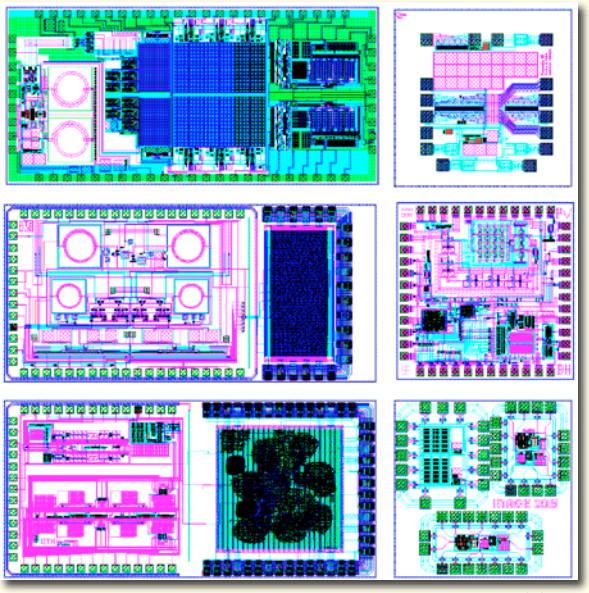
Supporting high-level system designers on the road to tapeout, EUROPRACTICE IC Service provides a physical design support service starting from RTL code in VHDL or Verilog or from a synthesized netlist.

The service supports the whole back-end design flow including synthesis, floorplanning, deep-submicron place and route and multi-mode multi-corner optimization, timing analysis, extraction, scan and BIST insertion and ATPG, tape-out preparation, etc. The service is equipped with state-of-the art tools from the major EDA vendors and has already supported technologies from many different foundries down to 16nm.



imec research mixed-signal low power design in 28nm TSMC technology.

Many circuits were successfully taped out for in-house developed Systems-On-a-Chip as well as for ASICs developed by companies, design houses, research institutes and universities. These circuits included a.o. analog full custom blocks, memory macro's from different vendors, special I/O cells and RTL level (soft and firm) IP. The team is well versed in low-power techniques as well as the state-of-the art power format descriptions (CPF/UPF). Interrelated gated clock domains, power shut-off, multi supply-voltage and backbiasing have been successfully implemented.



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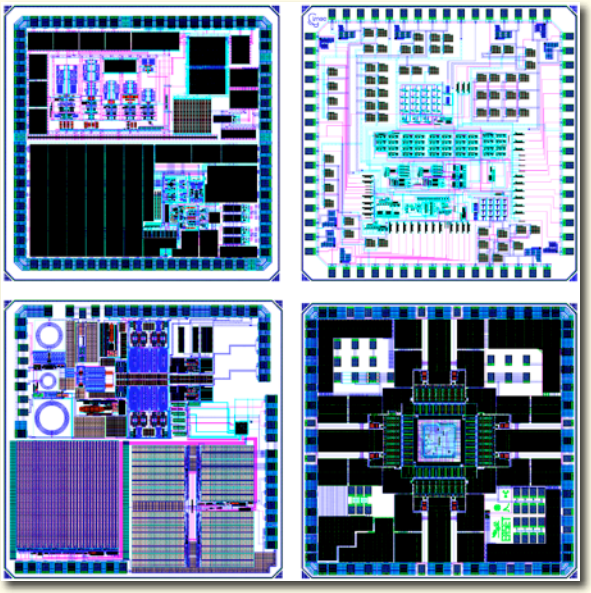

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LOW COST IC PROTOTYPING

The cost of producing a new ASIC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. This is largely due to the NRE (Non-Recurring Engineering) overheads associated with design, manufacturing and test.

EUROPRACTICE has reduced the NRE, especially for ASIC prototyping, by two techniques:

(i) Multi Project Wafer Runs or
(ii) Multi Level Masks.

MULTI PROJECT WAFER RUNS

By combining several designs from different customers onto one mask set and prototype run, known as Multi Project Wafer (MPW) runs, the high NRE costs of a mask set is shared among the participating customers. Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full prototyping wafer run. A limited number of tested or untested ASIC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time".

In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service. EUROPRACTICE is organising about 200 MPW runs per year in various technologies.

MULTI LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi Level Mask (MLM). With this technique the available mask area (20 mm x 20 mm field) is typically divided in four quadrants (4L/R : four layer per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is thus reduced by a factor of four. By adapting the lithographical procedure it is possible to use one mask four times for the different layers by using the appropriate quadrants. Using this technique the mask costs can be reduced by about 60%.

The advantages of using MLM single user runs are : (i) lower mask costs, (ii) can be started any date and not restricted to scheduled MPW runs, (iii) single user and (iv) customer receives minimal a few wafers, so a few hundreds of prototypes.

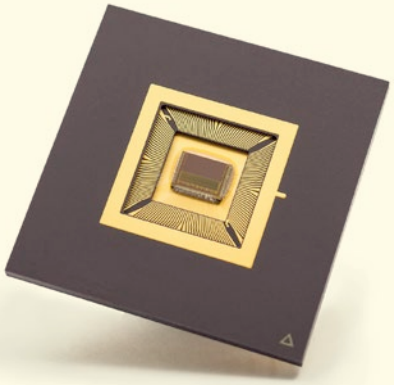
This technique is preferred over MPW runs when the chip area becomes large and when the customer wants to get a higher number of prototypes or preserie. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.

This technique is only available for technologies from ON Semiconductor, IHP, TSMC and XFAB. ■

TECHNOLOGIES

For 2016, EUROPRACTICE has extended its technology portfolio.
Currently customers can have access to prototype and production fabrication in the following technologies :

- ON Semi 0.7µ C07M-D & C07M-A
- ON Semi 0.5µ CMOS EEPROM C5F & C5N
- ON Semi 0.35µ C035U 4M
- ON Semi 0.7µ C07M-I2T100 100 V
- ON Semi 0.35µ C035 - I3T80U 80 V
- ON Semi 0.35µ C035 - I3T50U 50 V
- ON Semi 0.35µ C035 - I3T50U (E) 50 V
- ON Semi 0.35µ C035 - I3T25U 3.3/25 V
- ONC18MS - 0.18 µm
- ONC18MS-LL - 0.18 µm
- ONC18HPA - 0.18 µm
- ONC18-I4T - 0.18 µm 45/70V
- ams 0.35µ CMOS C35B4C3
- ams 0.35µ CMOS C35OPTO
- ams 0.35µ HV CMOS H35B4D3
- ams 0.35µ SiGe-BiCMOS S35
- ams 0.18µ CMOS C18
- ams 0.18µ HV CMOS H18 50V/20V
- BARC Diode for ams 0.35µ CMOS C35OPTO
- WLCSP for ams 0.35µ CMOS C35B4C3
- IHP SGB25V 0.25µ SiGe:C
- IHP SGB25VGD 0.25µ SiGe:C
- IHP SG25H1 0.25µ SiGe:C
- IHP SG25H3P 0.25µ Complementary SiGe:C
- IHP SG25H3 0.25µ SiGe:C
- IHP SG25H4 0.25µ SiGe:C
- IHP SG25H_EPIC (based on SG25H4)
- IHP SG13S SiGe:C
- IHP SG13C SiGe:C
- IHP SG13G2 SiGe:C
- IHP SG25 PIC
- IHP BEOL SG25
- IHP BEOL SG13
- X-FAB XH018 0.18µ HV NVM
- X-FAB XT018 0.18µ HV SOI
- X-FAB XS018 0.18µ OPTO
- TSMC 0.18 CMOS L/MS/RF
- TSMC 0.18 CMOS HV CV018LD
- TSMC 0.18 CMOS HV BCD Gen 2
- TSMC 0.13 CMOS L/MS/RF, G or LP (8")
- TSMC 0.13 CMOS L/MS/RF, G or LP (12")
- TSMC 90nm CMOS L/MS/RF, G or LP
- TSMC 65nm CMOS L/MS/RF, G or LP
- TSMC 40nm CMOS L/MS/RF, G or LP
- TSMC 28nm CMOS Logic, HPL (HKMG)
- TSMC 28nm CMOS Logic, LP (SION)
- TSMC 28nm CMOS Logic, HPM (HKMG)
- UMC L180 Logic GII
- UMC L180 Mixed-Mode/RF
- UMC L180 Logic LL
- UMC L180 EFLASH Logic GII
- UMC CIS180 – CONV diode
- UMC CIS180 – ULTRA diode
- UMC CIS11
- UMC L130 Logic
- UMC L130 MM/RF
- UMC L110AE L/MM/RF
- UMC L65N L/MM/RF - SP
- UMC L65N L/MM/RF - LL
- GF 55 nm LPe/LPx-NVM/LPx-RF
- GF 40 nm LP/LP-RF/RF-mmWave
- GF 28 nm SLP/SLP-RF/HPP
- GF 22 nm FDX
- MEMSCAP METALMUMPS
- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- MEMSCAP PIEZOMUMPS
- ePIXfab-imec SiPhotonics Passives
- ePIXfab-imec SiPhotonics ISIPP25G+
- ePIXfab-LETI SiPhotonics Passives + Heater
- Micralyne MicraGEM-Si
- Teledyne Dalsa MIDIS



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MINI@SIC PROTOTYPING CONDITIONS

FOR UNIVERSITIES AND RESEARCH LABORATORIES

Prototyping costs have been increasing with scaled technologies due to high mask costs. Even on MPW runs with shared costs, the minimum prototyping fee (corresponding to a minimum chip area) is high for advanced technologies such as 90, 65, 40 and 28nm.

In order to stimulate universities and research institutes to prototype small ASIC designs, Europractice has introduced in 2003 the concept of *mini***@sic**.

That means that Europractice has selected several MPW runs on selected technologies on which universities and research institutes have the opportunity to prototype very small ASIC designs at a highly reduced minimum prototype fee. The minimum charged chip area is highly reduced.

Through the *mini***@sic** concept, the price is reduced considerably. For the most advanced technologies however, the prototyping fee is further reduced through extra funding by the European Commission through the Europractice project (only for European universities and research institutes).

SPACE QUALIFICATION ACCORDING TO ESCC9000

During 25 years, Europractice built up a lot of experience for space qualification. Following the ESCC 9000 standard, the service is providing full support to get your product qualified and ready for flight model. Always pushing the limits of the technology the Europractice is the solution to launch your ASIC to space.

From the start of the project, Europractice provides consulting on the ASIC die pad layout taking into account the parasitics of the full package. Afterwards, if necessary, a dedicated package for your ASIC will be manufactured. The expertise of Europractice together with the professionalism of our partners result in a solution that will fit your space requirements.

In order to increase the yield after packaging, Europractice provides their customers with wafer probing prior before to assembly. All ASIC's are assigned to a unique number at wafer level. Taking this approach Europractice is able to provide full traceability of all the components.

When the ASIC's are ready to be assembled into the package, a pre-cap inspection is done. This step is in close cooperation with the customer, our partners and the experts of the Europractice service.

Before chart F4 of the qualification is performed, Europractice will check if the lot can be accepted by performing the "Lot Acceptance Test". This Lot Acceptance Test includes data analysis of the wafers and radiation tests. The radiation tests include the total dose steady-state irradiation (Tid) and single event effect test (SEE).

Over the years, imec, together with its partner Microtest developed, a portable test system called Hatina. This portable tester enables imec to perform a complete measurement and data log of the devices while performing radiation tests. These real-time measurements provide the customer with an in-depth understanding how the ASIC will behave in space.

When passing radiation tests, all the remaining parts will enter the chart F3 for screening and will continue from there to chart F4 for qualification. Working with different partners enables imec to implement in their supply chain a significant amount of quality assurance gates (QA gates). Imec has built up huge experience in logistics and an internally developed tool keeps track of the status of all devices.

In order to assess the operating life time of a device, a dedicated burn-in oven was developed. This oven has the ability to heat your ASIC up to the desired temperature, while the auxiliary components are still at room temperature. This makes sure that when a fail is detected, the customer knows that this is related to the device and not to one of the auxiliary components. During the operating life all devices are monitored and all data is written to a log file.

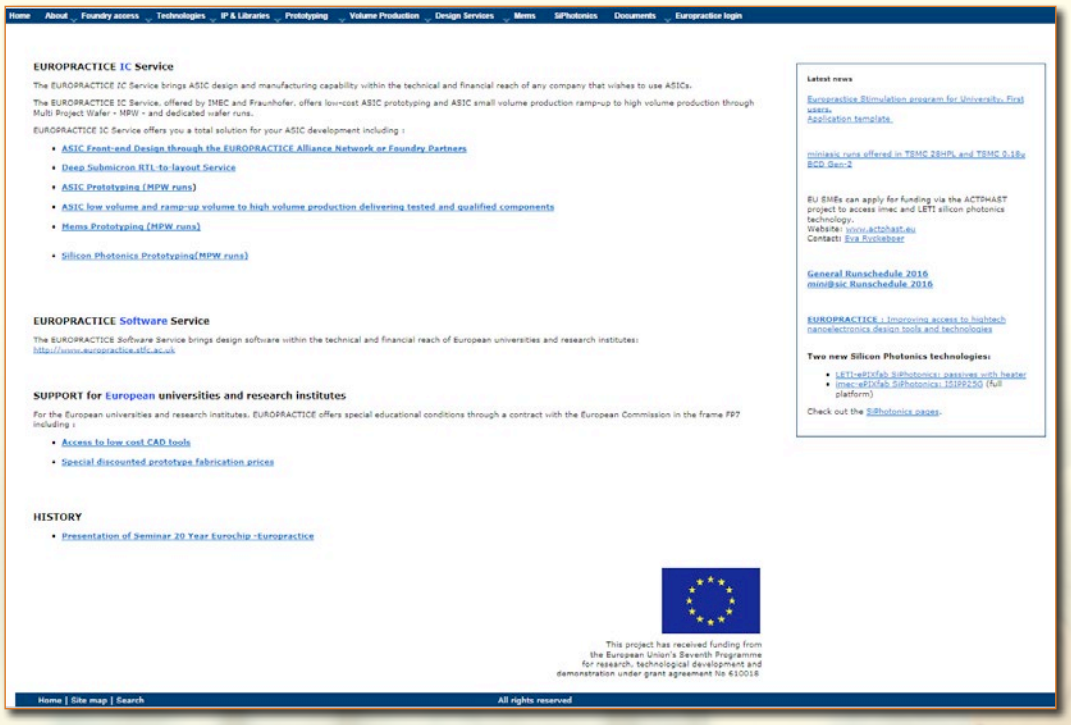
Finally a "Qualification report" is delivered together with the ASIC's (flight models) which contain all the data of each device.

WEB SITE

http://www.europractice-ic.com

The Europractice web site for IC prototyping has been totally renewed and provides full information such as:

- Technologies
- Specification sheets
- Available and supported cell libraries and design kits
- MPW runs
- MPW prices
- Small volume possibilities
- Deep submicron netlist-to-layout service
- Procedures for registration of designs for prototyping
- Etc.



RESULTS

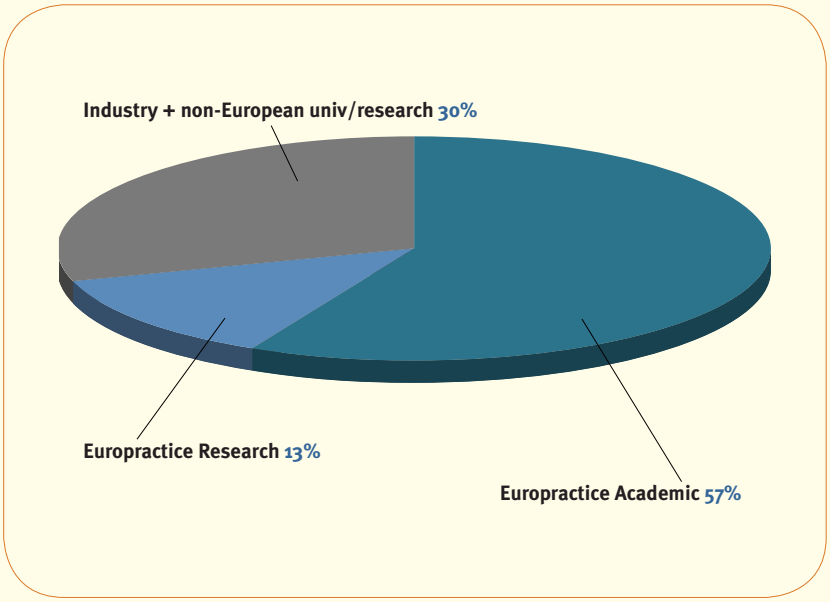
MPW PROTOTYPING SERVICE

ASICS PROTOTYPED ON MPW RUNS

In 2015, a total of 569 ASICs have been prototyped, a significant increase compared to 2014.
70% of the designs are sent in by European universities and research laboratories while the remaining 30% of the designs is being sent in by non-European universities and companies world-wide.

GEOMETRY MIX

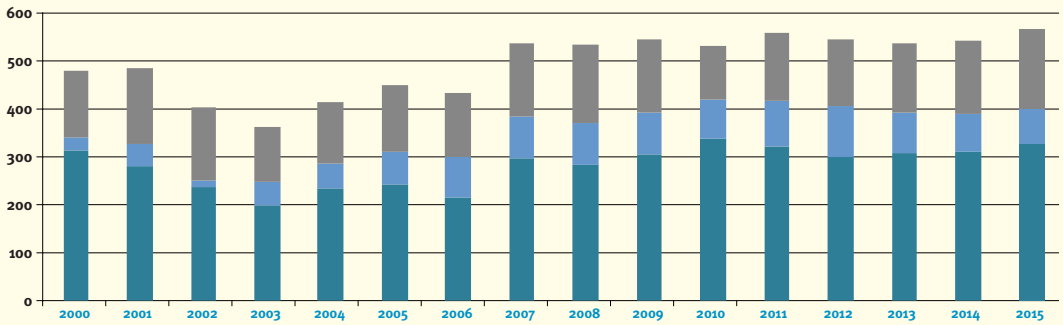
Year over year we see a shift towards newest technologies. Also in 2015 the same trend is shown. Again, the majority of designs is done in 0.18µ / 0.15µ technology. Also the number of designs in Silicon Photonics (indicated as MEMS) technology has taken up. The first designs in 28nm have been prototyped.



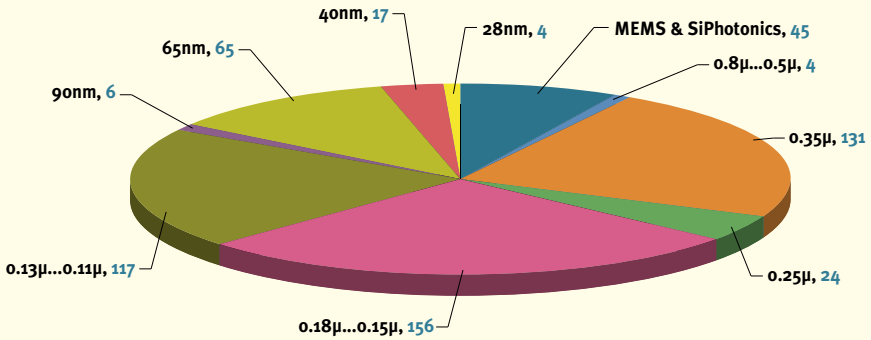
MPW designs in 2015

MINI@SIC

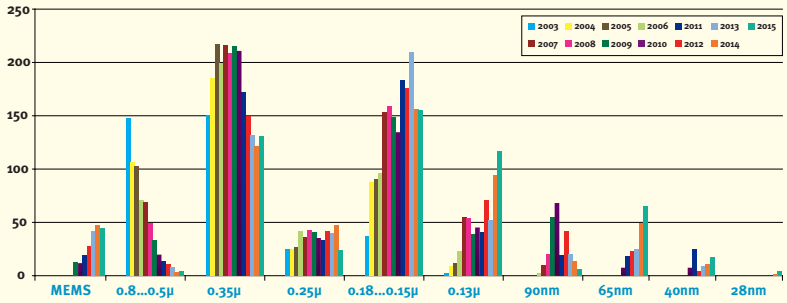
Very encouraging is the fact that the *mini***@sic** concept continues to be accepted very well by the universities in 2015.



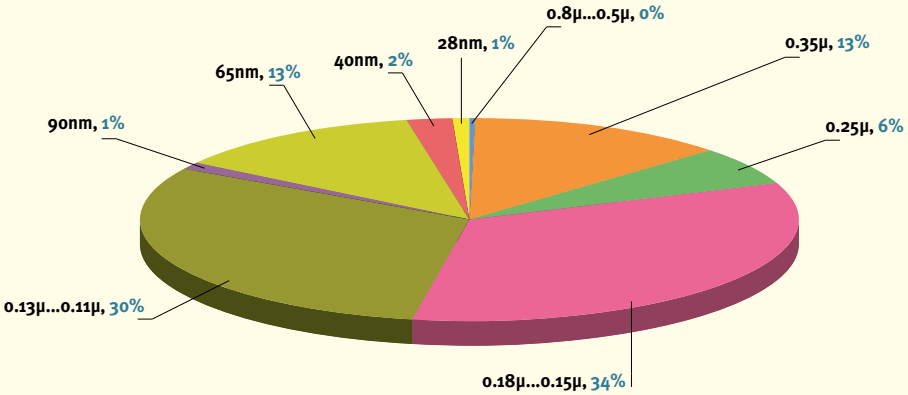
	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
Industry + non-European univ/research	140	159	155	115	128	138	134	154	164	153	113	143	139	144	153	169
Europractice Research	27	46	13	48	52	69	84	87	85	87	83	96	105	87	80	72
Europractice Academic	313	281	237	200	234	243	215	298	285	305	337	321	301	307	311	328



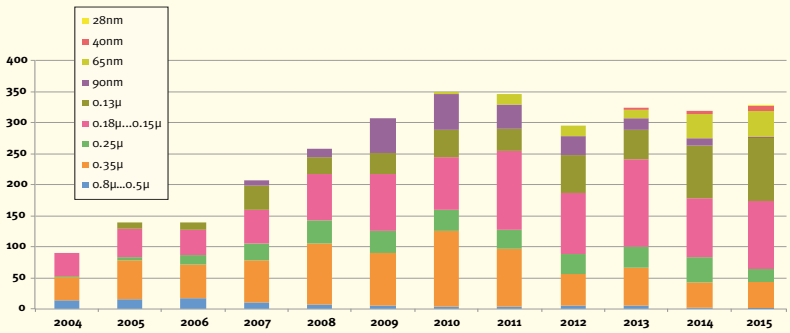
MPW designs in 2015: technology node and number of designs



Geometry mix



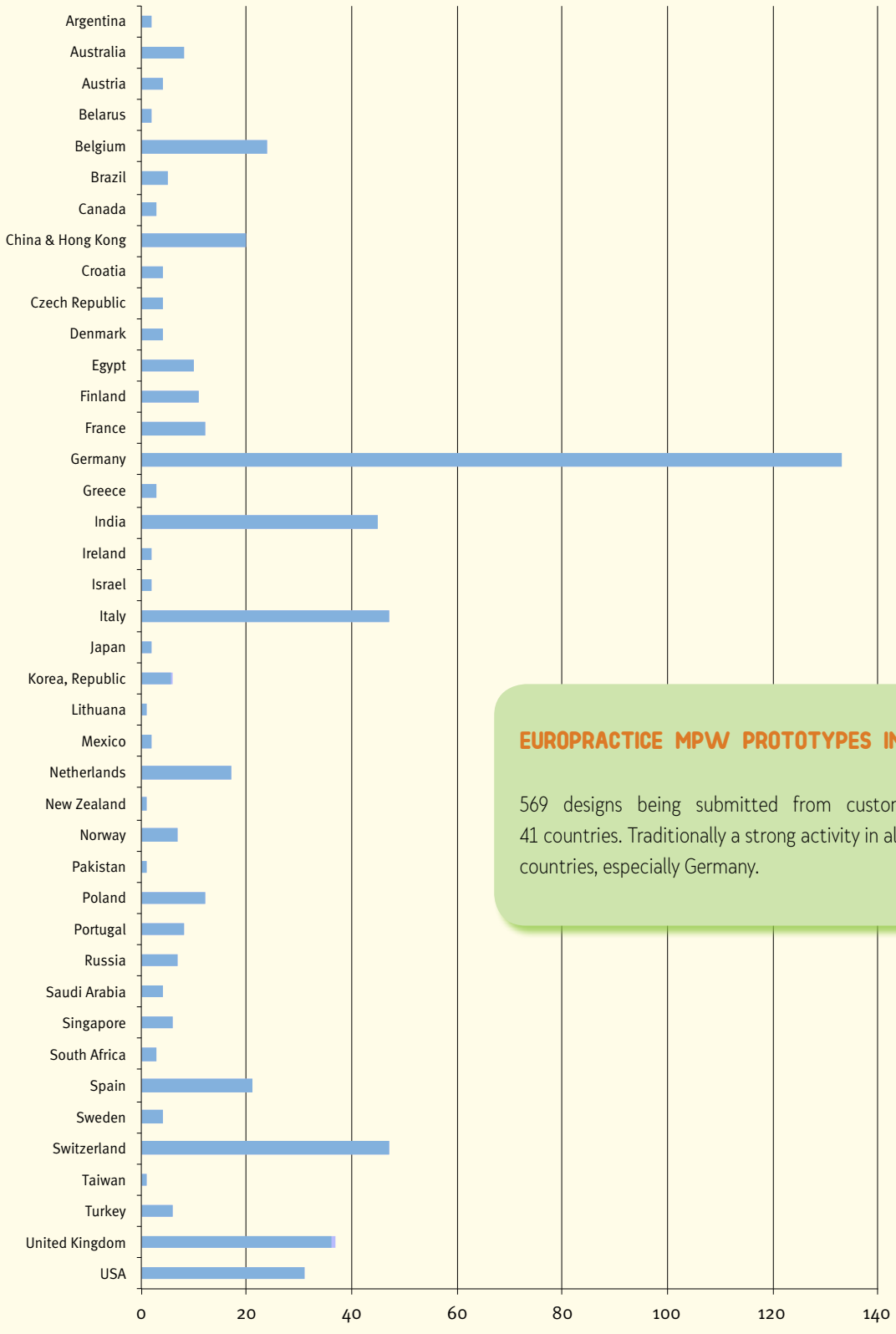
*mini***@sic** *designs per gatelength in 2015*



SMALL VOLUME PROJECTS

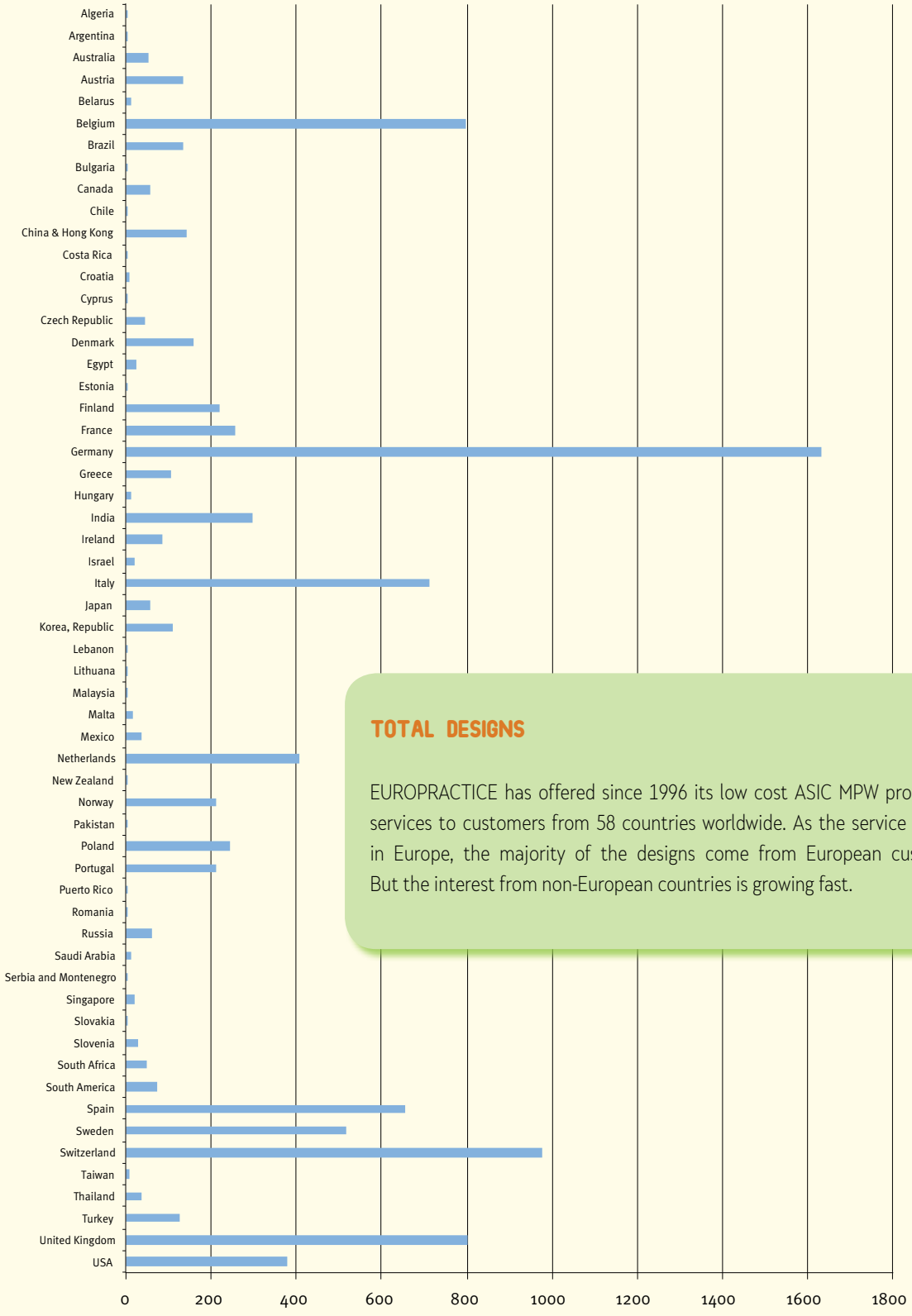
More and more customers are using the COT (Customer Own Tooling) model when they need volume production. Through this COT model they have full control about every aspect of the total design and production flow. Large customers with sufficient ASIC starts and volume production can invest in the COT model as it requires a considerable knowledge and experience about all aspects such as libraries, design kits, transistor models, testing, packaging, yield, etc. For smaller customers the COT model is very attractive but very difficult due to the lack of experience. For those customers EUROPRACTICE offers the solution by guiding the customers through the full production flow applying the COT model. EUROPRACTICE helps you with technical assistance in the selection of the right package, setting up the test solution, yield analysis, qualification, etc.

Through EUROPRACTICE you can also experience the benefits of the COT model.



EUROPRACTICE MPW PROTOTYPES IN 2015

569 designs being submitted from customers from 41 countries. Traditionally a strong activity in all European countries, especially Germany.



TOTAL DESIGNS

EUROPRACTICE has offered since 1996 its low cost ASIC MPW prototyping services to customers from 58 countries worldwide. As the service is based in Europe, the majority of the designs come from European customers. But the interest from non-European countries is growing fast.

EXAMPLES OF ASIC PROJECTS

Multi Project Tapeout for IoT Applications

RWTH Aachen University, Chair of Integrated Analog Circuits and RF Systems, Germany

Contact: Markus Scholl, Ye Zhang, Yishan Wang, Durgham Al-Shebanee, Ralf Wunderlich, Stefan Heinen
E-mail: mailbox@ias.rwth-aachen.de
Technology: UMC 130nm RF CMOS
Die Size: 1.6mm x 1.6mm

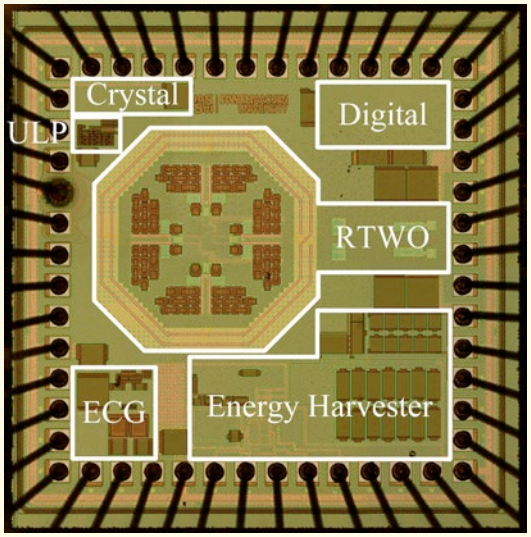
Description

To verify new concepts in silicon and ensure optimum performance one *mini***@sic** block has been divided into several subsystems. Targeting different IoT applications these subsystems have been taped out as a pre-study.

The design includes a low phase noise crystal oscillator as reference clock, a high performance rotary traveling wave oscillator (RTWO) as local oscillator, an ultra low power oscillator (ULP) for deep sleep operation in digital control systems, a wide band RF energy harvester and a low power and low noise electrocardiography (ECG) frontend.

The RF energy harvester, consists of an RF rectifier and a charge pump to increase the harvested voltage to the necessary supply level, utilizes an off-chip, wide band matching network to maximize the harvested energy. In measurements an output voltage above 1V was achieved with -25dBm RF input power at frequencies between 800MHz and 870MHz.

To reduce power consumption in state-of-the-art transceivers a duty cycle system using an ultra low power oscillator can be implemented. Among other application dependent requirements, the power consumption reduction is dependent on the frequency accuracy of the ULP oscillator. In this design a low power bandgap is used to reduce frequency drift over temperature and minimize frequency change with process variations. Therefore the temperature drift can be reduced to 50ppm/°C from 0°C to 100°C in the 32kHz oscillator consuming 325nA from a 1.2V supply as measurements show. For further improvements of the frequency accuracy a digital calibration loop is implemented, tuning the oscillation frequency utilizing the crystal oscillator before entering deep sleep mode. The resulting improvement depends on the duty cycle parameters of the transceiver design but temperature drifts down to 14ppm/°C can be achieved in measurement for typical application scenarios with slow temperature changes (1°C/s) and short sleep periods of 280ms.



Why Europractice?

Europractice's *mini***@sic** program is a great opportunity for universities to do affordable prototyping in state-of-the-art nanoscale CMOS technologies. The access to key software IC design tools, the excellent technical support and customer friendly attitude of its staff members is an invaluable benefit to our tapeouts and thereby enhances the success of our research significantly. Thank you Europractice, thank you imec!

CMOS Readout Circuit for Gallium Nitride (GaN) Photodiodes intended for detection in the Ultraviolet region

[1] Faculty of Electrical Engineering, Delft University of Technology, Delft, The Netherlands
[2] Advanced Detectors, Systems and Nanoscience Group, NASA's Jet Propulsion Laboratory (JPL), Pasadena, California, USA

Contact: Preethi Padmanabhan[1], Edoardo Charbon[1], Shouleh Nikzad[2], Douglas Bell[2], Bruce Hancock[2]
E-mail: preethipadmanabhan@student.tudelft.nl, e.charbon@tudelft.nl, shouleh.nikzad@jpl.nasa.gov, lloyddoug.bell@jpl.nasa.gov, bruce.r.hancock@jpl.nasa.gov
Technology: ams H35 HV CMOS 4M
Die size: 5 x 1 mm²

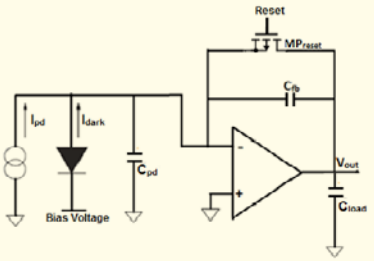


Fig. 1a: Schematic- Capacitive Transimpedance Amplifier (Ipd is the photodiode current, Idark is the dark current of the photodiode, Cpd is photodiode capacitance, Cfb is the feedback capacitance, Cload is the load capacitance, MPreset is the transistor used for reset operation)

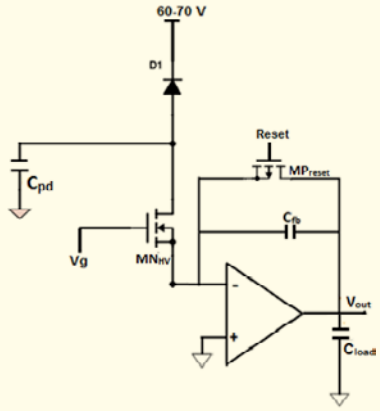


Fig. 1b: High Voltage Protection to low voltage CMOS Circuitry

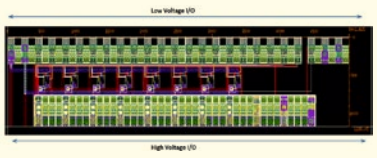


Fig. 2: Chip Overview

Introduction

The UV region in the electromagnetic spectrum is important in order to study about the stars, cosmos, galaxies along with the thin atmospheres in space. Additionally, UV instrumentation also supports medical applications such as cancer detection and tumour delineation. However, owing to the fact that UV instruments are starved of photons, photon counting detectors become an essential requirement. Gallium Nitride (GaN) and its alloys have been used to render solar blind UV Avalanche Photodiodes (APDs) due to their wide band gap nature (3.4 eV for GaN) enabling them to achieve high carrier multiplication and thus, a high gain. These APDs have shown more than 50% quantum efficiency [1][2]. One of the convenient ways to use these detectors would be to have a CMOS Readout Circuit which would provide enough gain to read the photodiode current and generate an equivalent voltage. The main objective of this work is to design a CMOS readout circuit for the GaN APDs. This work has been carried out on a collaborative effort with Advanced Detectors, Systems and Nanoscience Group in NASA's Jet Propulsion Laboratory (JPL) in Pasadena, California.

Description of the project

The GaN photodiodes operate at high voltages. They are reverse biased with voltages in the range of (60-100)V generating an equivalent photodiode current on the order of a hundred pA. The other parameters dictating the design of the readout are the detector capacitance which is in the order of 1 pF and the approximate load capacitance around 20-30 pF. The readouts for these detectors must thus accommodate high voltages, and must be able to rapidly quench the avalanche after photon detection in order to avoid damage to the device. Moreover, it is important to isolate the high voltage bias on photodiode from the low voltage CMOS circuitry. Thus, the 0.35 µm HV technology from Austria Microsystems (AMS) resorted as a nice option to design the readout for the GaN photodiodes. The availability of high voltage NMOS models in the AMS libraries facilitated a convenient technique in protecting the circuitry and also providing a method for quenching the current avalanche that is used for gain in APDs. When a photon is detected, the hot carrier

that is produced creates an avalanche in the detector layers due to the high electric fields in the device. This is the mechanism for gain in APDs. However, the carrier multiplication must be quickly quenched to avoid damage to the APD. Figures 1a and 1b depict the block diagram of a unit cell in the array of CTIAs along with the quenching mechanism. The amplifier architecture in each of the unit cells is a single stage amplifier with a common source configuration. When the diode avalanches, the input current to the amplifier rises suddenly. This rise due to avalanche brings CTIA to saturation causing the input voltage to rise. This is followed by the saturation of the high voltage NMOS transistor (depicted as MNHV in Figure 1b). Thus, much of the supply voltage drops across the high voltage NMOS transistor, thereby reducing the effective bias across the APD. Developing readouts for these diodes was with a motivation to better understand the timing performance of the diode which could later help in single photon detection with the operation of diodes in the Geiger mode which hitherto operate in the linear mode. These considerations led to the design of an array of Capacitive Transimpedance Amplifiers (CTIAs) as a feasible solution to read the current out from the GaN diodes.

The basic operation of the CTIA straightforwardly follows the Figure 1a. The incoming photodiode current (Ipd) is integrated via the feedback capacitor (Cfb) and an equivalent voltage is generated at the output such that the low-frequency DC gain is set by the ratio of photodiode capacitance (Cpd) and the feedback capacitance (Cfb). The feedback capacitor is initially reset by the transistor (MPreset). As soon as the reset switch is released and the photodiode current starts to flow in, the voltage at the input node starts to rise following with the charging of the feedback capacitor. The negative feedback of the amplifier however, maintains the input node at virtual ground and the output of the amplifier thus starts to drop from the initial value set by the reset transistor. Thus, the incoming photodiode current is neatly integrated via the feedback path, generating an equivalent voltage at the output.

Results

Figure 2 shows the top view of the layout designed. The CTIA layout consists of 1x8 linear array of CTIAs laid such that there is high voltage I/O on one side and low voltage I/O on the other, maintaining good isolation between the two. Once these are fabricated and tested, further measurements will enable to validate the simulation results obtained. Since we are targeting signal detection with a time resolution on the order of a microsecond, the CTIA is designed to operate within a 1-10 MHz bandwidth. The total power consumption of the array is estimated to be on the order of a mW at a supply voltage of 3.3 V. The open loop gain of the amplifier is around 45 dB with a 3 dB frequency at about 10 MHz considered enough to integrate the diode current within the given bandwidth.
The design has been submitted for fabrication to Europractice. The availability to prototype ASIC design in different technologies naturally came as a favourable choice to opt for Europractice. The proposed readout will support the GaN detector array for applications in imaging and spectrometry instruments. This test array of CTIAs will facilitate superior designs in future to be better compatible with the GaN APDs. If the time related characteristics of the APDs are examined through this readout design, the circuitry can be updated with timed reset signals and can also facilitate some programmable control circuitry. Additionally, if these detectors start to operate in Geiger mode in future, single photon counting applications will find a place and read out using a digital readout mechanism can be designed. In order to carry forward this project which has immense scope, reading out using these test pixels at the moment is important to help design better compatible circuits. Once these chips are fabricated, a set of measurements will be done to evaluate their performance and further ahead, they will also be tested with the GaN APDs at JPL.

References

[1] Shouleh Nikzad, John J. Hennessy, Michael E. Hoenk, April D. Jewell, Alex G.Carver,Timothy M. Goodsall, Todd J. Jones, Erika T. Hamden, Puneet Suvarna, Neeraj Tripathi, F.Shahedipour-Sandvik, and L. Douglas Bell, "Silicon and III-N UV Photon Counting Detectors," International Image Sensor Workshop, The Netherlands, June 2015.

[2] Puneet Suvarna, John Bulmer, Jeffrey M. Leathersich, Jonathan Marini, Isra Mahaboob, John Hennessy, L. Douglas Bell, Shouleh Nikzad, and F. (Shadi) Shahedipour Sandvik, "Ion Implantation-Based Edge Termination to Improve III-N APD Reliability and Performance," IEEE PHOTONICS TECHNOLOGY LETTERS, vol. 27, NO. 5, March 2015.

Optical 2x2 receiver array and photodiodes structures for visible light communication (VLC)

Department of Electrical, Computer and Systems Engineering, Smart Lighting Engineering Research Center, Rensselaer Polytechnic Institute, Troy, NY, USA

Contact: Dr. Bassem Fahs, Prof. Mona M. Hella
E-mail: fahsb@rpi.edu, hellam@rpi.edu

Technology: ams 0.35 µm opto BARC
Die size: 3 mm x 2 mm

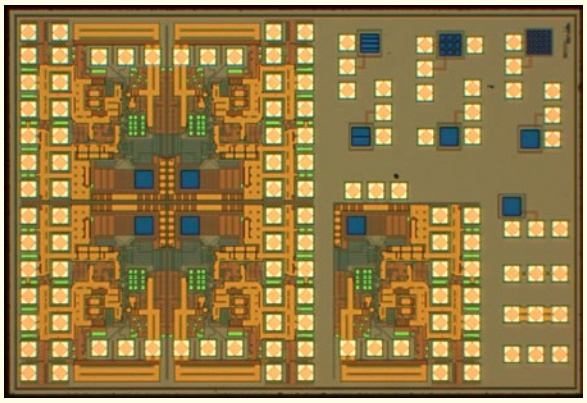


Fig. 1. Tape

Visible light communication (VLC) is an emerging wireless technology that could provide a solution for transmission bandwidth limitations in indoor communication scenarios. Such technology would either replace or complement WLAN infrastructures with a large spectrum of applications from point-to-point communication to high-definition video streaming. Our first VLC receiver tape-out is realized in AMS 4-metals 0.35 µm CMOS featuring an opto option with an integrated NWell/Psub photodiode (PD). In addition, a Bottom-Anti-Reflective-Coating (BARC) layer is used with the PD to maximize the light transmittance to the silicon layers while having all the dielectric layers etched on top of the PD. The PD responsivity is estimated to more than 0.5 A/W in the red. Different PD structures were fabricated to improve the PD responsivity in the visible spectrum and increase the optical bandwidth. Furthermore, a fully-integrated optical receiver using the BARC PD was realized for both optical and electrical testing purposes. A target data-rate in the Gb/s was possible thanks to an integrated programmable equalizer and a small-sized PD area of 100 µm x 100 µm. Fig. 1 shows the micrograph of the fabricated chip. All BARC PDs showed functionality with high responsivity levels. Optical receivers were tested in a real VLC setup with at least 46 cm link distance from a high-speed 680 nm laser-diode source. Data-rates at 1.5 Gb/s and 1.8 Gb/s for On-Off-Keying (OOK) signals were measured with VLC-compliant bit-error-rates (BER) below 10-6 and 10-4, respectively. The measured receiver output eye-diagram at 1.5 Gb/s is depicted in Fig. 2. According to a figure-of-merit taking into account the measured data-rate and the transmission distance, the single-receiver performance ranks first among all reported laser-based VLC solutions to date.

Why Europractice?

The post-processing of the manufactured BARC PDs has demonstrated excellent quality although the different PDs had non-conventional structures. The support teams showed valuable help throughout the complete design process with continuous DRC-errors tracking and validation on the customized photodiodes.

Acknowledgement

This work was supported primarily by the Engineering Research Centers Program (ERC) of the National Science Foundation under NSF Cooperative Agreement No. EEC-0812056 and in part by New York State under NYSTAR contract C090145. The authors would like also to thank AMS, Austria, and Fraunhofer Institute, Germany, for design-kit and fabrication facilities.

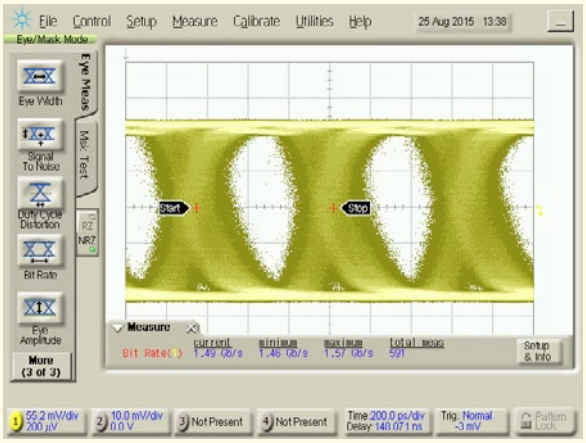


Fig. 2. Measured optical receiver output eye-diagram at 1.5 Gb/s.

HV Neural Stimulator for Visual Prosthesis

The University of Bremen, the Institute of Electrodynamics and Microelectronics (ITEM), Bremen, Germany

Contact: Dr. Dmitry Osipov, Dr.-Ing. Prof. Steffen Paul
E-mail: osipov@item.uni-bremen.de,
steffen.paul@me.uni-bremen.de

Technology: ams 0.35 µm HV CMOS
Die size: 4 mm²

Neural electrical stimulation of the human brain is widely used for many biomedical applications. One promising area is the vision restoration for people after accidents. Local electrical stimulation of visual cortex produces point-like visual sensations, or phosphenes, which can be used to create visual prosthesis. Activation currents for the epicortical placement of stimulation electrodes are in order of a few mA. The electrode-tissue interface resistance for currently tested electrodes lies in the range of several kΩ. The current stimulator for the use with epidural electrodes has to provide the possibility to stimulate with biphasic currents with amplitudes ±10.24 mA with 20-100 µA steps. Because of a relatively high load resistance the output voltage compliance should lie in the range of 90-120 V. For the current research, to explore the optimal waveform for the phosphenes generation, the stimulator has to provide the possibility to stimulate with arbitrary current waveforms.

Design Description

The typical current stimulation architecture is shown in Fig.1. The reference electrode is connected to the VHH/2 voltage. This architecture provides the opportunity to perform the biphasic stimulation (the stimulation with both anodic and cathodic pulses). The biphasic stimulation is important, because although the neurons are activated with any phase, the charge injected into the tissue can lead to the electrolysis and, consequently, to the damage of the tissue. To avoid this, the tissue has to be stimulated with the opposite phase after the activation phase (anodic or cathodic) in order to completely remove the injected charge.
The proposed HV output interface is shown in Fig. 2. The output current of the external DAC multiplied by 32 is mirrored by the HV current mirror to the output node. The φ_A and φ_B control signals set the current direction. A non-overlapping phases generator is used to prevent the shorting of the DAC output to the ground. Both switches operate in the LV domain and do not require additional level shifters. The chosen HV

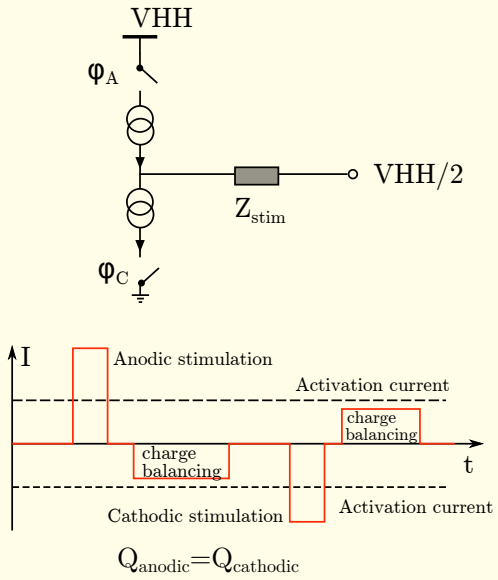


Fig. 1. Standard stimulator architecture for cortex stimulation and the stimulation sequence. The charge injected during anodic phase should be completely removed during cathodic phase.

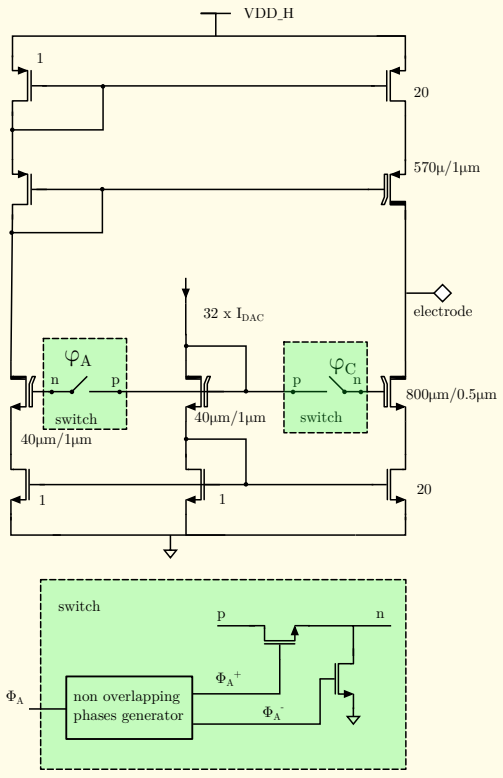


Fig. 2. Proposed HV output interface

transistors sizes sure their operation in the safe area region. By operating with the HV VDD below 90 V the 10 years lifetime is predicted by the AMS SOAC (Safe Operation Area Check) tool, if operating between 90-120 V the predicted lifetime reduces to 3 years. The output HV transistors also operate as ESD protection diodes providing the ESD path through their parasitic bulk-source diodes.

Results

The HV output interface with two channel ASIC was fabricated in HV AMS 0.35 µm technology. The die photo is shown in Fig.3. Two variants of the stimulator with and without standard ESD cells were fabricated. The measurements showed no difference between the stimulators with and without library ESD protection. For measurement purposes the input current was delivered to the input node of the HV output interface by 12-bit external current DAC. The measured output current for the 512 µA current on the input node is shown in Fig.4. The tissue was modelled as a reactive load consisting of a parallel connection of 4.1 kΩ resistor and 1 pF capacitor. The inter pulse current does not exceed 60 pA. The residual charge after biphasic stimulation equals to 4 nC.

Why Europractice?

The wide set of available technologies gives us the opportunity to choose one that fits best to the design requirements. The design support from Europractice is really helpful, especially in not quite obvious issues of the chip finalization and design rules checks. The *mini***@sic** program allows us to prototype design ideas fast and cheap in silicon.

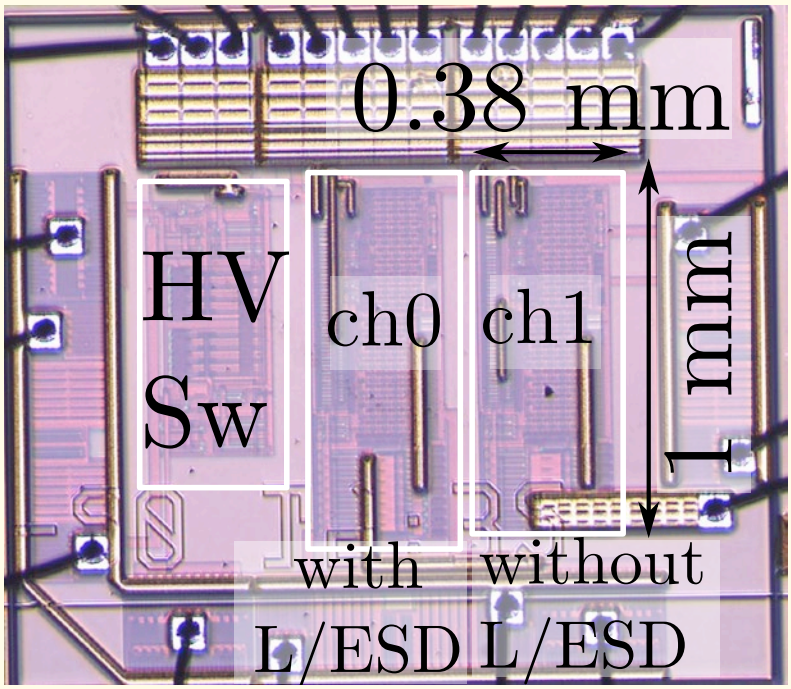


Fig. 3. Test ASIC with two channel HV output interface

Acknowledgment

This work was supported by the Creative Unit I-See, University of Bremen (Excellence Initiative)

References

Osipov D., Paul St., Strokov S. Kreiter A. K. "A new current stimulator architecture for visual cortex stimulation", Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), 2015

Osipov D., Paul St. "A novel HV-switch Scheme with Gate-Source Overvoltage Protection for Bidirectional Neural Interfaces", Electronics, Circuits and Systems (ICECS), 2015 22st IEEE International Conference on, 2015.

Fig. 4. The measured output current pulses

Wireless Energy and Data Transmission ASIC for a Medical Implant

Institute of Nano- and Medical Electronics, Hamburg University of Technology, Germany

Contact: Bibin John, Rajeev Ranjan, Lait Abu Saleh, Dietmar Schroeder and Wolfgang H. Krautschneider
E-mail: bibin.john@tuhh.de
Technology: ams 0.35 µm HV-CMOS (H35B4C3)

In future, medical implants will be used for telemetric monitoring of patients. An implant contains sensors and wireless electronics for monitoring vital biomedical parameters inside the body of the patient. External data reader hardware will receive the sensor data wirelessly from the implant and send these data to the doctor. This approach can reduce frequent visits of the patient to hospital after a major operation.

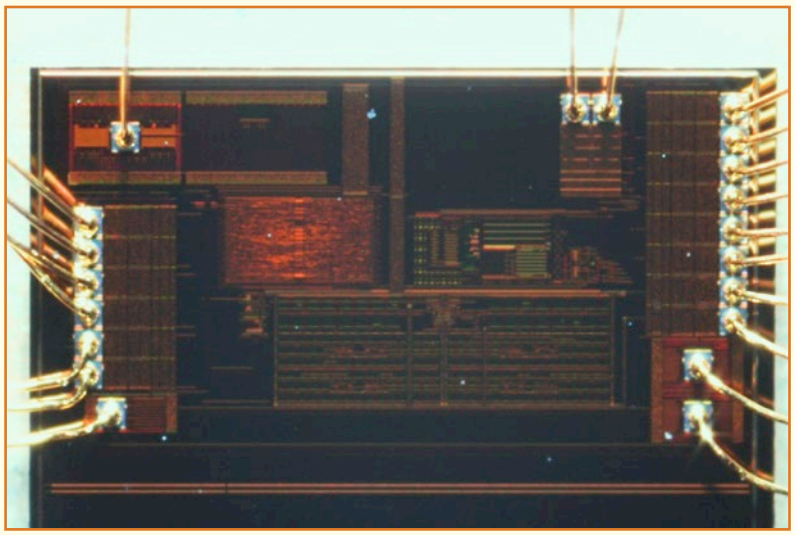


Fig. 1. Fabricated ASIC

Description

This ASIC is designed to receive power wirelessly using inductive coupling, fetch sensor data from a separate chip and transmit data wirelessly. Error detection and forward error correction are implemented to enhance data integrity for wireless data transmission.

The ASIC consists of three modules: wireless power reception, sensor data reception and wireless data transmission. The wireless power reception module receives energy through inductive coupling in order to power the whole implant. It has on-chip rectifier and Low Dropout Regulator (LDO), which converts the sine signal output of the resonant LC circuit into regulated 3.3V supply.

The sensor data reception module fetches sensor data from a separate chip in the implant using SPI interface. The data packet passed on to the wireless data transmission module consists of sensor data, chip address, error detection and forward error correction bits. The wireless data transmission module transmits the data packet to the external data reader hardware. The on-chip charge pump supplies high voltage for sending data in the form of pulses.

The chip has been tested and it consumes approximately 1mW. The small dimension (2.3 mm x 1.3 mm) and low power consumption of this chip makes it suitable for the implant planned for the project.

Publications

Rajeev Ranjan, Bibin John, Dipal Gosh, Soumil Kumar, Lait Abu Saleh, Dietmar Schroeder and Wolfgang H. Krautschneider, "Wireless Energy and Data Transmission ASIC for Blood Pressure Measurement in an Aneurysm Implant", Biodevices 2016, Feb 2016

Why Europractice?

Europractice's designkit services and organized MPW, *mini***@sic** runs is crucial for a research project demanding small volume production at an affordable price. The Europractice staff, both at the Fraunhofer Institute and IMEC, provides excellent service and information in each stage of the chip design process.

Acknowledgement

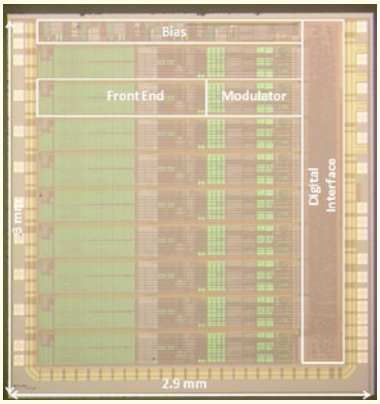
This work is funded by Federal Ministry of Education and Research (BMBF, ESiMed [16 M3201D])

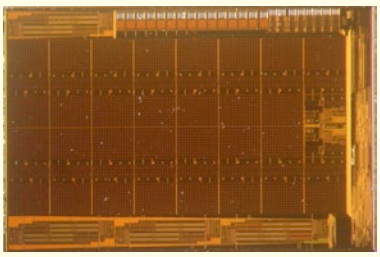
Integrated Circuits for an Implantable Bidirectional Neural Interface

Università di Cagliari, EOLAB – Microelectronics and Bioengineering Lab, Italia

Contact: Massimo Barbaro, Caterina Carboni, Lorenzo Bisoni, Roberto Puddu
E-mail: {barbaro,caterina.carboni,lorenzo.bisoni,roberto.puddu}@diee.unica.it

Technology: ams AG C35 0.35µm CMOS 4M and ams AG H35 0.35µm HV-CMOS 4M
Die size: 2.9 mm x 3 mm (C35) and 5.2 mm x 3.4 mm (H35)





This research activity is focused on the realization of an implantable electronic system capable to interface the human neural system and a robotic hand prosthesis. The system is needed to implement a bi-directional interface capable of recording and decoding the neural commands sent by the brain to the hand and to generate a feedback stimulus to provide sensory information to the brain. Such kind of closed-loop is crucial for the embodiment of the prosthesis in order to realize a "natural" rather than "artificial" prosthesis. The system will be implanted in the stump of an amputee, connected to his/her peripheral neural system through an array of electrodes and wirelessly connected to the prosthesis. Low-power and low-area constraints are particularly stringent since the device should be either battery-operated or inductively powered through the skin.

Description

The recording-stimulation system is composed of an analog front-end implemented in two different integrated circuits and of a digital back-end implemented in a Xilinx Spartan6 LX45 prototyping board. The recording module (implemented in C35 process) includes eight parallel channels, each with a band-pass filter and a sigma-delta converter. The BPFs and the modulators are integrated in a microchip while the decimator module is hosted on the FPGA and shared among all channels. The BPF amplifies the neural signal filtering unwanted biological and environmental interferences. The gain can be programmed by the user and must be set properly to benefit from the amplification effect without risking the loss of information due to amplifier saturation. The stimulator, implemented in the high-voltage H35, contains eight low voltage current DACs to generate the stimulation currents and eight high-voltage output stages to mirror the current in the high-voltage domain altogether with two voltage boosters able to raise the voltage up to 17V. Stimuli and the booster configuration are managed by the digital back-end hosted on the prototyping board. The two microchips are stacked on the same PCB making it possible to embed in a single compact device a bidirectional interface between the electrodes implanted in the peripheral neural system and a host computer or a robotic limb, as foreseen for the final project phase.

Results

The recording module has shown its capability to record neural spikes in the order of tens of microvolts with a total underlying noise of less than 5µVrms. The stimulator can elicit with bi-phasic pulses the single nerve fascicles and evoke a correspondent reaction on muscles, making it possible to elicit selectively different muscles with different stimulation channels. The tests prove the system capability to be used as a compact, efficient and complete device for neural recording and stimulation in laboratory trials with small animals and open very interesting perspectives on future developments aimed at making the device fully implantable for long-term experiments on humans.

Why Europractice?

EOLAB has been member of Europractice for more than 10 years, being thus able to introduce state-of-the-art EDA/CAD software in the curriculum of the students of the B.SC. and M.Sc. courses of study in electronic engineering and of the Ph.D. in Electronic Engineering and Computer Science. The possibility offered by MPW allowed us to successfully participate to several European Research Projects in the role of technology providers.

Acknowledgements

This work was partially funded by MIUR (Italian Ministry of Education, University and Research) through project HANDBOT (PRIN 2010/2011), by Italian Ministry of Health through project NEMESIS and by the European Commission, ICT-2013.9.6 FET Proactive: Evolving Living Technologies (EVLIT), through project NEBIAS (n. 611687).

A large dynamic range charge measurement ASIC for beam calibration and monitoring in high intensity radiotherapy applications

Turin section of National Institute of Nuclear Physics -INFN- in collaboration with Physics Department of Turin University and DE.TEC.TOR. Devices & Technologies Torino

Contacts: Giovanni Mazza, Federico Fausti
E-mail: mazza@to.infn.it, fausti@to.infn.it
Technology: ams 0.35 CMOS C35B4C3
Die size: 4680 x 5800 µm

The TERA09 chip will be employed in the electronics readout of monitor chambers used as on-line detectors for the newest (and future) generation of particle accelerators in hadrontherapy applications. The trend in this application is to use compact accelerators that provide high-intensity pulsed beams.

Description

This new ASIC is a 64 channels, bipolar current-to-frequency converter (or charge-to-counts converter), designed in CMOS 0.35 µm technology. Each channel (fig. 1) is based on the charge-recycling integration technique and embeds both the current-to-frequency converter and a 32-bits counter. The chip is able to manage high intensity currents, maintaining an excellent linearity in the conversion into counts of the charge collected at the electrodes over more than 4 orders of magnitude. From the post-layout simulations (Fig.2) it is possible to appreciate that the single channel conversion linearity is maintained from few hundreds of pA up to 15µA, with a deviation of the order of 1%. The charge collected is related to the dose released by the beam to the patient, therefore a great accuracy is required. The chip architecture allows a dead time free data acquisition and is able to change the range of the input current, connecting in parallel a variable number of channels. A 320 MHz master clock permits a maximum counting rate of 80 MHz. In this technology node, an LVDS receiver has been designed in order to control the electronics noise. Under these parameters, the dynamic range of the readout system applications is very wide in terms of input currents: ±100pA up to ±1mA for a quantum charge of 200 fC (the conversion resolution).

The project is performed by the National Institute of Nuclear Physics (INFN), site of Torino, in collaboration with the Physics department of the Turin University and the university spin-off company DE.TEC.TOR. (Devices & Technologies Torino S.r.l.). The TERA09 is patent pending. The ASIC design has been submitted in September 2015 (Fig.3a, the TERA09 Layout) and we received the first prototypes at the beginning of December.

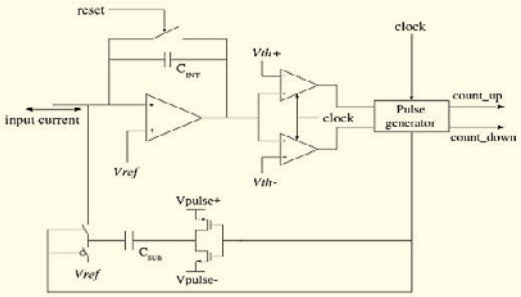


Fig. 1.: The TERA09 channel block diagram.

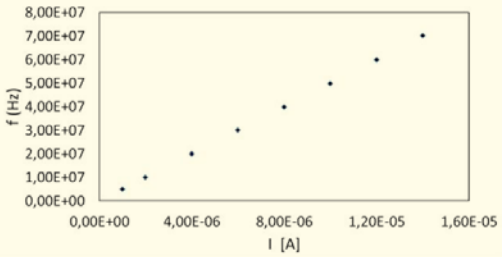


Fig. 2.: Post layout simulation of the single channel current-to-frequency conversion.

Results

The tests on TERA09 prototypes are still ongoing. The digital logic functionalities has been successfully tested and the channels parallel interconnections are verified. The conversion linearity will be under our attention during the next weeks.

Why Europractice?

Europractice offered us the possibility to work in optimal conditions with a technology, the AMS 0.35 µm, which reliability and strength are essential features in the medical field. Moreover the customer support, which includes checks of designs for errors, is excellent.

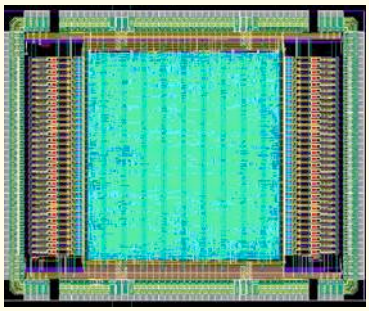


Fig. 3.: (a) TERA09 Layout representation from Cadence Virtuoso. (b) TERA09 PCB Motherboard with the ASIC.

A low power front-end for fast single photon counting in ring imaging Cherenkov detectors

INFN & University of Milano Bicocca, Italy

Contact: Dr Claudio Gotti
E-mail: claudio.gotti@mib.infn.it

Technology: ams AG C35 0.35µm CMOS 4M
Die size: 2000 x 2500 µm^2

Several modern light sensors provide excellent sensitivity to single photons. Among these, pixelated devices such as multi-anode photomultiplier tubes (PMTs), with multiplication chains based either on discrete dynodes or on microchannel plates, are available off the shelf from many manufacturers. Pixel dimensions are usually in the range of a few mm2. Their fast response and good spatial resolution can be used for precise single photon imaging, as required for instance by ring imaging Cherenkov (RICH) detectors, employed for particle identification in high energy physics experiments.

Description

The CLARO8 is a 8 channel ASIC designed for fast single photon counting with multi-anode photomultiplier tubes. The current version of the chip, CLARO8v2, was designed in 2015 (Fig. 1). Single photon signals are fast current pulses carrying a charge in the range of 10 fC to 1 pC in about 1 ns. Each channel of the CLARO8v2 has a differential structure, and is composed of a charge sensitive amplifier, a DAC and a comparator. The DAC allows to set the threshold of the comparator. Each channel gives at its output a digital signal whenever the input pulse from the photomultiplier exceeds the threshold. The fast return to baseline of the amplifier and of the comparator, below 25 ns in nominal operating conditions, allows counting rates up to 40 M hits/s (Fig. 2). The low power consumption, about 1 mW per channel, allows to place many channels close together to instrument large planes without the need for special cooling. The noise of the charge sensitive amplifier at 10 pF input capacitance is 0.3 fC RMS. The threshold can be precisely set in a wide range, between 5 fC and 3.2 pC.

The gain and threshold settings for each channel, as well as other features of the chip, can be programmed via SPI, and are stored in a 128-bit register protected against soft errors (single event upsets) with triple modular redundancy (TMR). The configuration register also allows to pulse individual channels and to read their outputs, thus providing a way to test the analog channels via SPI only.

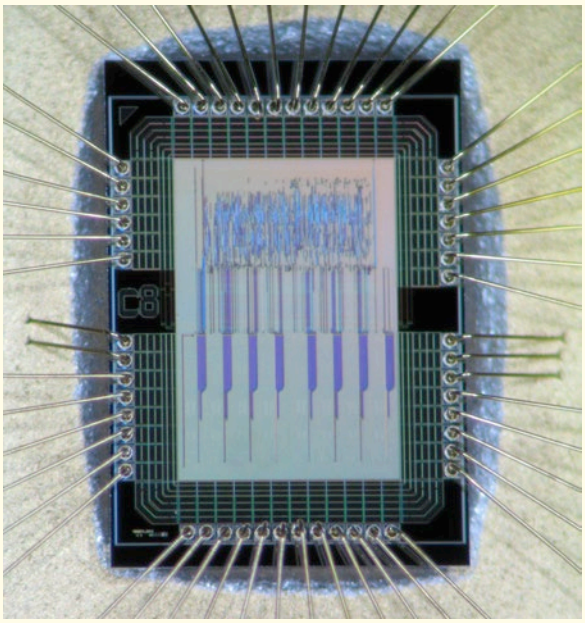


Fig. 1.: Photograph of the CLARO8v2 prototype

Why Europractice?

Europractice provides access and support for a wide range of IC technologies, and all the software tools that a designer needs. Several MPW runs throughout the year allow to develop small prototypes in short time and with reasonable costs, as is often required in the field of applied research.

Acknowledgements

The CLARO8 is the result of a collaboration between INFN Milano Bicocca (P.Carniti, L.Cassina, C.Gotti, M.Maino, G.Pessina), INFN Ferrara (A.Cotta Ramusino, M.Fiorini, R.Malaguti), and AGH Krakow (M.Baszczyk, P.Dorosz, W.Kucewicz). The work was funded by Istituto Nazionale di Fisica Nucleare (INFN), Italy, in the framework of the LHCb RICH upgrade project.

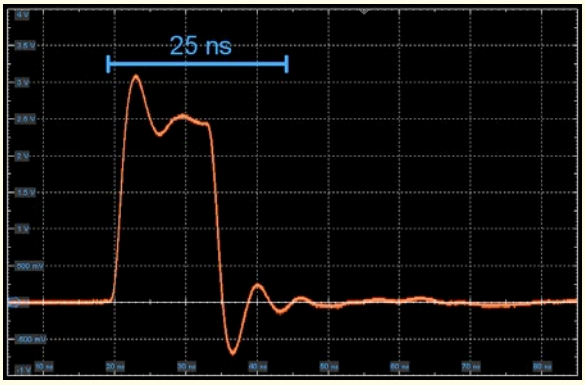


Fig. 2.: A typical single photon hit at the output of the CLARO8v2

ATHENIS_3D Test Chip for High Temperature Characterization

Fraunhofer IIs, Department Integrated Circuits and Systems, Erlangen, Germany

Contact: Norbert Schuhmann
E-mail: norbert.schuhmann@iis.fraunhofer.de
Technology: GLOBALFOUNDRIES 28nm Super Low Power
Die Size: 1.64 mm x 2.20 mm

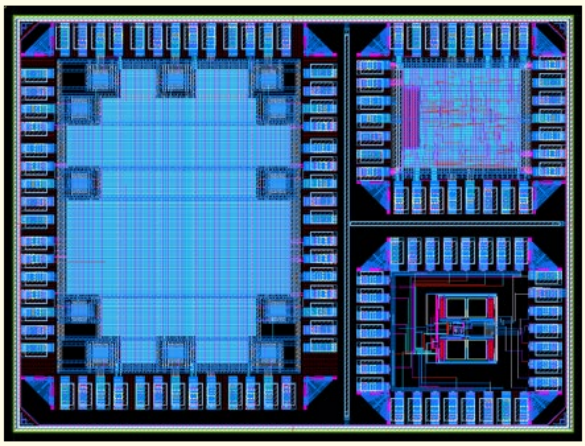
In industrial and automotive applications there is continuing demand for semiconductors running at an extended junction temperature range from -50 to +150 °C, e.g. to avoid active cooling or heat sinks. Even temperatures up to 175 and 200 °C are requested for digital and mixed signal electronic components directly connected with combustion engines, electric drives, etc.

Within the EU-project ATHENIS_3D (Automotive Tested High voltage and Embedded Non-Volatile Integrated System on Chip platform employing 3D Integration) the industry's first 3D heterogeneous integration technology platform for harshest automotive conditions with high temperature digital and mixed signal silicon designs using technologies from 180 to 28 nm, through silicon vias (TSV) and wafer level packaging (WLP) will be explored. ATHENIS_3D is an FP7 European funded project, where eleven partners from five different countries develop a new technology platform for automotive electronics. With this innovative IC platform electronic engineers will be able to integrate more functionality on a single chip for lower costs.

Description

The purpose of TESTCHIP28 is to analyze the usability of designs in 28 nm technology for industrial use cases in very high temperature range. Regular I/O-, standardcell libraries and RAM generators usually cover the operating conditions with temperatures from -40 °C to 125 °C or in some cases the extended range up to 150 °C only. So new methods to predict the circuit behaviour at higher than specified temperatures have to be developed as well as strategies to improve the overall performance and additional design rules to cover very high temperature stress.

The TESTCHIP28 design is implemented in Globalfoundries 28 SLP technology and consists of three separate sub-chips, LOGIC, RAM and ADC (see chip plot and photo).

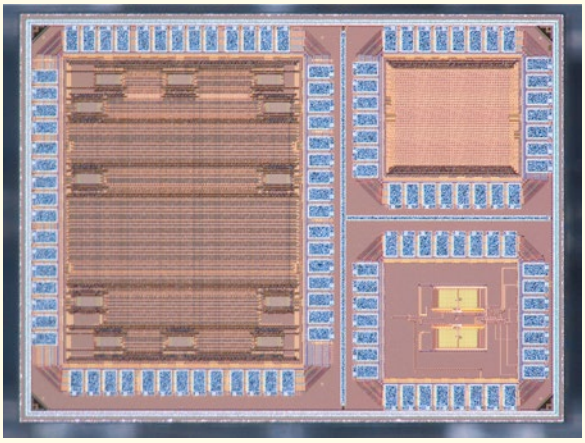


On the LOGIC chip 12 different ring oscillators and delay line sub-designs have been implemented, each with its own power and ground supply, to allow independent characterization. They differ in the type of used standard cells (nand, nor or inverter), in drive strength and the magnitude of loads connected to each of the logic stages.

The RAM sub chip will investigate the usability and behaviour of standard RAM generator cells under high temperatures and is composed of a 1k x 32 highspeed RAM with built-in memory BIST to run stand alone tests.
The ADC sub chip focuses on behaviour of analog structures of a 12 bit successive approximation A/D-Converter.
All designs will be evaluated with dedicated temperature profiles from -40 up to 200 °C using a Thermostream high precision thermal generator. In the meantime a small SoC with MIPS microcontroller, FPU and DSP, RAMS, I/O and a specific high temperature MRAM interface is in development.

Why Europractice?

The availability of this 28 nm technology for a small test chip at low cost made the choice of this low leakage technology a good and cost-effective option. The availability of ARM cell libraries pad libraries and was essential for timely design completion.



Digital Dynamic Frequency Divider in D-Band (110 - 170 GHz)

University of Paderborn

Contact: Umair Ali, Prof. Dr.-Ing Andreas Thiede
E-mail: umair.ali@uni-paderborn.de, thiede@uni-paderborn.de
Technology: IHP 0.13µm SG13G2 SiGe:C
Die size: 0.47 mm^2

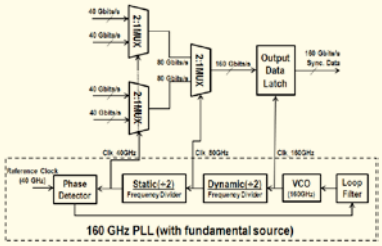
In recent years, the demand for analog bandwidth has increased manyfold for the communication, radar, and sensor applications. Inevitably, to meet the higher bandwidth demand, the analog components have to operate at increasingly higher frequency bands, which are opened up by state of the art semiconductor device technologies. However, while the domain of analog circuits has made continuous progress, the advancement in the digital circuits is relatively slower. Therefore, the research at our group is focused on pushing the maximum frequency of operation for in particular digital circuits. In one of our research project, basic building blocks of a digital 4:1 multiplexer (MUX) for data rates up to 160 Gbits/s, namely voltage-controlled oscillators (VCOs), frequency dividers, and phase-locked loops (PLLs) are intended to be designed and characterized. Out of these building blocks, the design and characterization of the frequency divider have been explained here. Fig. 1 shows the proposed architecture of the MUX.
One potential application of such multiplexers can be seen in digital short range communication, e.g. chip-to-chip.

Description

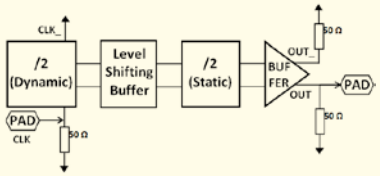
Generally, flip-flop based static frequency dividers are considered to be the first choice for frequency dividers. Maximum operating frequencies of 128.7 GHz[1] and 133 GHz[2] have been reported in SiGe technology for such static frequency dividers. The sub-mm wave frequency synthesizers with fundamental mode oscillators demand significantly higher operating frequencies from the frequency dividers. Static dividers have tendency to work over a large bandwidth but they fail to fulfill the high operating frequency requirements at sub-mm wave frequencies. For instance, the maximum operating frequencies of both[1] and[2] prove insufficient for 160 GHz fundamental VCO based PLL, which is an essential component of our proposed 160 Gbits/s multiplexer. To overcome the maximum operating frequency limitations of the static frequency dividers, dynamic frequency dividers are proposed.
Dynamic frequency dividers are classified into two types i.e. analog and digital. The analog frequency divider, also known as regenerative divider, is based on mixers such as Gilbert cell. The digital dynamic frequency divider is derived from flip-flop based static frequency divider. However, in contrast to the conventional static frequency divider the latching differential pair has been completely omitted to reduce the load for the sensing differential pair to extend the maximum operating frequency[3]. We have opted for digital dynamic divider scheme as we are focusing on digital circuits. To the author's knowledge, such digital dynamic divider has been adopted from HEMT technology to bipolar successfully for the first time.
Fig. 2 shows block diagram of the fabricated divide ratio four frequency divider. The input clock having frequency fin is fed to the first stage dynamic divider which divides the signal frequency by two. The first divider stage is followed by the level shifting buffer consisting of emitter followers. The following static divider stage further decreases the signal frequency to half and ejects the signal at fin/4. The chip micro photograph of the divider is shown in fig. 3.

Results

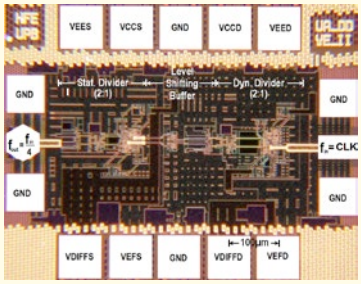
With single-ended sine wave clock input, the dynamic divider was measured to be operational from 100 to 166 GHz. The measured maximum frequency of operation is comparable to the fastest reported Gilbert cell based analog dynamic divider in SiGe technology[4]. The input power sensitivity curve of the dynamic frequency divider is shown in fig. 4. The divider needs input power of -4 dBm at 166 GHz input frequency.



◀ *Fig.1.*

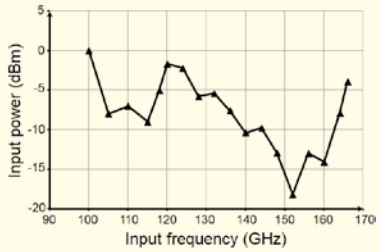


▲ *Fig.2.*



▶ *Fig.3.*

▶▶ *Fig.4.*



Why Europractice?

Europractice plays unique role of a bridge between the IC designers at our University and the state-of-the-art IC fabrication houses e.g. IHP. We are thankful to the Europractice team for providing quality administrative services for each of the MPW runs at an affordable price.

Acknowledgment

We are thankful to IHP for chip fabrication and German Research Foundation (DFG) for funding project TH829/9-1.

References

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Silicon Photonic Components for Optical Data Links in High Energy Physics Experiments

CERN, Geneva, Switzerland

Contact: Marcel Zeiler
E-mail: marcel.zeiler@cern.ch
Technology: imec ISIPP25G
Die size: 5mm x 5mm

Future high energy physics experiments (HEP) at CERN will produce a higher rate of particle collisions compared to the Large Hardon Collider (LHC) which discovered the Higgs boson. This will lead to higher radiation levels inside the particle detectors and an increase in generated measurement data. Consequently, new optical transceivers that provide high data rates and that can withstand high levels of ionizing and non-ionizing radiation will be needed to read-out the measurement data of the particle detectors. Silicon photonics (SiPh) technology is currently being regarded as a potential solution to address these challenges due to recently demonstrated high data rate optical transmitters and receivers as well as an expected radiation hardness similar to that of silicon particle sensors. Our research aims at answering the question whether high-speed, radiation-hard optical transceivers can be designed and manufactured in the SiPh platform.

Description

Our group has already demonstrated that SiPh Mach-Zehnder modulators (MZMs) are relatively insensitive to non-ionizing radiation. However, the same devices strongly degrade when exposed to ionizing radiation [1]. In order to be able to deploy SiPh based optical transceivers within future particle detectors at CERN, a MZM that is resistant against high levels of both kinds of radiation has to be found. Therefore, we produced a chip design with which key design parameters that affect the radiation hardness of MZMs can be identified. This design includes different MZMs with varied design parameters, such as the etch depth of the waveguides, the doping concentrations of the pn-junctions incorporated into these waveguide, the arm length of the MZMs and the shape of the pn-junction itself, i.e. whether the junction extends laterally or longitudinally with respect to the propagation direction of light. The various MZMs were either custom designed or taken as a building block from the Process Design Kit (PDK).

Even though the current research focus lies on radiation hard transmitting devices, some building block photo diodes (PDs) are also part of the chip layout. They will be used to get first results of the radiation hardness of receiving devices. In addition, several passive test structures, e.g. to determine the losses of waveguides, complete the design. A microscope image of a fully fabricated chip that is glued onto and bonded to a PCB test board is shown in Fig. 1. More information about the chip design can be found in [2].

Based upon simulation results, we expect that MZMs with a shallower etch depth and a higher doping concentration will survive higher total ionizing doses (TID) [3]. To experimentally verify these simulation outcomes, some of the chips will be irradiated with x-rays

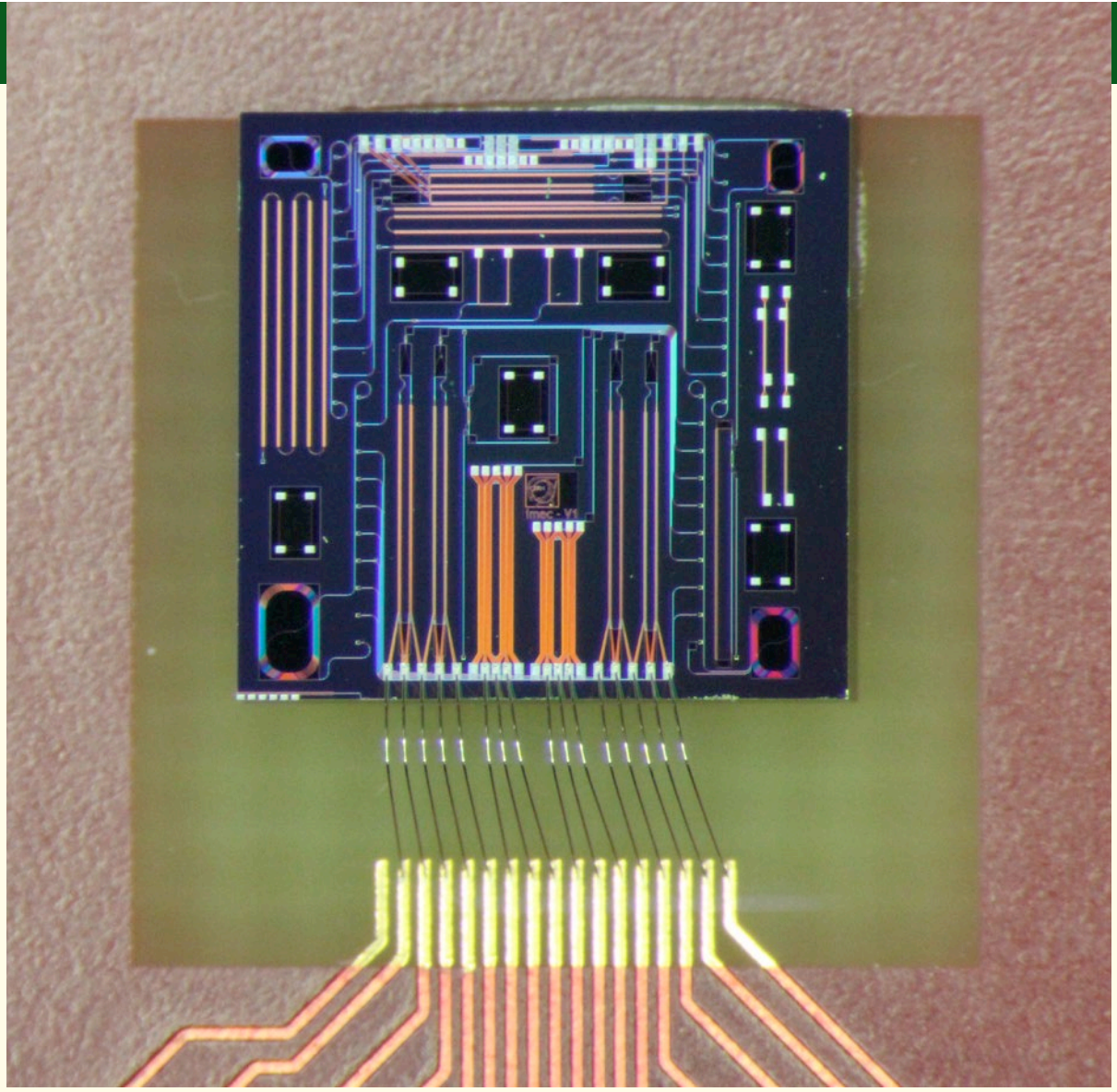

Fig. 1.: Microscope image of the fully fabricated chip glued onto and bonded to a PCB board for testing purposes.

and key performance indicators of the individual components on-chip, e.g. phase shift for MZMs and dark current for PDs, will be measured as a function of TID. The test results will help us to then improve the radiation hardness of future MZM designs and to optimize the simulation procedure.

Why Europractice?

We chose a Europractice-organized Multi Project Wafer (MPW) run for our SiPh prototyping work to access affordable, state-of-the-art fabrication technology. The availability of validated building block devices, a comprehensive PDK and qualified support offered from Europractice played a decisive role in selecting this service.

Acknowledgement

Parts of this work have been funded through the ICE-DIP programme. ICE-DIP is a European Industrial Doctorate project funded by the European Commission's 7th Framework programme Marie Curie Actions under grant PITN-GA-2012-316596.

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SOMBRA: Integrated Switch for Substring Reconfiguration to Optimize PV Panel Power under Partial Shading

Ghent University – imec, CMST

Contact: Pieter Bauwens
E-mail: pieter.bauwens@elis.ugent.be
Technology: On Semi 0.35µ C035-I3T50 – 50V
Design size: 8.74 mm² and 12.87 mm²

Description

The output power of a PV module can drop significantly if there is a current mismatch between the series-connected individual cells. This current mismatch can arise due to differences in temperatures of the cells or simply because of partial shading of the PV panel. The most common solution to this problem is by bypassing those limiting cells (in practice, the entire substring containing them is bypassed) and in doing so, ensuring a higher output power. The problem with this approach is that there might still be a lot of power available in those bypassed cells.

A reconfigurable module topology might be more efficient. In such a topology the connections between the substrings can be rearranged during operation in order to maximize the module power output. For this topology to be effective, a network of very low-ohmic (not exceeding a few mW) switches are needed. This work was dedicated in creating those switches, coping with some challenging design and layout requirements.

Aside from being low-ohmic, at least some of the switches in that topology should be able to block high voltages. The typical current within a PV panel can reach up to 10A, all of which will flow through the switches. Every switch should be uniquely identifiable with an address, and an I²C slave should be present for easy communication with a microcontroller. As most of the switches will have different reference voltages, the communication and voltage supply should be ensured irrespective of their reference voltage.

Results

Figure 1 shows the block diagram of the created chip. The external isolation capacitors separate the internal and external reference voltages. The supply voltage is realized by rectifying an AC signal. The signals for the I²C data communication (SDA, SCL) are cleaned up (Data Rec.) before they are entered into the I²C slave (Data Proc.), which will then control the switch. Data Proc. was created in Verilog and was automatically synthesized and laid out for the I3T50 technology.

Figure 2 shows the results. Two designs were created: a low-voltage version for the full 10A (top), and a high voltage version for 5A (bottom). The LV version (9mm²) has a transistor channel width of 0.8m, resulting in a measured on-resistance of 1.5mW. The HV version (13mm²) has a transistor channel width of 1.6m, resulting in a measured on-resistance of 7.3mW.

Why Europractice?

Having a theory or even simulation of how something might work is one thing. Having something created and actually measured has a tremendous added value. Europractice offers a great means of creating such prototypes at reasonable prices. Together with the packaging service (even for annoyingly large designs with a huge amount of bondpads) a ready to use prototype is provided.

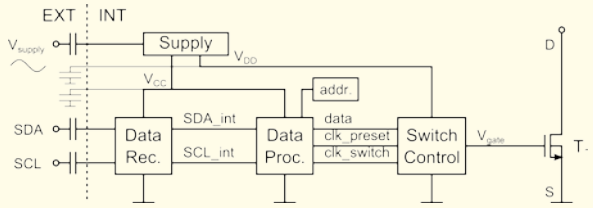


Fig. 1.

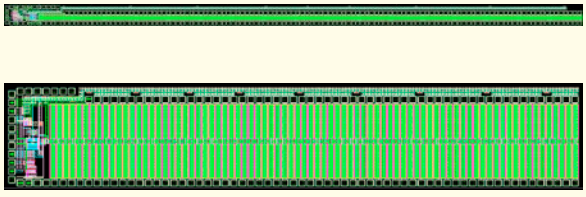
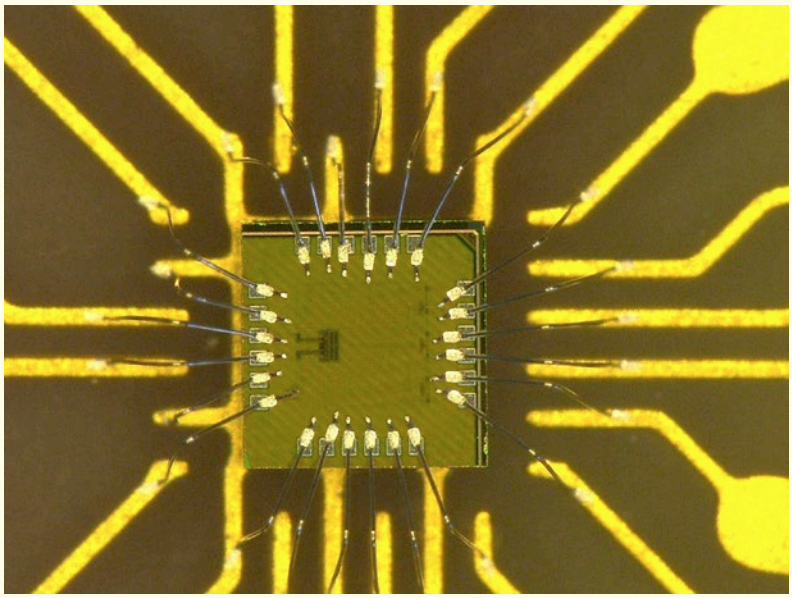


Fig. 2

A highly linear VCO for use in VCO-ADC's

University of Ghent (UGent), Electronics and Information Systems (ELIS) department, Circuit and System (CAS) research group

Contact: Prof. Pieter Rombouts, Amir Babaie-Fishani
E-mail: rombouts@elis.ugent.be, ababaief@elis.ugent.be
Technology: TSMC 65nm 1p9m CMOS, low power flavor
Die size: 1mm x 1mm
Run: 4655 (20 May 2015), Topcell: filterPWM_3rd_orderVCO_2015



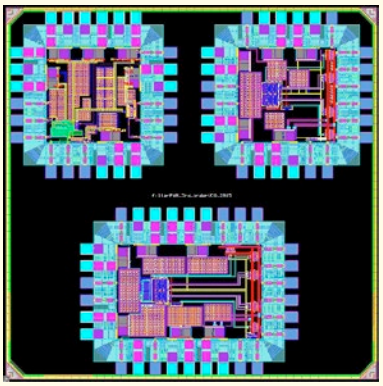
VCO based Analog to Digital conversion has recently gained a lot of interest, because it allows relatively easy implementation of multi-bit noise shaping A/D conversion, be it a closed-loop or an open-loop implementations. However, whichever overall architecture is used, a key issue is the overall linearity of the actual VCO that is used as the quantizer. Most researchers have tried to solve this issue at the architectural level e.g. by calibration, feedback or signal swing reduction.
In this work, we follow a complementary approach, in the sense that we have performed a circuit level optimization of the VCO core. The resulting VCO is typically an order of magnitude more linear than prior VCO designs. As a result further linearity correction at the architectural level may have become unnecessary or can significantly be simplified.

Description

The showcased design is a very simple Ring-Oscillator VCO structure for use in VCO-ADC applications. It has a greatly improved linearity compared to previously published VCO's.
The prototype was implemented in the low power flavor of TSMC 65nm CMOS technology.
This easy-to-implement idea consists of an 18-stage ring oscillator which are biased using a proposed new resistive input stage.

Results

The circuit was designed for a 1V power supply and an oscillation frequency centered around 300MHz.
The measured voltage to frequency conversion curve of the VCO for a rail-to-rail input voltage sweep has a deviation of maximum 2.2MHz over the entire tuning range from 100-to-500MHz, corresponding to 0.6\% of the full scale.
Once used in a pseudo differential configuration (using two parallel VCOs), this VCO-ADC obtained an SNR and SNDR of 71dB and 69dB over a bandwidth of 2MHz, while consuming 0.65mW per VCO. The area for a single VCO is 60 micro-meter in 25 micro-meter. The results obtained with this chip were included in a paper with the title 'A highly linear VCO for use in VCO-ADC's'. The paper has been accepted for publication in electronics letters.



Why Europractice?

Through Europractice, access is provided to state of the art EDA software and numerous CMOS technologies. The MPW runs administered through Europractive provide a regular, predictable and affordable avenue for research and development.

Acknowledgement

This work has been supported by the Fund for Scientific Research Flanders (FWO-Vlaanderen) Belgium.

Worldwide first 24 GHz RFID-Transponder for identification tasks

Fraunhofer IPMS Dresden Germany, Wireless Microsystems Group

Contact: Sascha Lischer, sascha.lischer@ipms.fraunhofer.de
Technology: TSMC 90 nm CMOS Mixed Signal RF Low Power Standard Process
Die size: 2500 x 1500 µm²

Together with industry partners, researchers at the Fraunhofer Institute for Photonic Microsystems (IPMS) have developed a novel RFID system which uses the "Super High Frequency"-Band (SHF). The use of 24 GHz makes it possible to implement very small antennas and to integrate these antennas directly on the chip. With an area of merely 2.5 × 1.5 mm² and a thickness of 150 µm, the tags can be manufactured at low cost and could help in the future to cost-effectively distinguish high-quality mass products such as pharmaceuticals and auto parts as well as ID and credit cards in order to identify stolen property, counterfeit goods or forgeries.

Fraunhofer IPMS Group Leader Hans-Jürgen Holland explains, "Using frequencies out of the SHF band provides the advantage of being able to use very small antennas. At 24 GHz, the free space wavelength is only 1.24 cm. Therefore, it is possible to integrate the antenna directly on the tag as an On-Chip Antenna (OCA). This eliminates the cost of packaging and assembly required by an external antenna and reduces the overall size of a complete RFID-Tag to a few square millimetres."

Reader equipment to interpret serial numbers with which the product to be identified is assigned, has been developed within the project consortium by metraTech GmbH. An electromagnetic field emitted by the reader, carries the energy, which is necessary for the operation of the chip, making a read range of a few millimetres possible. The chip follows a transmission protocol according to the ISO 18000-6c standard, also known as EPC C1G2. To keep production costs low, the system is manufactured in a standard CMOS technology.

The passively operated RFID-Transponder with the integrated antenna can be easily incorporated into several products. Project partners are already busy working to develop and test methods for the rapid and cost-effective integration of RFID-Tags into labels, tickets for public transportation, admission tickets, stickers and smartcards.

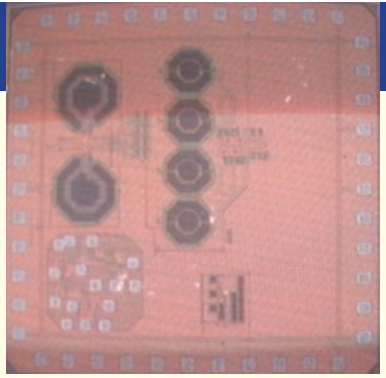
Picture description: "One possible application: identification of drugs via an integrated RFID chip (shown enlarged) for the detection of counterfeits."

Why Europractice?

Europractice gave us the opportunity to produce the chips of this project in a modern technology from the world's largest dedicated independent semiconductor foundry. Due to the use of MPW-runs, we received a sufficient count of chips to be able to do all needed tests at low cost. In addition, the Europractice ASIC Design Support helped us to resolve some unclarities in the Design Documents and to get additional informations from TSMC.

Acknowledgement

This project was funded by the Federal Ministry of Education and Research (BMBF) under grant number 031PT501A. Results of the recently completed project were presented to the professional public for the first time at the Mikrosystemtechnik (MST) Kongress in Karlsruhe (Germany) from 26 - 28 October 2015 and at the IEEE Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS) in Tel Aviv (Israel) from 2-4 November 2015.



Sub-Harmonic Mixer and Low Noise Amplifier for 70-90 GHz single chip solutions

MMIC design groups of Microwaves and Electronics Laboratories, National Technical University of Athens - Institute of Communication & Computer Systems

Contact: Fotis Plessas, Evaggelos Tsimpinos, Rodoula Makri
E-mail: rodia@esd.ntua.gr, fplessas@e-ce.uth.gr, etsimpinos@gmail.com

Technology: TSMC 65nm CMOS LP MS/RF - R4655/2015
Die-Size: 1.920 x 1.920 mm² (*mini***@sic**)

Description

As we move from 2G to 3G/4G there has been an inherent trend of simplifying the radio access network architecture, making it more compact and efficient for offering broadband services to the user. The primary motive is to enable mobile operators to keep low their network costs along with improved coverage and capacity since the demand for bandwidth and data traffic volumes grows rapidly. This calls for compact architectures while reducing power consumption and installation costs of broadband backhaul networks suitable WIMAX, LTE, 4G and wireless PtP communications. The aim of the present implementation is to prove the concept of significantly reducing millimeter-wave radio modems' costs through high degree of integration based on standard CMOS technologies. The corresponding application refers to the mm-wave front-end of a radio system operating in the E-Band (70-90GHz) and supporting GbE speeds for mobile backhauling and future private networks. Our goal is to demonstrate the feasibility of a relevant Si-based 65nm CMOS MMIC exploring the limits of the low power flavor in respect to the required specs.

The developed chip consists of 2 main modules: a sub-harmonic mixer for direct conversion purposes and a Low Noise Amplifier. The LNA consists of a four-stage design. The first stage is a MOS cascode amplifier with inductive source degeneration while 3 additional MOS cascode stages were employed for gain increase. Gain control is achieved via the current bleeding method. Key performance characteristics are: Frequency Range: 81 – 86GHz, Gain: 11dB, Noise Figure: 8.6dB, Input Matching at 50Ω: better than -14dB, Output matching at 50Ω: better than -10dB, Consumption: 36mW (30mA from 1.2V), Linearity: -4.3dBm IIP3, 5.5dBm OIP3, Area: 430um x 500um, Gain Range: Full Gain to 0dB.

Gilbert cell topology has been selected for the core of the 4x subharmonic mixer. In addition, Gilbert cell bottom devices have been replaced by two sets of four transistors being responsible for the generation of the fourth harmonic of the LO signal; this will allow the mixer to operate as a 4x SHM. Input signals of these transistors are octet-phase LO signals, with phases 0°, 90°, 180°, and 270° applied on the gates of one set, and phases 45°, 135°, 225°, 315° applied on the other set. These signals are internally generated using 45° phase shifters where a mechanism that controls and/or corrects the value of the phase produced has been added. Key performance characteristics are summarized as follows: P1dB: 8dB, Conversion Gain: -2dB, Input Matching at 50Ω: better than -11dB, Linearity: -6dBm IIP3, 12dBm IIP2, Port-to-Port Isolation: 30dB RF-LO, 66dB LO-RF, 28dB RF-IF, 63dB LO-IF, Area: 1mm x 1mm. A bandgap has also been included.

The whole implementation will lead to a radio chipset for proof of concept of the integrated RF functions, paving the way for fewer system components, smaller size and higher level of integration resulting in lowering the design complexity and cost of future applications in backhaul networks.

Why Europractice?

The National Technical University of Athens through its RFIC design groups is an active member of Europractice. Apart from the easy access to design tools and modern technologies, Europractice provides a unique possibility to obtain rapid and frequent prototyping of cutting edge silicon technologies in affordable prices along with high standards services, enabling experimentation on IC research designs at high frequencies and in nm-scale CMOS technologies. By this way it provides us the opportunity of creating an IP portfolio and scientific excellence leading to high innovation and enhancing our research capabilities.

Acknowledgment

The work has been co-financed by Hellenic Funds and by the European Regional Development Fund (ERDF) under the Hellenic National Strategic Reference Framework (NSRF / ESPA 2007 – 2013) in the framework of the research project 11SYN_6_100 entitled "EMOSIC: An E-band / mm-wave CMOS RFIC/MMIC implementation for future private networks and mobile backhaul radio applications", funded under the operational programme "Cooperation 2011" of MIA-RTDI / GSRT.

Pixel detector front-end for the experiment upgrades at the HL-LHC

Dept. of Electrical, Computer and Biomedical Engineering, University of Pavia, Via Ferrata 5, 27100 Pavia, Italy

Contact: Lodovico Ratti
Technology: TSMC 65N CMN65 LP
Die size: 2mm x 2mm (*mini***@sic** option)

Why Europractice?

In order to pursue frontier research and innovation, access to microelectronic technologies is of paramount importance for the academy. It is well known that the price of a mask set for engineering production is typically quite high (at least in comparison with the standard budget of a university research group). Multi project runs, with several customers sharing silicon and costs, become the most convenient solution for small circuit production or prototyping. Europractice enable the use of advanced CMOS technologies at a cost within reach of European research teams. In particular, with the *mini***@sic** option made available by Europractice (which was exploited in the case presented here), it is possible to override the minimum area (and minimum price) rule (i.e., under a given silicon area A, the price is the same as for A) commonly set by other brokers.

Introduction

In the upgraded version of the Large Hadron Collider (LHC), the so called High-Luminosity (HL) LHC, the instantaneous luminosity will be pushed to the unprecedented level of 5×10^{34} cm^{-2} s^{-1}, i.e., 5 times the present nominal one. This will result in a set of severe requirements for the tracking pixel detectors in the HL-LHC experiment upgrades, especially for the layers closer to the interaction points. Improved accuracy in momentum measurement will be achieved by increasing the granularity of the detector, down to a pixel size of 50 um x 50 um (or 25 um x 100 um) in the inner layers. In order to minimize the material budget and the complexity of the cooling system, the power dissipation will have to be kept around 0.5 W/cm^2 or below at hit rates in the order of 2 GHz/cm^2. Such a high rate will impact on the bandwidth requirements for the readout circuits, boosting the design efforts to include as much intelligence as possible in the elementary pixel front-end (FE) channel and reduce the amount of data to be transferred off chip. The foreseen growth in luminosity will also lead to a remarkable increase of the radiation levels. The front-end circuits will have to ensure reliable operation in a harsh radiation environment, with a predicted total ionising dose of 10 MGy and a 1 MeV neutron equivalent fluence of 2×10^{16} cm^{-2} accumulated during their lifetime. With respect to the present pixel detector systems, where 300 um is the typical thickness of the sensor substrate, thinner detectors are being proposed for the so called phase II experiment upgrades to reduce multiple scattering effects and improve radiation tolerance. This will lead to smaller signals, which in turn will tighten up the requirements on the noise performance of the analog front-end electronics. Actually, in order to preserve the detection efficiency, operation of the readout channel at relatively low thresholds, around 1000 electrons or lower, has to be envisioned, setting the equivalent noise charge (ENC) limit to about 140 electrons. The design of a new pixel readout chip complying with the above specifications is being tackled in the framework of the RD53 Collaboration using a 65 nm CMOS technology. The CHIPIX65 project, funded by the Italian Institute for Nuclear Physics (INFN), is contributing to the design effort led by the RD53 consortium with the development of several building blocks, including a couple of options for the very front-end channel to be bump-bonded to the pixel sensor. Both versions of the channel, together with other functional blocks, have been integrated in a Europractice *mini***@sic** run in a 65 nm CMOS technology. Following is a description of the main design features and per-

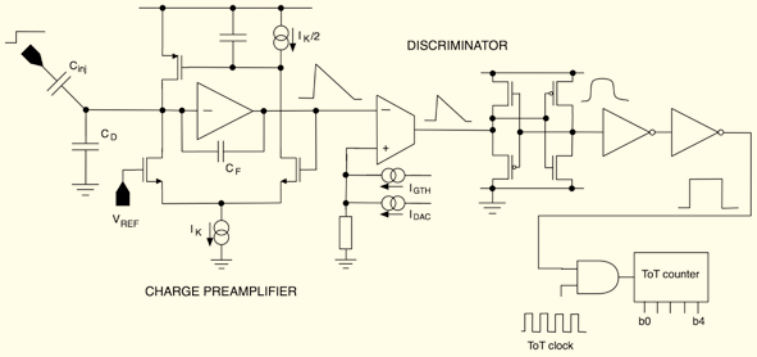


Fig. 1. Block diagram of the asynchronous very front-end channel.

formance of one of the proposed solutions, based on a Krummenacher network for the continuous reset of the charge sensitive amplifier, or CSA, and on a fast discriminator with locally adjustable threshold voltage. This solution is designated as asynchronous, as opposed to the other one developed in the frame of the same CHIPIX65 collaboration, based on the synchronous operation of a comparator with offset cancellation.

Circuit description

A block diagram of the asynchronous readout channel is shown in Fig. 1. The signal from the sensor is converted to a voltage by means of a charge sensitive amplifier, continuously reset, as already mentioned, through a Krummenacher stage. The Krummenacher architecture was specifically chosen for its capability to compensate for the detector leakage current, which is expected to increase significantly during the experiment. The signal at the preamplifier output is fed to a threshold discriminator, turning the signal amplitude into a time interval or ToT, time over threshold. The threshold discriminator is based on a low power transimpedance amplifier for fast switching operation. Given the triangular shape of the preamplifier response, featuring a very fast leading edge and a return to baseline with a constant slope, a linear relationship between amplitude (or input charge) and ToT is expected. The threshold discriminator output is used as a gate signal (through the AND gate) for the ToT clock, which is fed to the 5 bit ToT counter for time-to-digital conversion. The current IGTH is used for chip-wide threshold configuration and is set by circuits located in the chip periphery. Channel to channel dispersion of the threshold voltage is addressed by means of a local circuit for threshold adjustment, based on a 4-bit binary weighted DAC, which generates the current IDAC adding to IGTH. The power consumption per channel (not including the dynamic power dissipation of the AND gate and the counter in Fig. 1) is slightly smaller than 5 uW (about 4 uA at VDD=1.2 V). The front-end was designed to comply with a maximum input signal of 30000 electrons. With a current I_K=12.5 nA in the Krummenacher network and a

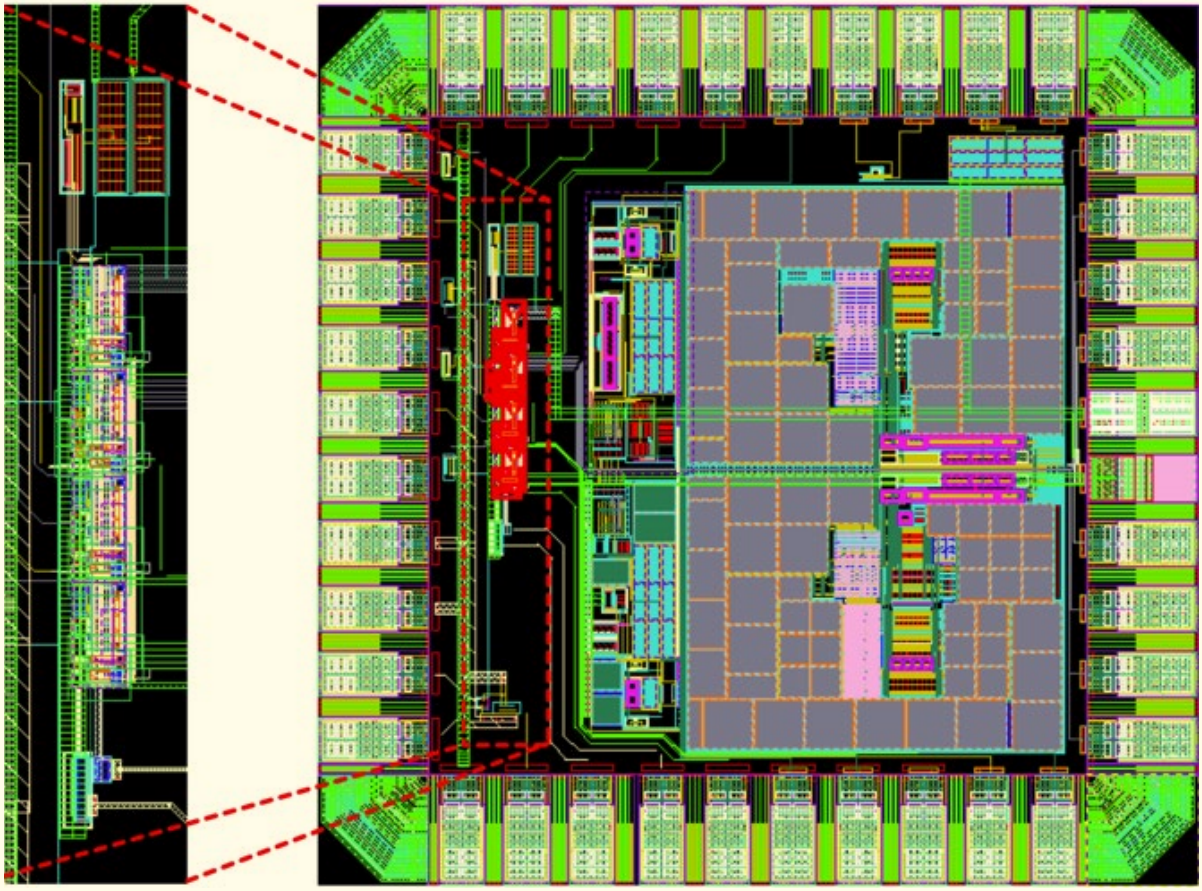


Fig. 2. Layout of the chip region including the two slightly different versions of the very front-end. A close-up view of the prototypes layout is also shown.

preamplifier feedback capacitance of about 10 fF, the maximum expected ToT is 400 ns. Therefore, a 40 MHz ToT clock is necessary to take advantage of a 5-bit dual edge (i.e., sensitive to both the rising and the falling edge of the clock) counter, to be included in the readout channel. Note that a clock with virtually the same frequency is provided by the LHC machine, where the bunch crossing rate is only slightly different from 40 MHz.

Short summary of the simulation results

The simulated circuit featured an output dynamic range around 450 mV, a charge sensitivity of about 15 mV/ ke^- and an equivalent noise charge of 114 electrons rms for a detector capacitance C_D=100 fF. A time walk not exceeding 25 ns was achieved with a threshold of 700 electrons and signals of 1000 electrons or larger.

Results from the prototype characterization

Fig. 2 shows the layout of the region accommodating the prototype structures of the asynchronous FE (AFE), not including the ToT counter. This region is just one quarter of a 2 mm x 2 mm *mini***@sic** chip. In the AFE, for the design of the preamplifier two different options were investigated: one where the feedback capacitor is implemented with a metal-insulator-metal (MIM) structure and one where a PMOS in an inversion mode configuration is used instead. A few programming bits can be used to set

- the charge sensitivity G (1 bit); this is obtained by changing the preamplifier feedback capacitance C_F, which can assume two alternative values, 10 or 20 fF, resulting in G=15 mV/ke^- or 7.5 mV/ ke^- respectively;
- the recovery time, or the slope of the falling edge of the signal (1 bit); this is obtained by varying the current I_K in the Krummenacher stage, which can assume two alternative values, 25 nA or 50 nA;
- the detector emulating capacitance C_D at the preamplifier input (2 bits); C_D can be made to vary from 0 to 150 fF in steps of 50 fF.

In the preamplifier test structures, a 30 fF injection capacitance C_{inj} connected to input terminal is used to test the stage response to a charge signal.

Fig. 3 shows the response of a charge preamplifier with a MOS capacitor in the feedback network to a 10^4 electron signal for the four different possible combinations of the charge sensitivity (low and high G) and of the recovery current (low and high I_K). The waveforms where obtained with a detector emulating capacitance C_D at the preamplifier input of 100 fF. The capacitance C^*_D referred to in Fig. 2 (and in the subsequent ones) also includes the contribution from the injection capacitance (which, as a part of the injection test system, has to be taken into account during the channel response and charge sensitivity measurements). Among the different possible settings of the charge preamplifier, the one with high gain and low recovery current is considered as the standard configuration. These are actually the charge sensitivity and recovery current values through which both the ToT range of 400 ns (corresponding to five 1's at the counter output) and the

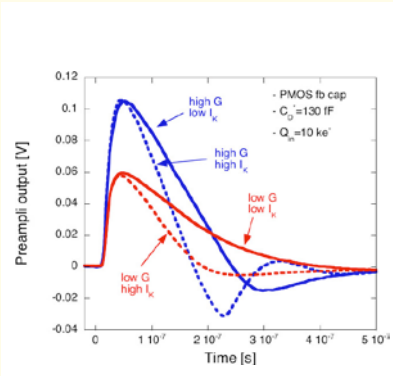


Fig. 3. Response of a charge preamplifier with a MOS capacitor in the feedback network to a 10^4 electron signal for the four different possible combinations of the charge sensitivity (low and high G) and of the recovery current (low and high I_K).

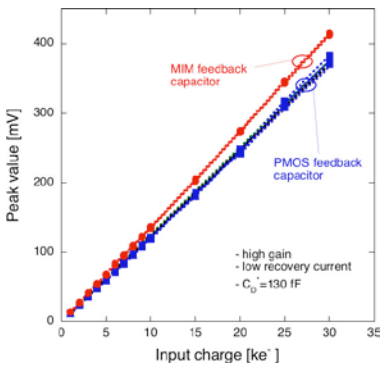


Fig. 4. Peak response of the charge preamplifier as a function of the input charge for the two versions of the stage. Each set of curves includes the results from the characterization of four different samples.

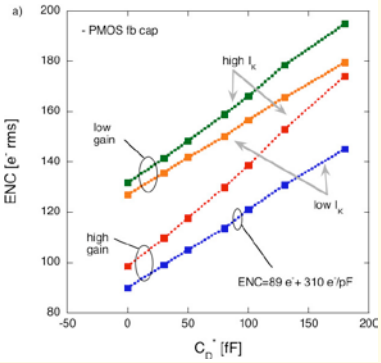


Fig. 5. Equivalent noise charge as a function of C^*_D for four different possible settings of the charge preamplifier:
a) CSA with PMOS capacitor in the feedback network and ...

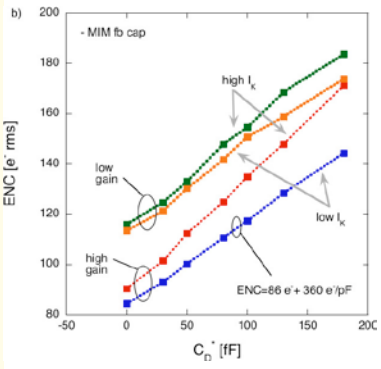
output dynamic range of 450 mV are simultaneously covered with an input rang of 3 x 10^4 electrons.

Fig. 4 shows the peak amplitude in the response of the charge sensitive amplifier as a function of the input charge Q_{in} for the two versions of the stage and for a detector emulating capacitance of 100 fF (C^*_D=130 fF). Each of the two sets of curves includes results from the characterization of four samples. In both cases, the dispersion in the curve slope, i.e., in the charge sensitivity, is quite small, the standard deviation being less than 1% of the average value in the case of the MIM feedback capacitor and about 1% in the case of the stage with the PMOS transistor in the feedback network. This result is quite in good agreement with the models provided by the foundry, predicting a larger (though limited) channel to channel dispersion in the gain for the CSA version with PMOS capacitor when process parameter variations are not included in the Monte Carlo simulations. In both cases, the charge sensitivity is smaller than the design one: about 13.7 mV/ke$^-$ for the CSA with MIM capacitor, about 12.4 mV/ ke$^-$ for the one with the PMOS capacitor. The non-linearity, estimated by means of the endpoint line approach, was found to be fairly low in both variants of the preamplifier: less than 4% for the one using the PMOS transistor, less than 3% for the other CSA version.

The equivalent noise charge (ENC) as a function of C^*_D is shown in Fig. 5 a) and b) for the CSA with PMOS capacitor in the feedback network and for the CSA with MIM capacitor respectively. The performance of the two preamplifier versions were also studied in the four possible combinations of the gain and recovery current settings. The main noise sources are located in the input transistor of the charge preamplifier, which is responsible for the series contribution to the ENC, and in the Krummenacher feedback network, mostly accounting for the parallel contribution. Not surprisingly, increasing the recovery current leads to an increase in the ENC due to the growth in the parallel noise contribution from the Krummenacher stage. Also, switching from the high to the low gain configuration has a detrimental impact on the noise behavior. For both the preamplifier variants, the high gain/low recovery current configuration results in the best ENC performance, with an equivalent noise charge of about 120 electrons rms at C^*_D=100 fF. It is worth noticing that, with this gain and IK current setting, the dENC/dCD slope in the CSA with MIM feedback capacitor, 360 e$^-$/pF, is about 20% larger than in the PMOS feedback capacitor case, where the slope is 310 e$^-$/pF.

Fig. 6 shows the signal at the discriminator output as a response to an input signal of 10000 electrons, obtained with a threshold of 800 electrons in a channel using a MIM capacitor in the preamplifier feedback network. The figure also shows the signal at the output of the charge preamplifier and fed to the discriminator input. The rise and fall times in the discriminator response are shorter than 5 ns when the input signal exceeds the threshold of at least 200 electrons.

In Fig. 7, the time over threshold is displayed as a function of the charge for the same channel as in Fig. 6. Here the ToT is measured directly at the discriminator output as the duration of the discriminator response. The ToT vs Q_{in} features a good linearity for charge values larger than 2000 electrons.



... b) CSA with MIM capacitor.

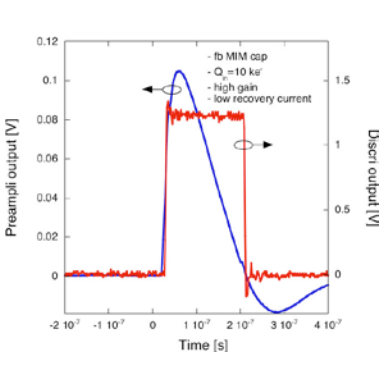


Fig. 6. Response of the discriminator to a 10 ke$^-$ electron signal with a threshold set to 800 electrons. The signal at the output of the charge preamplifier is also shown.

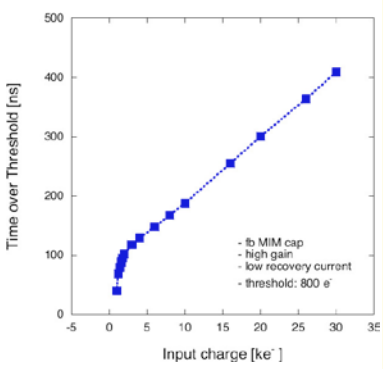


Fig. 7. Time over threshold as a function of the input charge. The ToT is measured directly at the output of the discriminator as the duration of the discriminator response.

Radiation Tolerant Library for XFAB 180nm CMOS

Avionic Systems Division, NASA Johnson Space Center, Houston, TX 77058

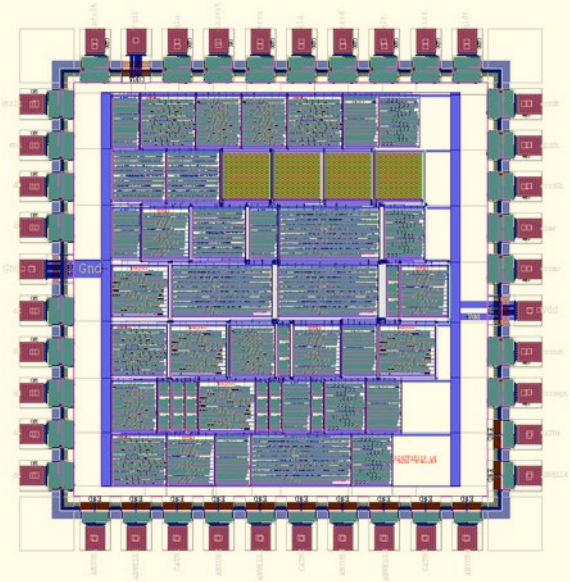
Contact: Robert L. Shuler
E-mail: robert.l.shuler@nasa.gov or robert@mc1soft.com

XFAB is a widely used specialty fab with many process variations supporting high voltage, high temperature, various types of sensors, and non-volatile memory. These features might find application in spacecraft and robotic space systems and instruments. To make effective use of the process in such cases, radiation tolerant digital circuits are needed for processing and control. In this project an existing general purpose highly compact digital Radiation Hardened by Design (RHBD) cell library was implemented, along with radiation tolerant input-output pad buffers, and test circuits for validation. The library allows implementation of a variety of common RHBD techniques for tolerating Single Event Transients (SET) and avoiding latch-up. We did not consider total dose, which at 180 nm is usually already acceptable for the levels of radiation expected on manned missions, and a good may more besides.

Description

The base library used was NASA JSC's "ten cell library" which is described in some detail in a recent paper.[1] The small number of cells provides easy porting, and is designed for routing efficiency. Horizontal guard bars between P and N regions provide latch up protection and additional spacing for reduction of multi-node SETs. This space also accommodates an internal routing channel adequate for some combination cells such as AND and OR. The N and P guard bars are closed off on the end of rows by a ROW_CAP cell, which can be placed by a script. The XFAB supplied PDK for Tanner Tools was used, though the cells can be exported via GDS to other tool chains.

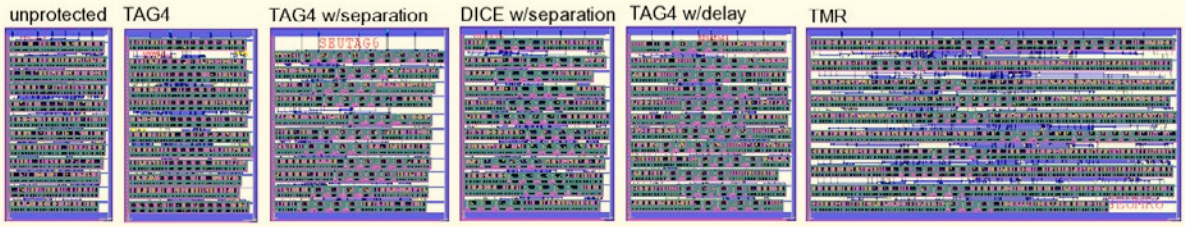
The RHBD techniques supported include single or dual rail, the Transition And Gate (TAG) (or Guard Gate), and several types of Dual Interlocked Cells (DICE, TAG4), with a 0.2 nanosecond delay cell that can be used in multiples for the degree of SET suppression desired on a second interlocked input. The interlocked latch base cells are half a latch, such that critical node pairs are split between base cells. Versions with 1 micron extra spatial separation are provided for critical applications. Conventional latches and flip flops are also included for comparison. A single base cell is used for mux, conventional latch, and XOR. A full set of NAND, inverter, buffer gates are provided, with one variation of tri-state gate which is also used for the guard gate. Due to the need for balanced rise and fall times for good SET suppression only a 2-input NOR gate is provided, with greater inputs constructed using multiple cells. The logic cells use a method of unified design rules and also pass DRC check for the UMC 180 nm process (requires switching base cells for via and contact).



Hierarchical routing of XFAB 180 nm RHBD test chip, with pad ring

The pad cells include ground, corners, core and pad-ring Vdd, and a bi-directional buffered pad from which fixed-direction input and output pads are derived. The buffered pads support 1.8, 2.5 or 3.3 volt input-output and have an effective generic ESD design which was effective under stress in bench testing. The buffers have 5x input and output force-voted redundancy.

The test circuit used included for each RHBD technique 48 flip flops in two strings wired for toggling with a logic cloud that represented a bit-slice of an ALU with an input MUX, in other words, typical processor and control circuitry. An XOR checks for differences between the strings, and an error injection circuit allows the test rig to be debugged during bench testing. Each test circuit has an on-chip triple modular redundant (TMR) supervisor circuit that reports errors and resets the circuit. There is also an on-chip programmable ring oscillator to verify simulation timing and provide high on-chip clock rates for SET stress testing. A triple modular redundant (TMR) test circuit was also included for comparison with the RHBD circuits.



Test circuit area comparison for RHBD techniques implemented with the 10-cell library

A hierarchical block routing technique was used which allowed very fast routing for prototyping, yet reasonable area efficiency. One quarter of each test circuit was auto-routed into a block. he control circuit and clock circuits were each auto-routed into a block. Then the router was switched to use these blocks as standard cells and the entire chip built. This co-locates similar circuitry and avoids a time consuming all-in-one routing approach. See figures for illustration.

Results

The circuits all performed as expected, with input-output pads functioning robustly through 170 MHz in a protoboard setup and somewhat above that with a custom circuit board. Conventional and TMR test circuits functioned at 200 MHz (note that this includes the mux and ALU time, not just flip flop toggles) and the interlocked RHBD versions without delays functioned at 110 MHz, and with a 1 ns delay at 66 MHz. We expect based on tests of similar technology an SET threshold of from 20 to 80 LET with the higher numbers for the slower circuits (or larger in the case of TMR). Heavy ion testing for this particular chip is still pending budget allocation. A limited supply of test chips can be made available to interested parties wishing to accelerate the testing process.

Why Europractice?

This was our first use of Europractice. Not being a European institution we were not able to take advantage of all facilities, such as design tools. However, the flexibility with respect to R&D scale pricing (*mini***@sic**'s) on processes of interest along with the excellent support provided by Europractice personnel, as well as billing flexibility have convinced us to give Europractice primary consideration in the future.

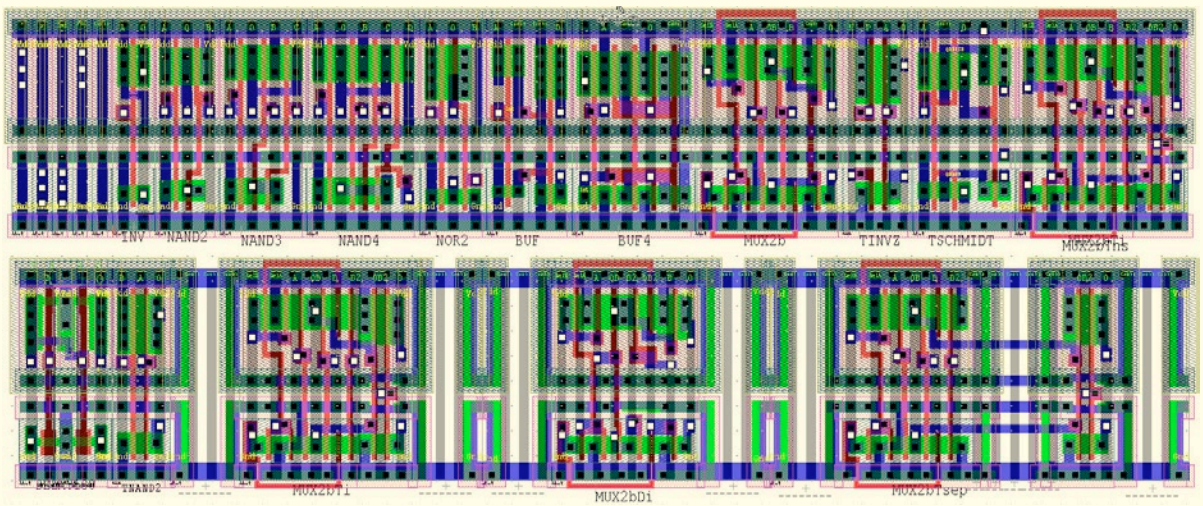
Acknowledgement

Support was provided by Indus Instruments, Houston, TX.

References

[1] R.L. Shuler, "Porting and Scaling Strategies for Nanoscale CMOS RHBD," IEEE Transactions on Circuits and Systems, 62, 12, 2856-2863 (2015).

The 10-cell base library (upper), plus special RHBD latches with extra critical node separation



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La Trobe University	Bundoora, Victoria	3
Macquarie University	Sydney	3
Monash University	Clayton	12
Motorola Australian Ressearch Centre	Botany	1
Royal Melbourne Institute of Technology (RMIT)	Victoria	1
University of Adelaide	Adelaide	1
University of Melbourne	Melbourne	1
University of New South Wales	Sydney	12
University of Sydney	Sydney	8
University of Western Australia	Crawley	1
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austriamicrosystems	Unterpremstaetten	74
Austrian Academy of Sciences	Wiener Neustadt	1
Austrian Aerospace	Vienna	2
Austrian Institute of Technology - AIT	Vienna	1
Carinthia Tech Institute	Villach-St.Magdalen	1
Fachhochschule Technokum Kaernten	Villach-St.Magdalen	7
FH Joanneum Graz	Graz	1
IEG	Stockerau	1
Johannes Keppler University	Linz	3
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Riegl Laser Measurement System	Horn	4
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TU Graz	Graz	4
TU Wien	Vienna	22
University of Applied Sciences Technikum Wien	Vienna	1

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Browning International SA	Herstal	1
Caeleste	Antwerp	1
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ED&A	Kapellen	3
EqcoLogic	Brussels	52
FillFactory	Mechelen	2
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IMEC	Leuven	220
K.U. Leuven	Heverlee	162
Katholieke Hogeschool Brugge-Oostende	Oostende	23
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KHLim	Diepenbeek	9
KIHA	Hoboken	2
Macq Electronique	Brussel	1
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UNESP/FE-G	Guaratingueta - SP	4
UNICAMP- University of Campinas	Campinas, SP	34
Universidade de Sao Paulo	Sao Paulo-SP	33
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Epic Biosonics	Victoria	4
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TeraXion	Québec	1
University of Alberta	Edmonton	1
University of Toronto	Toronto	1
University of Waterloo	Waterloo	6
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CETC38	Heifei	11
Chinese Academy of Science, Institute of Semiconductors	Beijing	1
Chongqing University	Chongqing	1
Dept.Computer Science and Technology	Beijing	1
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Hirain	Beijing	1
Hong Kong University of Science and Technology	Hong Kong	36
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Peking University	Beijing	1
Shanghai Exceleration Semiconductor Ltd.	Shanghai	1
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The Chinese University of Hong Kong	Shatin-Hong Kong	47
Tsinghua University	Beijing	5
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Aarhus University	Aarhus	2
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Nokia Networks	Espoo	2
Tampere University of Technology	Tampere	8
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ELA Recherche	Meylan	4
ENSEA	Cergy Pontoise	2
ENST Paris	Paris	2
ESIEE	Noisy Le Grand	3
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Institut des Sciences Nucleaires	Grenoble	5
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Fachhochschule Aschaffenburg	Aschaffenburg	3
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Fachhochschule Wilhelmshaven	Wilhelmshaven	1
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Trias	Krefeld	1
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TU Chemnitz	Chemnitz	12
TU Darmstadt	Darmstadt	19
TU Dresden	Dresden	34
TU Hamburg-Harburg	Hamburg	60
Universitaet Dortmund	Dortmund	2
Universitaet Duisburg - Essen	Duisburg	3
Universitaet Giessen	Giessen	1
Universitaet Hannover	Hannover	14
Universitaet Kaiserslautern	Kaiserslautern	22
Universitaet Paderborn	Paderborn	32
Universität Rostock	Rostock	8
University of Bielefeld	Bielefeld	1
University of Bonn	Bonn	13
University of Bremen	Bremen	41
University of Erlangen-Nuernberg	Erlangen	52
University of Freiburg	Freiburg	11
University of Hamburg, HAW - Applied Sciences	Hamburg	2
University of Heidelberg	Heidelberg	105
University of Kassel	Kassel	5
University of Magdeburg	Magdeburg	13
University of Mannheim	Mannheim	36
University of Munich	Munich	1
University of Oldenburg	Oldenburg	1
University of Saarland	Saarbruecken	4
University of Siegen	Siegen	21
University of Stuttgart	Stuttgart	15
University of Ulm	Ulm	65
University of Wuppertal	Wuppertal	2
Vishay semiconductor	Heilbronn	2
Wellhoeffer	Schwarzenbruck	2
Work Microwave GmbH	Holzkirchen	1
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ACE Power Electronics LTD	AG Dimitrios	1
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Found. for Research and Techn.-Hellas	Heraklion	1
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Hellenic Semiconductor Applications	Athens	2
InAccess	Athens	1
Intracom	Paiania	1
National Tech. Univ. of Athens	Athens	19
NCSR	Athens	23
NTNU	n/a	2
RETECO LTD.	Athens	1
Technical University of Crete	Crete	1
Technological Educational Institute of Chalkis	Chalkis	4
Unibrain SA	Athens	1
University of Athens	Athens	1
University of IONNINA	Ioannina	2
University of Patras - VLSI Laboratory	Rio - Patras	24
Hungary		
Hungarian Academy and Science	Budapest	2
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Computer and Automation Inst.	Budapest	6
JATE University	Szeged	1
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Birla Institute of Technology and Science	Pilani	1
CEERI	Pilani	12
College of Eng. Guindy Anna Univesity	Chennai	2
Concept2Silicon Systems	Bangalore	1
Electronics Corporation of India	Mumbai	23
imec India	Bangalore	4
Indian Institute of Science	Bangalore	32
Indian Institute of Science	New Dehli	13
Indian Institute of Technology - Bombay	Mumbai	29
Indian Institute of Technology - Gandhinagar	Gandhinagar	1
Indian Institute of Technology - Hyderabad	Hyderabad	9

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International Institute of Info. Technology	Hyderabad	1
National Institute of Science and Technology	Odisha	1
National Institute of Technology Trichirappalli	Trichirappalli	4
National Institute of Technology Warangal	Warangal	1
National Institute of Technology, Hyderabad	Hyderabad	5
National Institute of Technology, Karnataka	Surathkal	1
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TIFR	Colaba	1
VECC	Kolkata	6
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Cork Institute of Technology	Cork	4
Duolog LtD	Dublin	2
National University of Ireland	Kildare	3
Farran Technology	Ballincollig	1
Tyndall National Institute	Cork	23
Parthus Technologies (SSL)	Cork	7
TELTEC	Cork	1
University College Cork	Cork	15
University of Limerick	Limerick	17
Waterford Institute of Technology	Waterford	8
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Bar Ilan University	Ramat Gan	1
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BIOTRONIC SRL	San Benedetto	1
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IIT Istituto Italiano di Tecnologica - Torino	Torino	6
INFN Bari	Bari	1
INFN Bologna	Bologna	1
INFN Cagliari	Cagliari	5
INFN Catania	Catania	15
INFN Ferrara	Ferrara	1
INFN Genova	Genova	2
INFN Milano	Milano	14
INFN Padova	Padova	4
INFN Pavia	Pavia	4
INFN Pisa	Pisa	3
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ISE	Vecchiano	1
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LABEN S.p.A.	Vimodrone (MI)	3
Microgate S.r.L	Bolzano	6
Microtest	Altopascio	1
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Optoelettronica Italia	Terlago	1
Politecnico di Bari	Bari	10
Politecnico di Milano	Milano	152
Politecnico di Torino	Torino	10
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SYEL S.r.l.	Pontadera	1
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Università degli Studi di Ancona	Ancona	4
Universita degli Studi di Firenze	Firenze	3
Universita della Calabria	Arcavacata di Rende	3
Universita di Cagliari	Cagliari	25
Universita di Catania	Catania	38
University of Bologna	Bologna	32
University of Brescia	Brescia	12
University of Genova	Genova	15
University of Milano-Bicocca	Milano	13
University of Modena and Regio Emilia	Modena	4
University of Naples	Napoli	7
University of Padova	Padova	30
University of Parma	Parma	13
University of Pavia	Pavia	20
University of Perugia	Perugia	7
University of Pisa	Pisa	32
University of Rome La Sapienza	Roma	2
University of Rome Tor Vergata	Roma	10
University of Salento	Lecce	7
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Hokkaido University	Sapporo	24
Kobe University	Kobe	9
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Macam Co., Ltd	Seoul	2
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Radtek	Yusung-Ku, Daejeon	1
Samsung Advanced Institute of Technology	Yongin-si Gyeonggi-do	5
Samsung Electro-Mechanics	Suwon	1
Seoul National University	Seoul	13
Seloco	Seoul	56
SoC8611	Gyeonggi-do	3
SML	Seoul	7
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American university of Beirut	Beirut	1
Lithuana		
Center for Physical Sciences and Technology	Vilnius	1
Kaunas University of Technology	Kaunas	1
Vilnius University	Vilnius	2
Malaysia		
MIMOS	Kuala Lumpur	1
SunSem Sdn. Bhd.	Kuala Lumpur	1
University of Technology	Skudai	1
Malta		
University Of Malta	Msida	16
Mexico		
INAOE	Puebla	34
Universidad Autonoma de Baja California	Tijuana	1
Universidad Autonoma de Puebla	Puebla	1
Netherlands		
Aemics	Hengolo	8
ASTRON	Dwingeloo	1
Catena Microelectronics BV	Delft	1
Cavendish Kinetics	's Hertogenbosch	1
Delft University of Technology	Delft	201
ESA - ESTEC	AG Noordwijk ZH	7
GreenPeak Technology	Utrecht	12
Hogeschool Heerlen	Heerlen	1
IMEC-NL	Eindhoven	61
Intrinsic-ID	Eindhoven	1
Lucent Technologies Nederland BV	Huizen	1
Mesa Research Institute	Twente	6
NFRA	Dwingeloo	1
Nikhef	Amsterdam	5

CUSTOMER	TOWN	Number of ASICs
Smart Telecom Solutions		1
Sonion	Amsterdam	3
SRON	Utrecht	14
Technische Universiteit Eindhoven	Eindhoven	54
TNO - Delft	Delft	1
TNO - FEL	The Hague	18
TNO Industrie	Eindhoven	1
University of Amsterdam	Amsterdam	1
University of Twente	Enschede	5
Xensor Integration	Delfgauw	3
New Zealand		
Industrial Research Ltd	Lower Hutt	4
Massey University	Albany	1
University of Auckland	Auckland	1
Norway		
AME As	Horten	1
IDE AS	Oslo	2
Interon	Asker	21
Nordic VLSI	Trondheim	38
Norwegian Institute of Technology	Trondheim	22
Novelda	Oslo	1
Nygon	Asker	3
SINTEF	Trondheim	19
University of Bergen	Bergen	6
University of Oslo	Oslo	97
Vestfold University College	Tonsberg	2
Pakistan		
NUST	Islamabad	1
Poland		
AGH University of Science and Technology	Krakow	101
Institute of Electron Technology	Warsaw	53
Military University of Technology	Warsaw	3
Technical University of Gdansk	Gdansk	12
Technical University of Lodz	Lodz	10
University of Mining and Metallurgy	Krakow	24
University of Technology - Poznan	Poznan	2
University of Technology & Agriculture	Bydgoszcz	1
Warsaw University of Technology	Warsaw	33
Wroclaw University of Technology	Wroclaw	1
Portugal		
Acacia Semiconductor	Lisboa	6
Chipidea	Oeiras	22
INESC	Lisboa	44
INETI	Lisboa	1
Instituto de Telecomunicacoes	Lisboa	36
Instituto Superior Tecnico	Lisboa	6
International Iberian Nanotechnology Laboratory	Braga	1
ISEL-IPL	LIsboa	1
PETsys	Oeiras	1
Universidade de Aveiro	Aveiro	19
Universidade Nova de Lisboa - Uninova	Caparica	15

CUSTOMER	TOWN	Number of ASICs
University of Minho	Guimaraes	11
University of Porto	Porto	20
University of Tras-os-Montes e Alto	Vila Real	3
Puerto Rico		
University of Puerto Rico	Mayaguez	1
Romania		
Gheorghe Asachi Technical University of Iasi	Iasi	1
National Inst. for Physics and Nuclear Engineering	Bucharest	2
Polytechnic inst. Bucharest	Bucharest	2
Russia		
Budker Institute of Nuclear Physics	Novosibirsdk	4
IPMCE	Moscow	3
JSC "NTLAB"	Moscow	2
Moscow Engineering Physics Institute	Moscow	20
Moscow Institute of Electronic Technology	Moscow	5
Moscow Institute of Physics and Technology	Moscow	5
N.I. Lobachevsky State Univ	Nizhni Novgorod	8
SRIET-SMS CJSC	Voronezh	6
TUSUR university	Tomsk	2
University St Petersburg	St Petersburg	6
Vladimir State university	Vladimir	1
Saudi Arabia		
King Abdullah University of Science and Technology	Thuwal	11
King Saud University	Riyadh	1
Serbia and Montenegro		
University of Novi Sad	Novi Sad	3
University of Nis	Nis	2
Singapore		
Agilent	Singapore	2
DSO National Laboratories	Singapore	6
Nanyang Technology University	Singapore	7
National University of Singapore	Singapore	5
Slovakia		
Inst. of Computer Systems	Bratislava	1
Slovak University of Technology	Bratislava	5
Slovenia		
Iskraemeco d.d.	Kranj	19
NOVOPAS	Maribor	1
University of Ljubljana	Ljubljana	8
University of Maribor	Maribor	1
South Africa		
CSIR Material Science and Manufacturing	Pretoria	1
Solid State Technology	Pretoria	8
University of Pretoria	Pretoria	41
South America		
CNM/Iberchip		74

CUSTOMER	TOWN	Number of ASICs
Spain		
Acorde S.A.	Santander	30
Anafocus	Sevilla	2
Arquimea Ingenieria	Madrid	4
CIEMAT	Madrid	2
CNM	Bellaterra	91
Design of Systems on Silicon	Paterna	7
EUSS	Barcelona	1
Facultad de Informática UPV/EHU	San Sebastián	2
Oncovision	Valencia	2
Technical University of Madrid	Madrid	3
Universidad Autonoma de Barcelona	Barcelona	25
Universidad Carlos III Madrid	Madrid	1
Universidad de Cantabria	Santander	37
Universidad de Extremadura	Badajoz	30
Universidad de Las Palmas Gran Canaria	Las Palmas de Gran Canaria	24
Universidad de Navarra	San Sebastian	36
Universidad de Santiago de Compostela	Santiago de Compostela	3
Universidad del Pais Vasco	Bilbao	3
Universidad Politecnica de Cartagena	Cartagena	4
Universidad Politecnica de Madrid	Madrid	3
Universidad Publica de Navarra	Pamplona	16
Universitat de Barcelona	Barcelona	57
Universitat Illes Balears	Palma Mallorca	4
Universitat Politecnica de Catalunya	Barcelona	55
Universitat Ramon Llull - La Salle	Barcelona	1
Universitat Rovira i Virgili	Tarragona	2
University of Malaga	Malaga	3
University of Sevilla	Sevilla	98
University of Valencia	Valencia	4
University of Valladolid	Valladolid	1
University of Vigo	Vigo	3
University of Zaragoza	Zaragoza	38
Sweden		
Aeroflex Gaisler	Goteborg	3
Bofors Defence AB	Karskoga	2
Chalmers University	Goteborg	6
Chalmers University of Technology	Gothenburg	66
Defence Researh Establishment	Linkoping	5
Ericsson	Molndal	2
Ericsson Microelectronics	Kista	2
Halmstad University	Halmstad	2
Institutet for Rymdfysik	Kiruna	1
Imego AB	Goteborg	1
Lulea University of Technology	Lulea	13
Lund University	Lund	181
Malardalens University	Vasteras	2
Mid Sweden University	Sundsvall	12
Royal Institute of Technology	Kista	41
RUAG Aerospace Sweden	Goteborg	2
SiCon AB	Linkoping	4
Svenska Grindmatriser AB	Linkoping	3
University of Trollhattan	Trollhattan	3
University of Linköping	Linköping	157
Uppsala University	Uppsala	11

CUSTOMER	TOWN	Number of ASICs
Switzerland		
Agilent Technologies	Plan-les-Ouates	2
Asulab SA	Marin	22
austriamicrosystems		2
Bernafon	Bern	1
Biel School of Engineering	Biel	9
CERN	Geneva	47
CSEM	Zurich/Neuchatel	62
CT-Concept	Biel/Bienne	9
Dectris	Baden	1
Ecole d'ingenieurs de Geneve	Geneve	1
Ecole d'ingenieurs et d'Archtectes	Fribourg	9
EPFL IMT ESPLAB	Neuchatel	39
EPFL Lausanne	Lausanne	334
ETH Zurich	Zurich	184
HMT Microelectronics Ltd	Biel/Bienne	4
Hochschule Rapperswill	Rapperswill	1
HTA Luzern	Horw	2
HTL Brugg-Windisch	Windisch	2
id Quantique	Carouge	19
Innovative Silicon S.A.	Lausanne	1
Institut MNT	Yverdon-les-Bains	1
Institute of Microelectronics, Uni. of Applied Sciences Northwest	Windisch	2
Landis + Gyr AG		1
Leica Geosystems	Heerbrugg	1
LEM	Plan-les-Ouates	3
MEAD Microelectronics S.A.	St-Sulpice	2
MICROSWISS	Rapperswil	2
Paul-Scherrer-Institute	Villigen	19
Photonfocus	Lachen	3
Senis	Zurich	4
Sensima technologies	Nyon	8
Sensirion	Staefa	2
Sentron AG	Lausanne	7
siemens	Zug	2
Smart Silicon Systems SA	Lausanne	2
SUPSI-DIE	Manno	2
Suter IC-Design AG	Waldenburg	4
University of Applied Sciences HES-SO	Valais	3
University of Neuchatel	Neuchatel	22
University of Zurich	Zurich	67
Uster Technolgies	Uster	1
Xemics SA - CSEM	Neuchatel	33
Taiwan		
Feng Chia University	Taichung	1
National Cheng Kung University		1
National Sun Yat-Sen University	Kaohsiung	3
National Tsing Hua University	Hsinchu	4
Thailand		
Kasetsart University	Chatuchak, Bangkok	1
Microelectronic Technologies	Bangkok	2
NECTEC	Bangkok	36

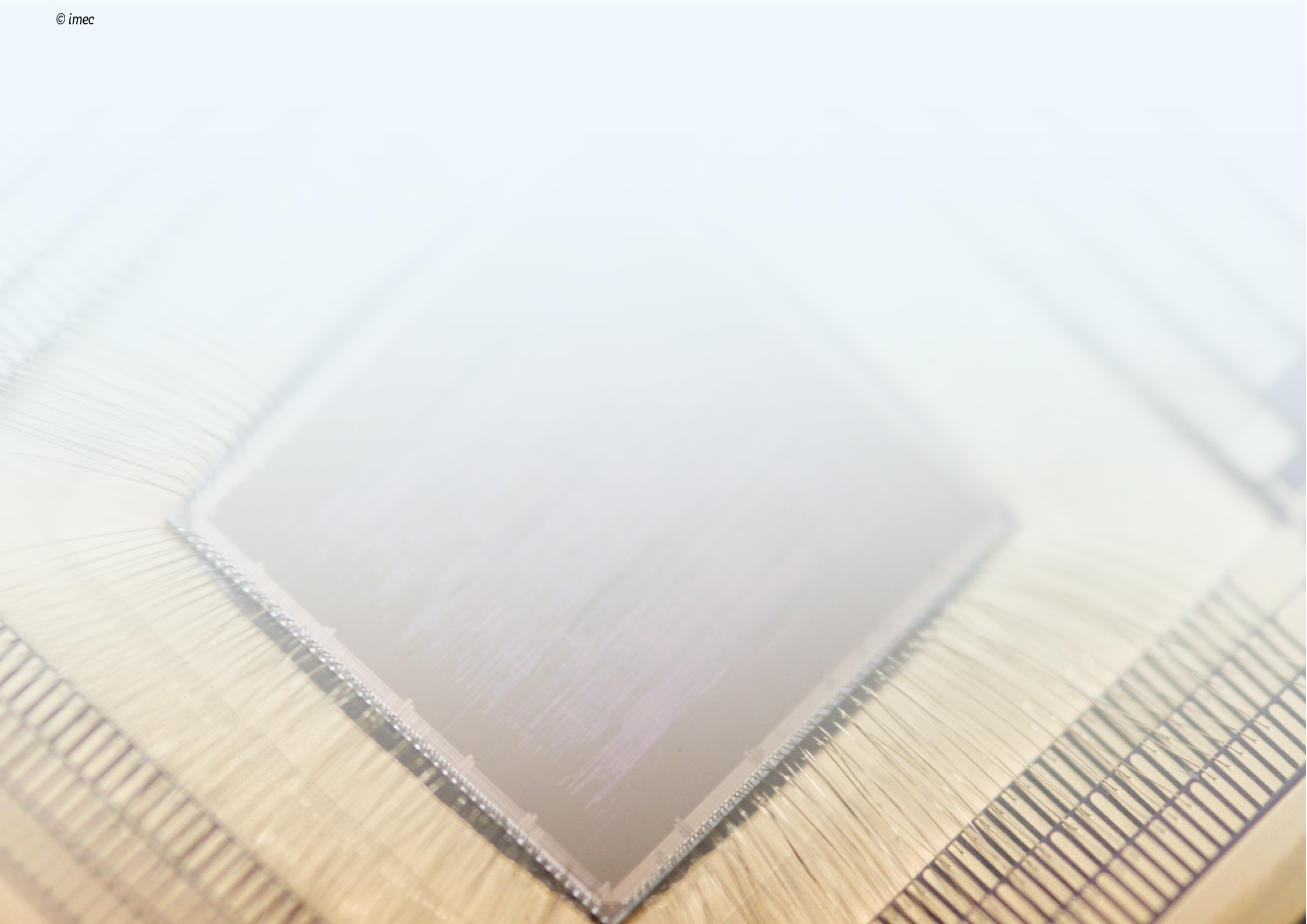
CUSTOMER	TOWN	Number of ASICs
Turkey		
ASELSAN	Ankara	1
Bahcesehir Universitesi	Istanbul	1
Bilkent University	Ankara	6
Bogazici University	Istanbul	24
Istanbul Sehir University	Altunizade	1
Istanbul Technical University	Istanbul	28
Kardiosis	Ankara	1
KOC University	Istanbul	1
Kocaeli University	Izmit	1
Middle East Technical Univ.	Ankara	15
Mikroelektronik Arastirma Gelistirme Tasarim ve Tic.	Istanbul	1
Sabanci University	Istanbul	24
Tubitak Bilten	Ankara	4
Yeditepe University	Istanbul	11
United Kingdom		
Aberdeen University	Aberdeen	1
Barnard Microsystems Limited	London	2
Bournemouth University	Poole	3
Bradford University	Bradford	7
Brunel university	Uxbridge	1
Cadence Design Systems Ltd	Bracknell	1
Cambridge Consultants Ltd.	Cambridge	3
Cardiff University	Cardiff	5
CML Microcircuits Ltd.	Maldon	21
Control Technique	Newtown	4
Data Design & Developmentsq	Stone	1
Dukosi	Edinburgh	2
Edinburgh University	Edinburgh	76
ELBIT Systems Ltd.		1
Epson Cambridge research lab	Cambridge	2
Heriot-Watt University	Edinburgh	2
Imperial College	London	77
Jennic Ltd	Sheffield	1
K.J. Analogue Consulting	Malmesbury	1
King's College London	London	1
Lancaster University	Lancaster	7
Leicester University	Leicester	1
Middlesex University	London	6
Napier University	Edinburgh	4
National Physical Laboratory	Teddington	3
Nokia Research Center	Cambridge	2
Nortel	Harlow	1
Plextek Ltd	Essex	4
Polatis	Cambridge	1
Positek Limited	Glos	1
Roke Manor Research Ltd.	Southampton	11
Saul Research	Towcester	22
Sheffield Hallam University	Sheffield	1
Sofant Technologies	Edinburgh	2
STFC - RAL	Didcot	59
Swansea University	Swansea	1
Swindon Silicon Systems Ltd	Swindon	3
Tality	Livingston	1
The Queens University of Belfast	Belfast	5

CUSTOMER	TOWN	Number of ASICs
The University of Hull	Hull	1
The University of Liverpool	Liverpool	14
UMIST	Manchester	58
University College London-UCL	London	2
University of Bath	Bath	29
University of Birmingham	Birmingham	6
University of Brighton	Brighton	1
University of Bristol	Bristol	15
University of Cambridge	Cambridge	37
University of Dundee	Dundee	1
University of East London	London	1
University of Glasgow	Glasgow	51
University of Hertfordshire	Hatfield	1
University of Kent	Canterbury	14
University of London	London	38
University of Newcastle upon Tyne	Newcastle upon Tyne	24
University of Nottingham	Nottingham	43
University Of Oxford	Oxford	29
University of Plymouth	Plymouth	2
University of Reading	Reading	1
University of Sheffield	Sheffield	7
University of Southampton	Southampton	42
University of Stirling	Stirling	1
University of Surrey	Guildford	6
University of the West of England	Bristol	2
University of Wales, Aberystwyth	Aberystwyth	5
University of Warwick	Coventry	6
University of Westminster	London	7
University of York	Heslington	2
Walmsley (microelectronics) Ltd	Edinburgh	1

USA

Analog	Phoenix	1
Arizona State University	Tempe	29
austriamicrosystems USA		1
Boston university	Boston	15
Brookhaven National Laboratory	Upton, NY	1
Brown University	Providence	1
Californian Institute of Technology	Pasadena	1
Carnegie Mellon University	Pittsburgh	1
Case Western Reserve University	Cleveland	1
Columbia University	Irvington, New York	20
Cornell University	Ithaca	1
Discera		1
Duke Universtity	Durham	1
Eutecus Inc	Berkeley	3
Exelys Ilc	Los Angeles	2
Flextronics	Sunnyvale	1
Forza Silicon Corporation	Pasadena	1
Fox Electronics	Fort Myers	5
Future Devices		1
General Electric	Niskayuna	3
Glacier Microelectronics	San Jose	1
Goddard Space Flight Center, NASA	Greenbelt	1
Intellectual Property, LLC	Cross Plains	1
Intrinsix	Fairport	1

CUSTOMER	TOWN	Number of ASICs
Iwatsu	Irving	4
Johnson Space Center, NASA	Houston	1
Kaiam Corporation	Newark	2
KLA Tencor	Milpitas	1
Lawrence Berkeley National Laboratory	Berkeley	8
Linear Dimensions, Inc.	Chicago	1
Micrel Semiconductor	San Jose	11
Microchip Technology		1
MIT - Lincoln Lab	Cambridge	31
MOSIS	Marina del Rey, CA	69
Neofocal Systems	Portland	8
Nova R&D	Riverside	3
Oklahoma State University	Stillwater	1
Omega Optics	Austin	4
Parallax Inc.	Rocklin	2
Philips Medical Systems	Andover	1
PhotonIC Corporation	Culver City	1
Princeton University	Princeton, NJ	5
Purdue University	Lafayette	1
Rensselaer Polytechnic Institute	Troy	2
Rockwell Scientific	Thousand Oaks, CA	13
Signal Processing Group	Chandler	1
Stanford Linear Accelerator	Meno Park	11
Symphonix	San Jose	5
Tachyon Semiconductor	Naperville, IL	2
Tekwiss USA, Inc	Costa Mesa	2
Telemetric Medical Applications	Los Angeles	1
Triad Semiconductor		1
TU Dallas	Richardson	5
University of California - San Diego	La Jolla	1
University of California - Santa Cruz	Santa Cruz	1
University of Chicago	Illinois	3
University of Colorado	Boulder	7
University of Delaware	Newark	3
University of Florida	Gainesville	11
University of Maryland - Joint Quantum Institute	Maryland	3
University of Michigan	Ann Arbor	1
University of Pennsylvania	Philadelphia, Pa.	2
University of Southern California - Los Angeles	Los Angeles	1
University of Southern California - Marina del Rey	Marina del Rey, CA	1
University of Texas at Austin	Austin	36
University of Washington	Seattle	2
USRA	Washington	1
Vectron International Inc.	Hudson NH	5
Western Cryptographic	Berkeley	1
Xerox	El Segundo	1
Yanntek	San Jose, CA	5



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