EUROPRACTICE
IC SERVICE

ACTIVITY REPORT 2014

EUROPRACTICE
IC SERVICE

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THE RIGHT COCKTAIL OF ASIC SERVICES

EUROPRACTICE IC SERVICE OFFERS YOU A PROVEN ROUTE TO ASICS THAT FEATURES:

- Low-cost ASIC prototyping
- Flexible access to silicon capacity for small and medium volume production quantities
- Partnerships with leading world-class foundries, assembly and testhouses
- Wide choice of IC technologies
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- RTL-to-Layout service for deep-submicron technologies
- Front-end ASIC design through Alliance Partners

Industry is rapidly discovering the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who don't need always the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise that includes IC manufacturing, packaging and test. This you can get all from EUROPRACTICE IC service, a service that is already established for 20 years in the market.

THE EUROPRACTICE IC SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:

- imec, Leuven (Belgium)
- Fraunhofer-Institut fuer Integrierte Schaltungen (Fraunhofer IIS), Erlangen (Germany)

By courtesy of imec

This project has received funding from the European Union's Seventh Programme for research, technological development and demonstration under grant agreement N° 610018.

This funding is exclusively used to support European universities and research laboratories.

FOREWORD

Dear EUROPRACTICE customers,

Time goes on. A year passes very quickly and when we look around us we see a tremendous rapidly changing world. And one of the reasons is the increasing use of micro- and nano-electronics in our daily life. While consumer, computing, telecom and mobile have been driving semiconductor usage for many years, the new growth opportunities are in data-com, security, medical and wearables, vision and imaging, and smart environments (including IoT). But these markets are significantly more differentiated and segmented and so innovation is being driven by Small and Medium Enterprises (SMEs) rather than the larger firms of previous eras, a process termed substream innovation.
It is in this new area of innovation that EUROPRACTICE has to play a more important role than ever. Europe can only play this leading role in substream innovation when our universities and research institutes have the necessary knowledge and infrastructure.
Thanks to the EUROPRACTICE service (since about 25 years, including EUROCHIP) students and researchers at about 650 European universities and research institutes have access to the most advanced and state-of-the-art EDA tools and micro- and nano-electronics technologies.

In 2014 we have been able to conclude successful negotiations with foundries to introduce 28nm.
From GLOBALFOUNDRIES we offer 55nm, 40nm and 28nm IC technologies. From TSMC we offer in addition to the existing 65nm, 40nm technologies also the 28nm technology in 2015.

But when we look at the new application areas where we see the future wave of substream innovation happening such as medical and wearables, IoT, ... we see that it is not necessarily needed to use the most advanced technologies such as 28nm. We see primarily two sweet spot of technologies used, namely the 0.18µ CMOS with its specialty versions mixed-signal, RF, high-voltage and eFlash and secondly the 65nm CMOS both logic and mixed-signal RF.

It is encouraging to see that we have fabricated now for the last 8 years around 540-550 ASIC designs on MPW runs. The *mini***@sic** runs are still heavily used to fabricate very small designs at very low prices. The majority of designs are still being fabricated in 0.18µ and 0.13µ CMOS technologies, but the use of 65nm technology is taking up.

To stimulate the substream innovation, we continue to support European SMEs and start-up companies with technology access, prototyping, test and packaging, qualification and production ramp.

Wishing you a prosperous 2015 !

Sincerely yours,

Dr. C. Das
Chairman EUROPRACTICE IC Service
imec (Belgium)

By courtesy of imec

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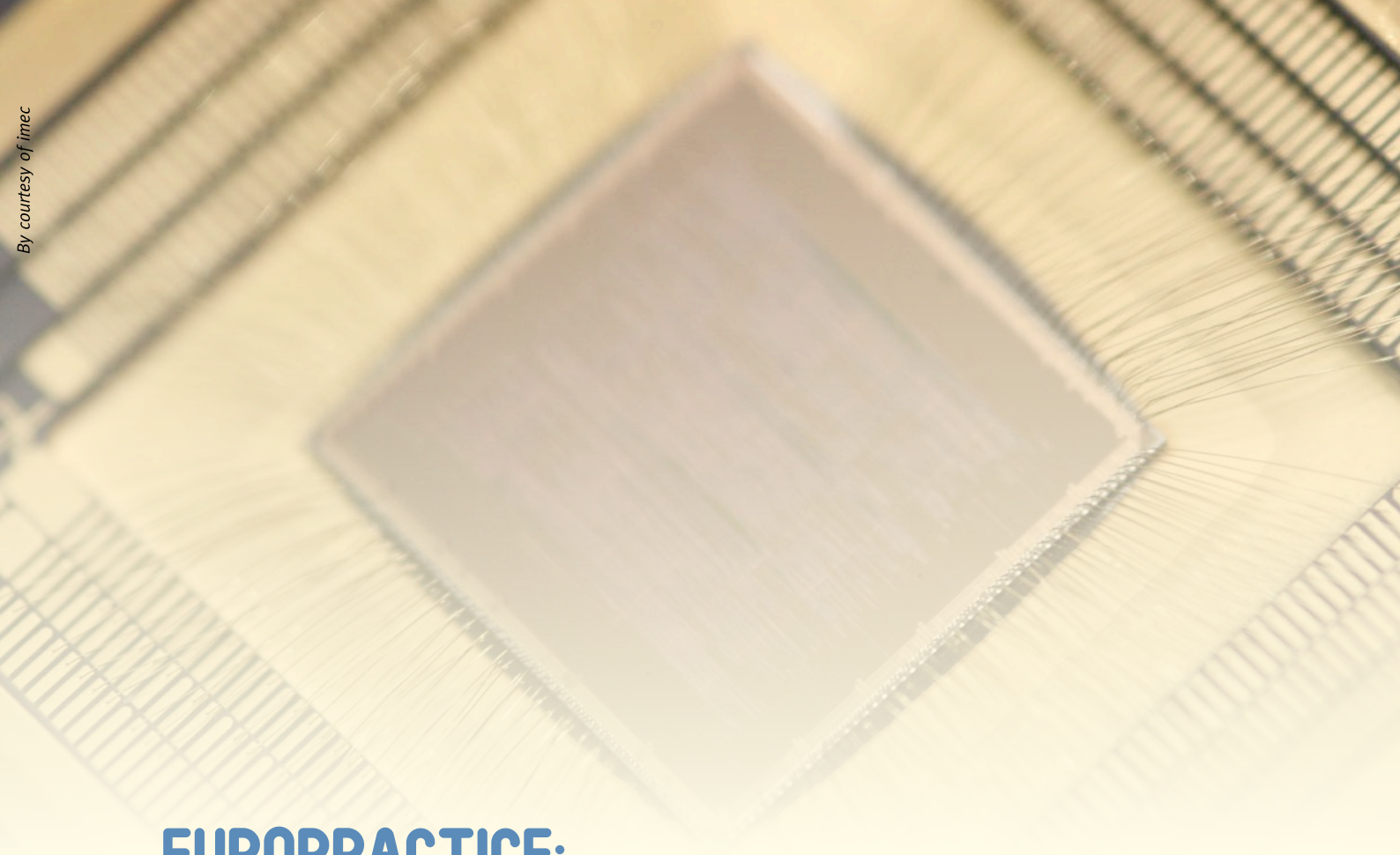


By courtesy of imec

EUROPRACTICE:
YOUR TOTAL AND TURN-KEY ASIC SOLUTION

EUROPRACTICE provides semiconductor and system companies with a total and turn-key ASIC solution including :

- easy access to foundry design rules, cell libraries and design kits
- deep submicron RTL-to-layout service
- low cost prototype fabrication service
- volume fabrication service including wafer fabrication, packaging and test
- ASIC qualification
- logistics
- technical customer support

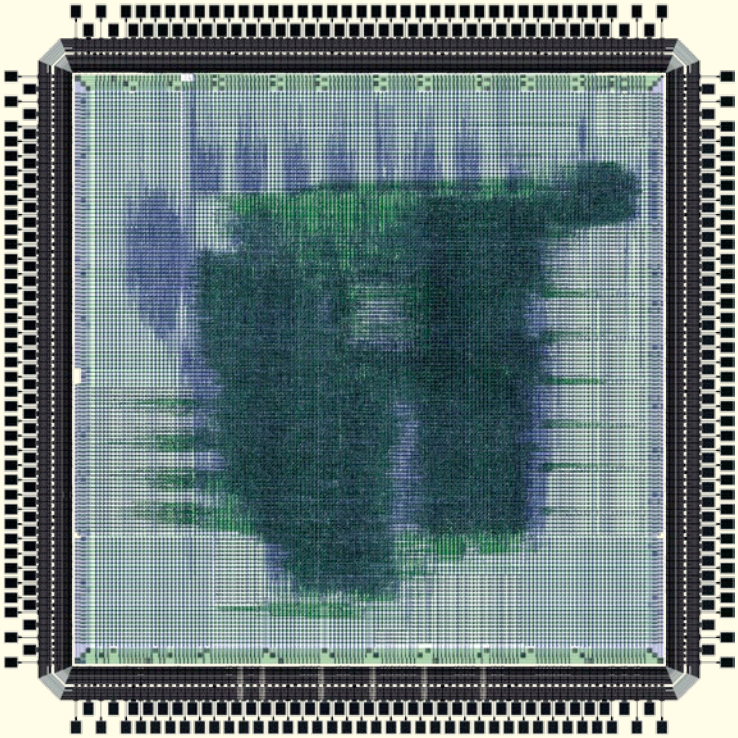
New fables startup companies as well as small companies or companies having small ASIC volume products in niche markets experience huge problems to get access to foundries since their volume is too small.

EUROPRACTICE has wafer foundry agreements with different leading suppliers, allowing to offer the most advanced as well as specific technologies to those customers. Our foundry partners acknowledge the EUROPRACTICE Service as the optimal solution to provide wafer capacity to smaller customers. Suppliers see EUROPRACTICE as one big customer representing about 650 universities, research centers and 300 companies world-wide. Through agreements with foundry partners, EUROPRACTICE is able to offer ASIC solutions ranging from a few wafers to thousands of wafers per year.

EASY ACCESS

Through its agreement with foundries and library partners, EUROPRACTICE is allowed to distribute foundry technology information and cell libraries upon simple signature of a standard Non-Disclosure Agreements or a Design Kit License Agreement. Those agreements can be downloaded from the EUROPRACTICE website. In this way you have access in a few days without having to go through a painful customer qualification procedure at the foundry. Foundry information includes design rules, spice parameters, design & layout manuals and DRC/ERC/LVS decks. Cell library information includes library manuals and design kits for most of the popular CAD tools (Cadence, Synopsys, Mentor Graphics, Tanner, etc.). This foundry and library information is distributed through our download servers.

ASIC DESIGN



By courtesy of imec

When customers have received design rules, cell libraries, etc., they can start the ASIC design. ASIC design can be split up into front-end design and back-end design. Front-end design covers ASIC specification feasibility study and design including tasks such as schematic entry, VHDL description, scan insertion, simulation and synthesis. The front-end design can be carried out by the customer himself or can be subcontracted to a design house. During this design phase, Europractice offers technical support on technology, test, type of package, etc. Important know-how and feedback from the test house will be used to improve the DFT (Design For Testability). "State-of-the-art" CAD tools are used during the ASIC design phase.
When the netlist is ready the backend design activity starts including layout generation using state-of-the art layout tools. Deep submicron digital place & route tasks are in most cases not performed by the customers. For those customers that have not their own layout tools, EUROPRACTICE is offering such deep submicron layout service (see deep submicron layout service on page 7). After initial layout, timing verification is carried out by the customer using parasitic layout information and layout is iterated until timing is met. Verification of the design needs to be done in all technology corners.

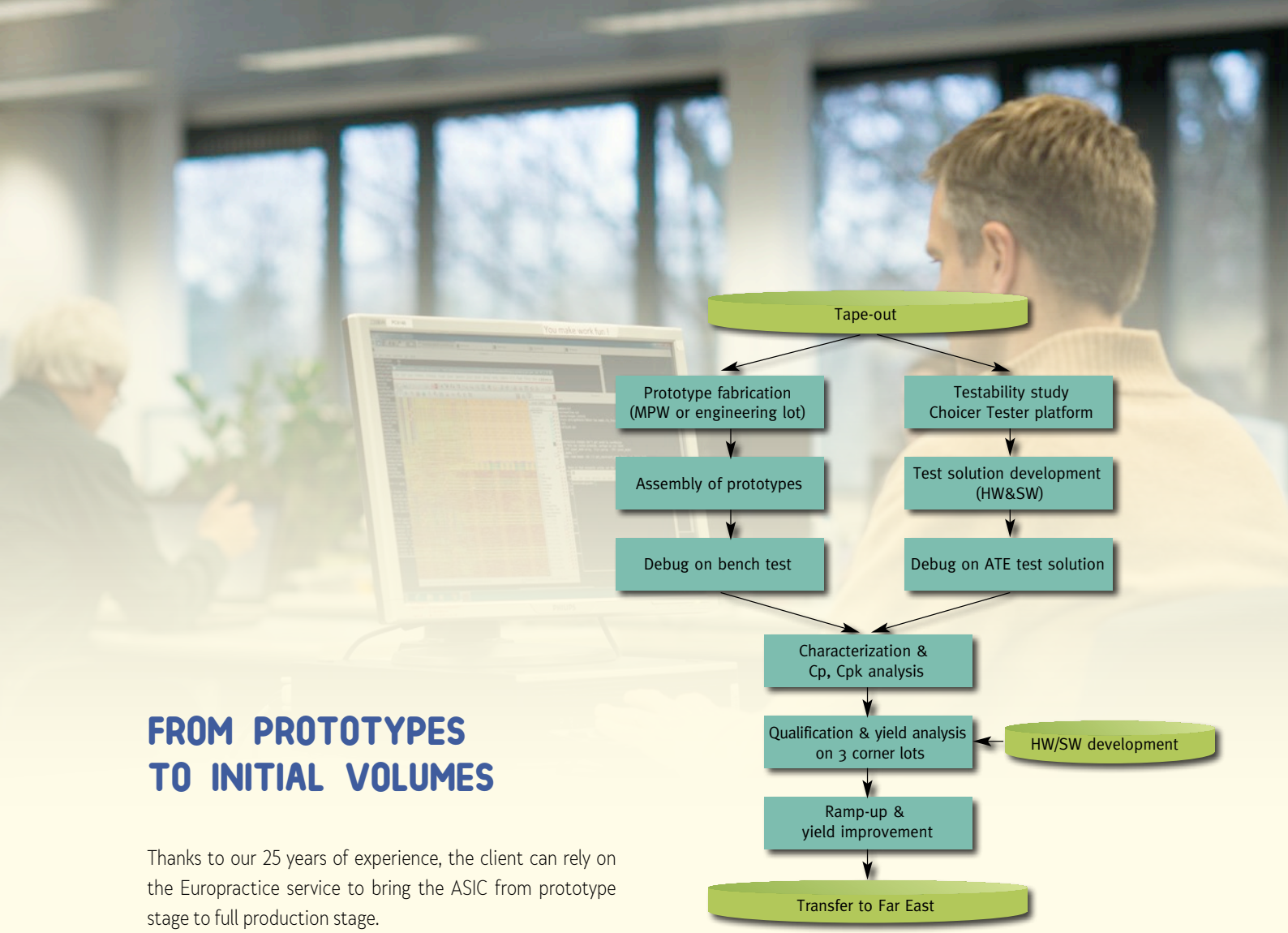
When layout is finished, a final DRC (Design Rule Check) and LVS (Layout versus Schematic) is performed on the GDS-II database in order to deliver a correct GDS-II to the foundry for manufacturing.

BACKEND OPERATION SERVICES THROUGH COOPERATION WITH CERTIFIED PARTNERS

A history of more than 25 years offering programs to microelectronics industry and academia endorse Europractice as the key partner to your ASIC's success. We embrace COT and turnkey business models to adapt to your requirements with a maximum level of transparency and flexibility. Side by side with world class partners and our long term agreements, Europractice boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.
Through these collaborative agreements our customers can benefit of working with highly recognized chip industry players. The most relevant companies involved in our semiconductor supply chain are listed below:

- **Foundry partners:**
  TSMC, UMC, ON Semi, ams, IHP, XFAB, GLOBALFOUNDRIES
- **Ceramic assembly partners:**
  HCM, Systrel, Optocap, Kyocera
- **Plastic assembly partners:**
  ASE, Kyocera
- **Wafer bumping partner:**
  Pactech, ASE
- **Test partners:**
  ASE, Microtest, Delta, Rood Technology and Blue test
- **Failure analysis:**
  Maser Engineering
- **Library partners:**
  Faraday, ARM

By courtesy of imec



FROM PROTOTYPES TO INITIAL VOLUMES

Thanks to our 25 years of experience, the client can rely on the Europractice service to bring the ASIC from prototype stage to full production stage.

PROTOTYPE FABRICATION

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. Europractice will produce the first prototypes for the customer and organize the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program.

The devices can be tested on both wafer level as well on packaged devices. The goal is to reduce the test time and to test the ASIC for manufacturing problems using the ATPG and functional patterns.

Europractice will support you during the development of single site test solution as well as with a multi-site test solution when high volume testing is required. Based on the test strategy followed diverse type of implementations can be realized.

DEBUG AND CHARACTERIZATION

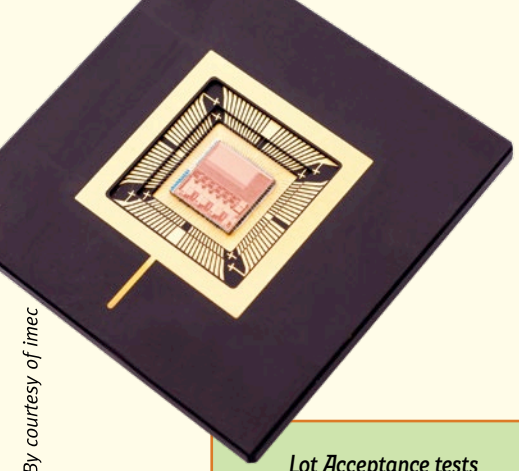
Before going into production a characterization test program will check if all the ASIC specifications are met according to the customer expectations. Threshold values are defined for each tested parameter. The software will test all different IP blocks and the results will be verified with the bench test results.

A characterization at Low (LT), Room (RT) and High (HT) temperature will be performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be strong against process variations, the product qualification can start. Europractice can support you through the full qualification process using different kind of qualification flows ranging from Consumer, Industrial, Medical to Space according to the Military, Jedec and ESCC standards....

In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.



By courtesy of imec

FROM INITIAL VOLUMES TO FULL PRODUCTION

Lot Acceptance tests

- Pre-cap inspection
- Destructive Physical Analysis (DPA)
- Electrical screening
- External and Internal visual inspection
- Cross sectioning: SEM
- Radiation tests (Tid, SEE)

Mechanical Acceptance tests

- Bond pull, Die shear
- Solderability
- Gross & Fine leakage tests
- PIND
- Marking resistance
- Mechanical shock
- Constant acceleration
- Vibration tests

Environmental tests

- Pre-conditioning
- TCT
- HTS
- HAST
- Autoclave, unbiased

Qualification tests

- Static or dynamic burn-in
- Operating life tests (HTOL)
- ESD & LU tests

Failure Analysis

- Non-destructive analysis: X-ray, SAM
- Electrical Failure analysis: Photo Emission Microscopy, probing, OBIRCH
- Physical analysis: SEM, TEM, FIB

SUPPLY CHAIN MANAGEMENT

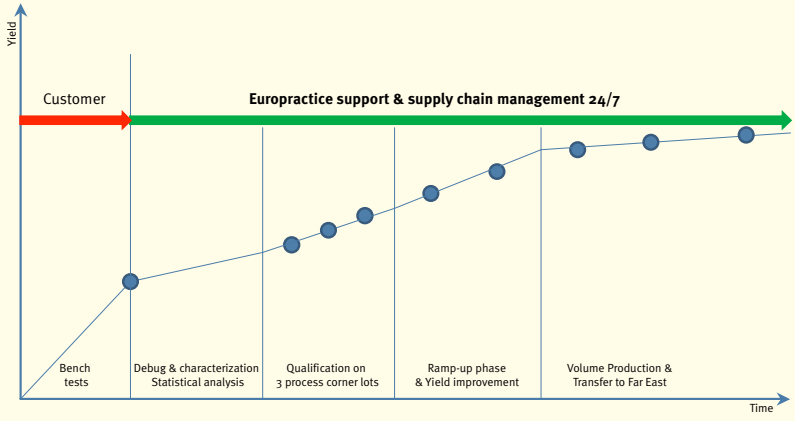
Europractice is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.

Customer products are treated internally as projects and followed closely by the imec engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. Europratice therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

YIELD IMPROVEMENT

Europractice can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the qualification of the device on 3 different corner lots, Europractice can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers will be analyzed to check for yield issues related to assembly or wafer production. Europractice is using the well proven tool Examinator™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.

FROM PROTYPE TO PRODUCTION KEEPING COST UNDER CONTROL



Europractice supports you from production ramp up till volume production taking into account global project costs. In cases of certain high volume in test is achieved, we are able to transfer the production test solution to Far East. The replicated test solutions are developed in close relationship with the Far East test houses to be fully compliant with their tester platforms.

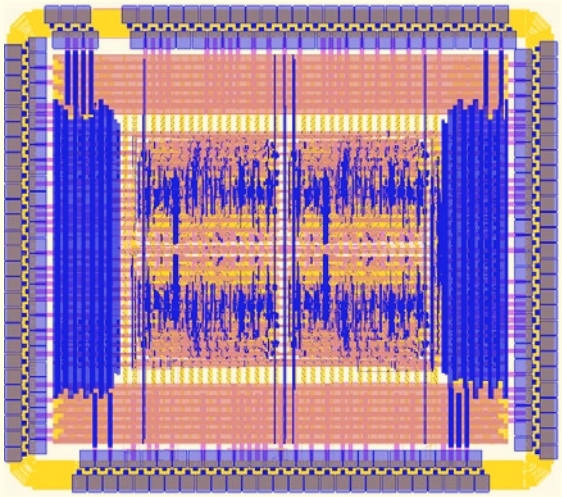
EUROPRACTICE OFFERS DEEP SUBMICRON DESIGN SUPPORT SERVICE

Synthesis and layout of deep submicron chips is not straightforward. You need a highly trained team of engineers equipped with expensive state-of-the art EDA tools to tape out first time right Silicon. The chips are growing in size while the technology dimensions are getting smaller and power specifications are becoming more stringent. Because of this, chip designers have to understand how to tackle issues like: hierarchical layout, clock skew, latencies of interacting clock domains, IR-drop on the power distribution, electro-migration and signal integrity, handling many metal layers in the back-end, incorporating IP blocks in the design, on-chip variation, design for packaging, design for manufacturing... And the list goes on.

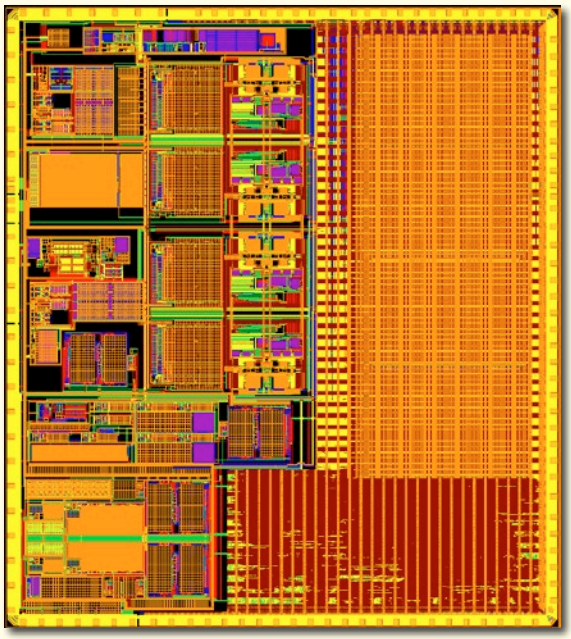
Supporting high-level system designers on the road to tapeout, EUROPRACTICE IC Service provides a physical design support service starting from RTL code in VHDL or Verilog or from a synthesized netlist.

The service supports the whole back-end design flow including synthesis, floorplanning, deep-submicron place and route and multi-mode multi-corner optimization, timing analysis, extraction, scan and BIST insertion and ATPG, tape-out preparation, etc. The service is equipped with state-of-the art tools from the major EDA vendors and has already supported technologies from many different foundries down to 28nm.

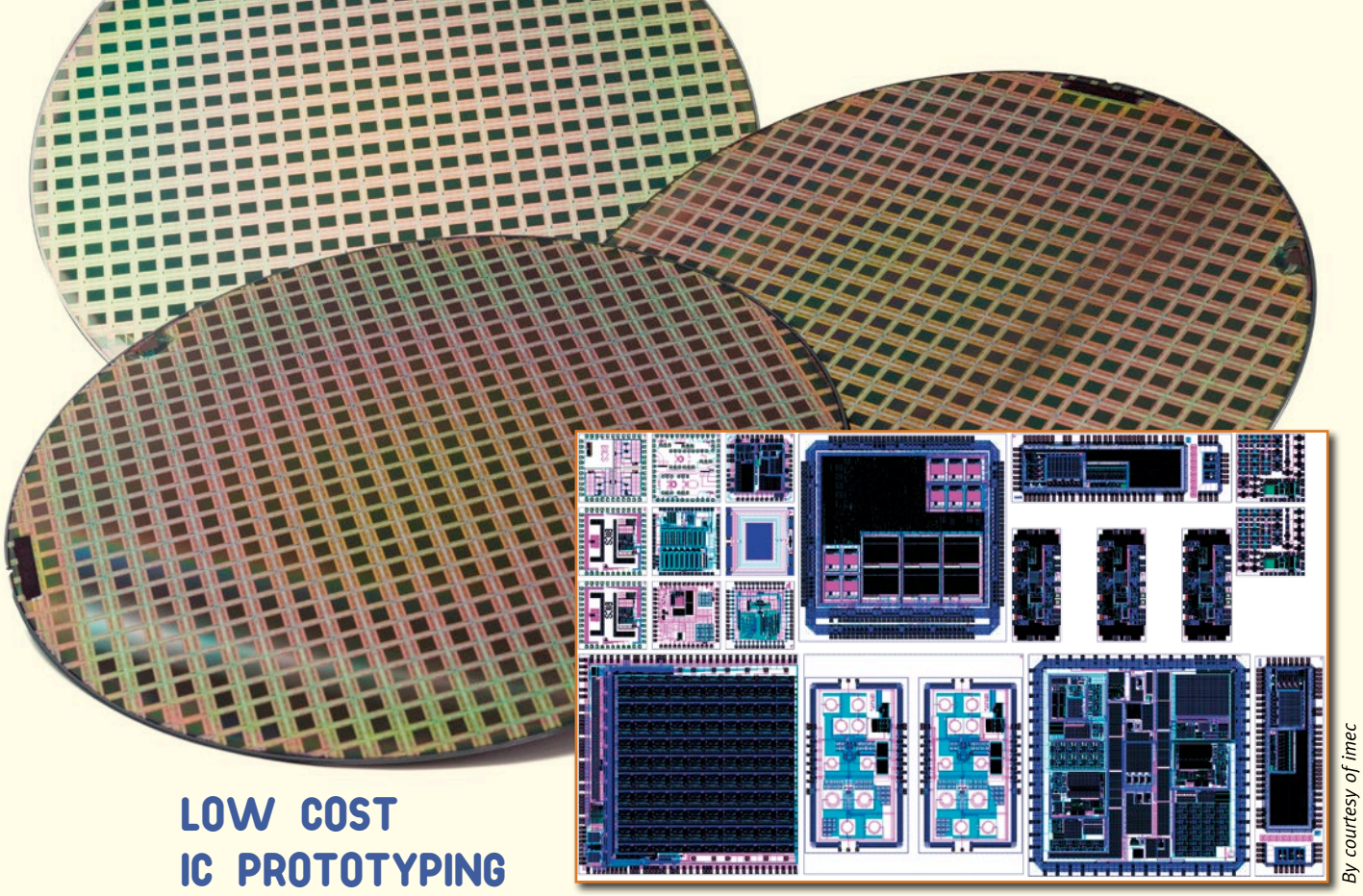
Many circuits were successfully taped out for in-house developed Systems-On-a-Chip as well as for ASICs developed by companies, design houses, research institutes and universities. These circuits included a.o. analog full custom blocks, memory macro's from different vendors, special I/O cells and RTL level (soft and firm) IP. The team is well versed in low-power techniques as well as the state-of-the art power format descriptions (CPF/UPF). Interrelated gated clock domains, power shut-off, multi supply-voltage and backbiasing have been successfully implemented.



Imec research design in 28nm TSMC technology. (By courtesy of imec)



Imec's mixed-signal chip for multisensor biopotential and optical data acquisition in 180nm. (By courtesy of imec)



By courtesy of imec

LOW COST IC PROTOTYPING

The cost of producing a new ASIC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. This is largely due to the NRE (Non-Recurring Engineering) overheads associated with design, manufacturing and test.

EUROPRACTICE has reduced the NRE, especially for ASIC prototyping, by two techniques:

(i) Multi Project Wafer Runs or
(ii) Multi Level Masks.

MULTI PROJECT WAFER RUNS

By combining several designs from different customers onto one mask set and prototype run, known as Multi Project Wafer (MPW) runs, the high NRE costs of a mask set is shared among the participating customers. Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full prototyping wafer run. A limited number of tested or untested ASIC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time".

In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service. EUROPRACTICE is organising about 200 MPW runs per year in various technologies.

MULTI LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi Level Mask (MLM). With this technique the available mask area (20 mm x 20 mm field) is typically divided in four quadrants (4L/R : four layer per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is thus reduced by a factor of four. By adapting the lithographical procedure it is possible to use one mask four times for the different layers by using the appropriate quadrants. Using this technique the mask costs can be reduced by about 60%.

The advantages of using MLM single user runs are : (i) lower mask costs, (ii) can be started any date and not restricted to scheduled MPW runs, (iii) single user and (iv) customer receives minimal a few wafers, so a few hundreds of prototypes.

This technique is preferred over MPW runs when the chip area becomes large and when the customer wants to get a higher number of prototypes or preserie. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.

This technique is only available for technologies from ON Semiconductor, IHP, TSMC and XFAB. ■

TECHNOLOGIES

For 2015, EUROPRACTICE has extended its technology portfolio.
Currently customers can have access to prototype and production fabrication in the following technologies :

- AMIS 0.7µ C07M-D 2M/1P & AMIS 0.7µ C07M-A 2M/1P/PdiffC/HR
- AMIS 0.5µ CMOS EEPROM C5F & C5N
- AMIS 0.35µ C035U 4M (3M & 5M optional) only thick top metal
- AMIS 0.7µ C07M-I2T100 100 V - 2M & 3M options
- AMIS 0.7µ C07M-I2T30 & I2T30E 30 V - 2M & 3M options
- AMIS 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)
- AMIS 0.35µ C035 - I3T50 50 V 4M - 3M optional (5M on special request)
- AMIS 0.35µ C035 - I3T50(E) 50 V 4M - 3M optional (5M on special request)
- AMIS 0.35µ C035 - I3T25 3.3/25 V 4M (3M & 5M optional) only thick top metal
- ams 0.35µ CMOS C35B3C3 3M/2P/HR/5V IO
- ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO
- ams 0.35µ CMOS C35OPTO 4M/2P/5V IO
- ams 0.35µ HV CMOS H35B4D3 120V 4M
- ams 0.35µ SiGe-BiCMOS S35 4M/4P
- ams 0.18µ CMOS C18 6M/1P/MIM/1.8V/5V
- ams 0.18µ HV CMOS H18 6M/50V/20V/5V/1.8V/MIM
- IHP SGB25V 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V
- IHP SGB25VGD 0.25µ SiGe:C Ft=75GHz@BVCEO 2.4V + RF HV-LDMOS GD-Module 22V
- IHP SG25H1 0.25µ SiGe:C Ft/Fmax=190GHz/220GHz 5M/MIM
- IHP SG25H3P 0.25µ Complementary SiGe:C Ft/Fmax (npn)110/180GHz / (pnp)90/120GHz 5M/MIM
- IHP SG25H3 0.25µ SiGe:C Ft/Fmax= 110/180GHz 5M/MIM
- IHP SG25H4 0.25µ SiGe:C Ft/Fmax= 200/220GHz 5M/MIM
- IHP SG13S SiGe:C Bipolar/Analog/CMOS Ft/Fmax= 250/300GHz 7M/MIM
- IHP SG13C SiGe:C CMOS 7M/MIM
- IHP SG13G2 SiGe:C Bipolar/Analog Ft/Fmax= 300/500GHz 5M/MIM
- IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)
- IHP BEOL SG25 (M1 and Metal Layers Above) + RF-MEMS + LBE + Photonics
- IHP BEOL SG13 (M1 and Metal Layers Above) + LBE + Cu
- X-FAB XH018 0.18µ HV NVM CMOS E-FLASH
- X-FAB XT018 0.18µ HV SOI CMOS
- TSMC 0.18µ CMOS General LOGIC, MS or MS RF (MIM: 1.0 or 2.0 fFum2 / UTM: 20kÅ)
- TSMC 0.18µ CMOS High Voltage Mixed-Signal (CV018LD 1.8/3.3/32V)
- TSMC 0.18µ CMOS High Voltage BCD Gen 2 (1.8V/5V...70V)
- TSMC 0.13µ CMOS General LOGIC, MS or MS RF (8-inch)
- TSMC 0.13µ CMOS General LOGIC, MS or MS RF (12-inch)
- TSMC 90nm CMOS General or LP Logic , MS or MS/RF (12-inch)
- TSMC 65nm CMOS General or LP MS/RF
- TSMC 40nm CMOS General or LP MS/RF
- TSMC 28nm CMOS Logic HPL (HKMG)
- TSMC 28nm CMOS Logic LP (SiON)
- UMC L180 Logic GII
- UMC L180 Mixed-Mode/RF
- UMC L180 Logic Low Leakage
- UMC L180 EFLASH Logic GII
- UMC CIS180 Image Sensor 1P4M – CONV diode
- UMC CIS180 Image Sensor 2P4M – ULTRA diode
- UMC CIS11 – image sensor
- UMC L130 Logic
- UMC L130 Mixed-Mode/RF
- UMC L110AE Logic/Mixed-Mode/RF
- UMC L65N Logic/Mixed-Mode/RF - SP
- UMC L65N Logic/Mixed-Mode/RF - LL
- GLOBALFOUNDRIES 55 nm Low Power E
- GLOBALFOUNDRIES 40 nm Low Power
- GLOBALFOUNDRIES 28 nm Super Low Power
- MEMSCAP METALMUMPS
- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- MEMSCAP PIEZOMUMPS
- ePIXfab-imec SiPhotonics Passives
- ePIXfab-imec SiPhotonics Full Platform*
- ePIXfab-LETI SiPhotonics Passives
- ePIXfab-LETI SiPhotonics Passives + Heater

By courtesy of imec

MINI@SIC PROTOTYPING CONDITIONS

FOR UNIVERSITIES AND RESEARCH LABORATORIES

Prototyping costs have been increasing with scaled technologies due to high mask costs. Even on MPW runs with shared costs, the minimum prototyping fee (corresponding to a minimum chip area) is high for advanced technologies such as 90, 65, 40 and 28nm.

In order to stimulate universities and research institutes to prototype small ASIC designs, Europractice has introduced in 2003 the concept of *mini***@sic**.

That means that Europractice has selected several MPW runs on selected technologies on which universities and research institutes have the opportunity to prototype very small ASIC designs at a highly reduced minimum prototype fee. The minimum charged chip area is highly reduced.

Through the *mini***@sic** concept, the price is reduced considerably. For the most advanced technologies however, the prototyping fee is further reduced through extra funding by the European Commission through the Europractice project (only for European universities and research institutes).

By courtesy of Microtest – Hatina ATE

SPACE QUALIFICATION ACCORDING TO ESCC9000

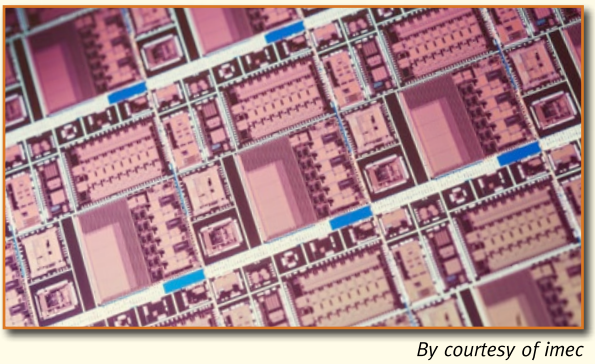
During 25 years, Europractice built up a lot of experience for space qualification. Following the ESCC 9000 standard, the service is providing full support to get your product qualified and ready for flight model. Always pushing the limits of the technology the Europractice is the solution to launch your ASIC to space.

From the start of the project, Europractice provides consulting on the ASIC die pad layout taking into account the parasitics of the full package. Afterwards, if necessary, a dedicated package for your ASIC will be manufactured. The expertise of Europractice together with the professionalism of our partners result in a solution that will fit your space requirements.

In order to increase the yield after packaging, Europractice provides their customers with wafer probing prior before to assembly. All ASIC's are assigned to a unique number at wafer level. Taking this approach Europractice is able to provide full traceability of all the components.

When the ASIC's are ready to be assembled into the package, a pre-cap inspection is done. This step is in close cooperation with the customer, our partners and the experts of the Europractice service.

Before chart F4 of the qualification is performed, Europractice will check if the lot can be accepted by performing the "Lot Acceptance Test". This Lot Acceptance Test includes data analysis of the wafers and radiation tests. The radiation tests include the total dose steady-state irradiation (Tid) and single event effect test (SEE).



By courtesy of imec

Over the years, imec, together with its partner Microtest developed, a portable test system called Hatina. This portable tester enables imec to perform a complete measurement and data log of the devices while performing radiation tests. These real-time measurements provide the customer with an in-depth understanding how the ASIC will behave in space.

When passing radiation tests, all the remaining parts will enter the chart F3 for screening and will continue from there to chart F4 for qualification. Working with different partners enables imec to implement in their supply chain a significant amount of quality assurance gates (QA gates). Imec has built up huge experience in logistics and an internally developed tool keeps track of the status of all devices.

In order to assess the operating life time of a device, a dedicated burn-in oven was developed. This oven has the ability to heat your ASIC up to the desired temperature, while the auxiliary components are still at room temperature. This makes sure that when a fail is detected, the customer knows that this is related to the device and not to one of the auxiliary components. During the operating life all devices are monitored and all data is written to a log file.

Finally a "Qualification report" is delivered together with the ASIC's (flight models) which contain all the data of each device.

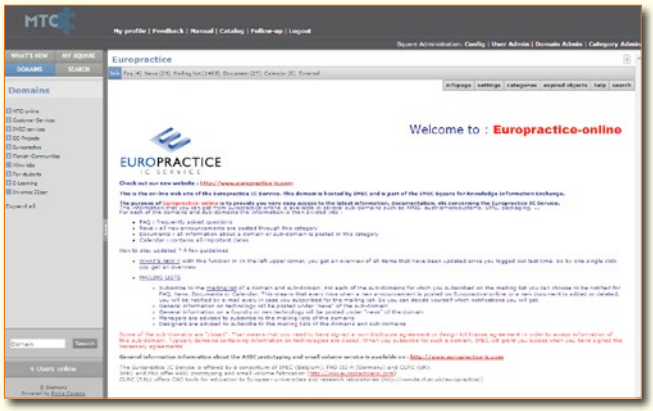
WEB SITE

http://www.europractice-ic.com

The Europractice web site for IC prototyping has been totally renewed and provides full information such as:

- Technologies
- Specification sheets
- Available and supported cell libraries and design kits
- MPW runs
- MPW prices
- Small volume possibilities
- Deep submicron netlist-to-layout service
- Procedures for registration of designs for prototyping
- Etc.

EUROPRACTICE-ONLINE



http://www.europractice-online.be

In 2003 Europractice introduced "Europractice-online", a platform for information exchange. This platform is hosted by imec's Microelectronics Training Center.

Users can register to access information available on Europractice-online. The information that is available is grouped per technology and contains:

- Public information
- Confidential information in 'closed' domains, accessible after signature of Non-Disclosure Agreement or Design Kit License Agreement
- News flashes
- Frequently Asked Questions
- Mailing lists

The user can personalize the mailing lists in such a way that he is automatically informed by e-mail whenever a new document is posted, news is posted, FAQ is posted, etc. The user can choose for which technologies he will be notified. As such managers can select to be informed on latest news, whereas designers can ask to be notified on all new items for a specific technology.

RESULTS

MPW PROTOTYPING SERVICE

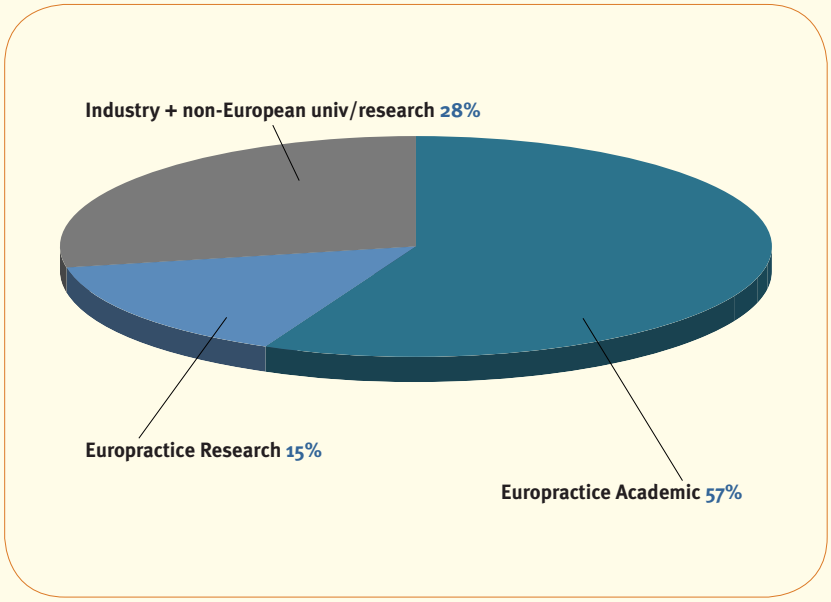
ASICS PROTOTYPED ON MPW RUNS

In 2014, a total of 544 ASICs have been prototyped.

72% of the designs are sent in by European universities and research laboratories while the remaining 28% of the designs is being sent in by non-European universities and companies world-wide.

GEOMETRY MIX

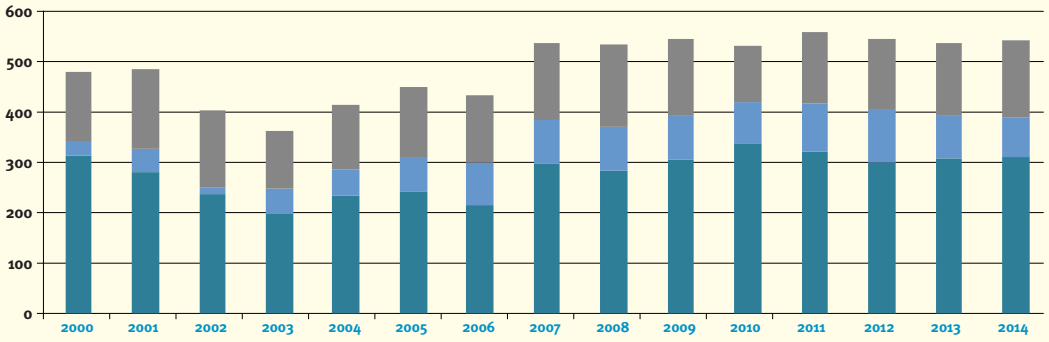
Year over year we see a shift towards newest technologies. Also in 2014 the same trend is shown. Again, the majority of designs is done in 0.18µ / 0.15µ technology (28%). Also the number of designs in Silicon Photonics (MEMS) technology has taken up.



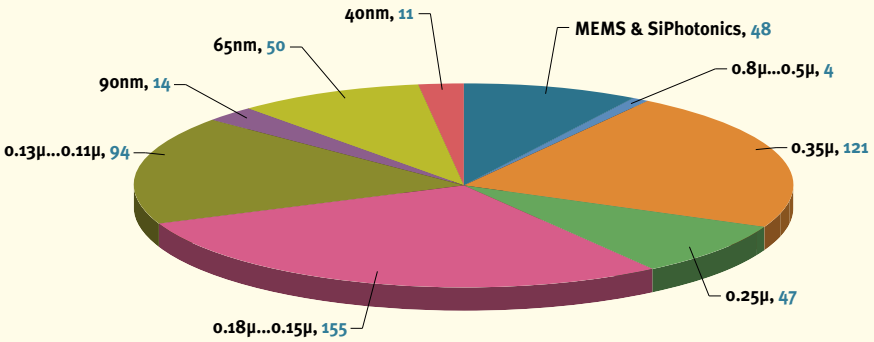
MPW designs in 2014

MINI@SIC

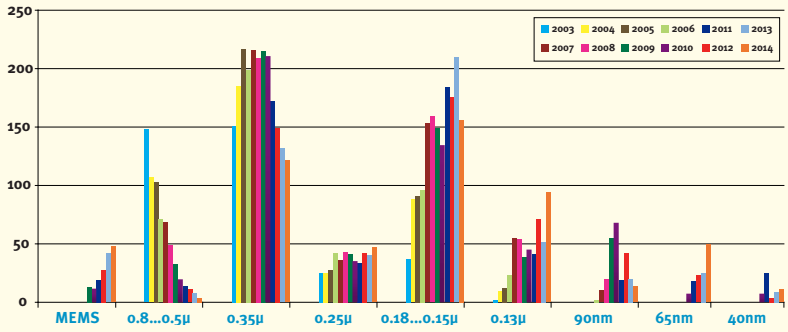
Very encouraging is the fact that the *mini***@sic** concept continues to be accepted very well by the universities in 2014.



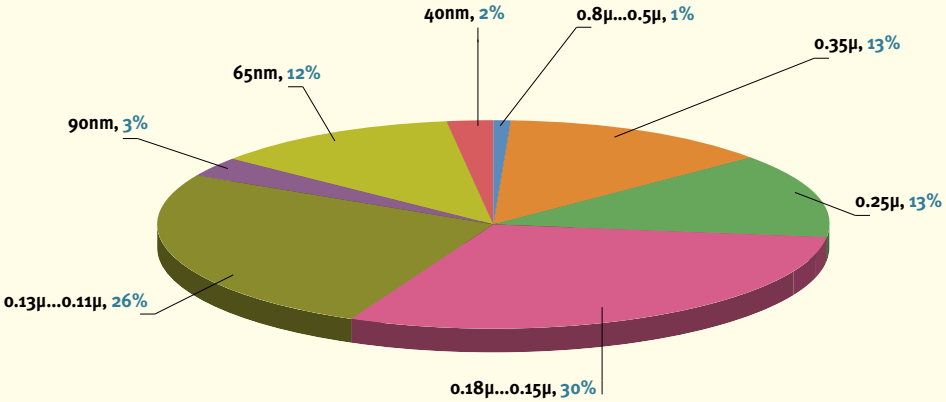
	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
Industry + non-European univ/research	140	159	155	115	128	138	134	154	164	153	113	143	139	144	153
Europractice Research	27	46	13	48	52	69	84	87	85	87	83	96	105	87	80
Europractice Academic	313	281	237	200	234	243	215	298	285	305	337	321	301	307	311



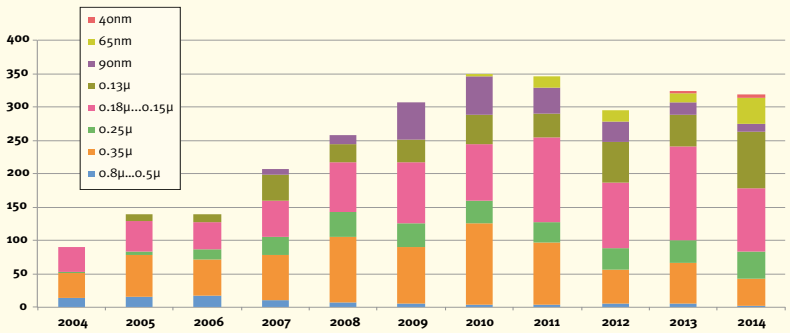
MPW designs in 2014: technology node and number of designs



Geometry mix



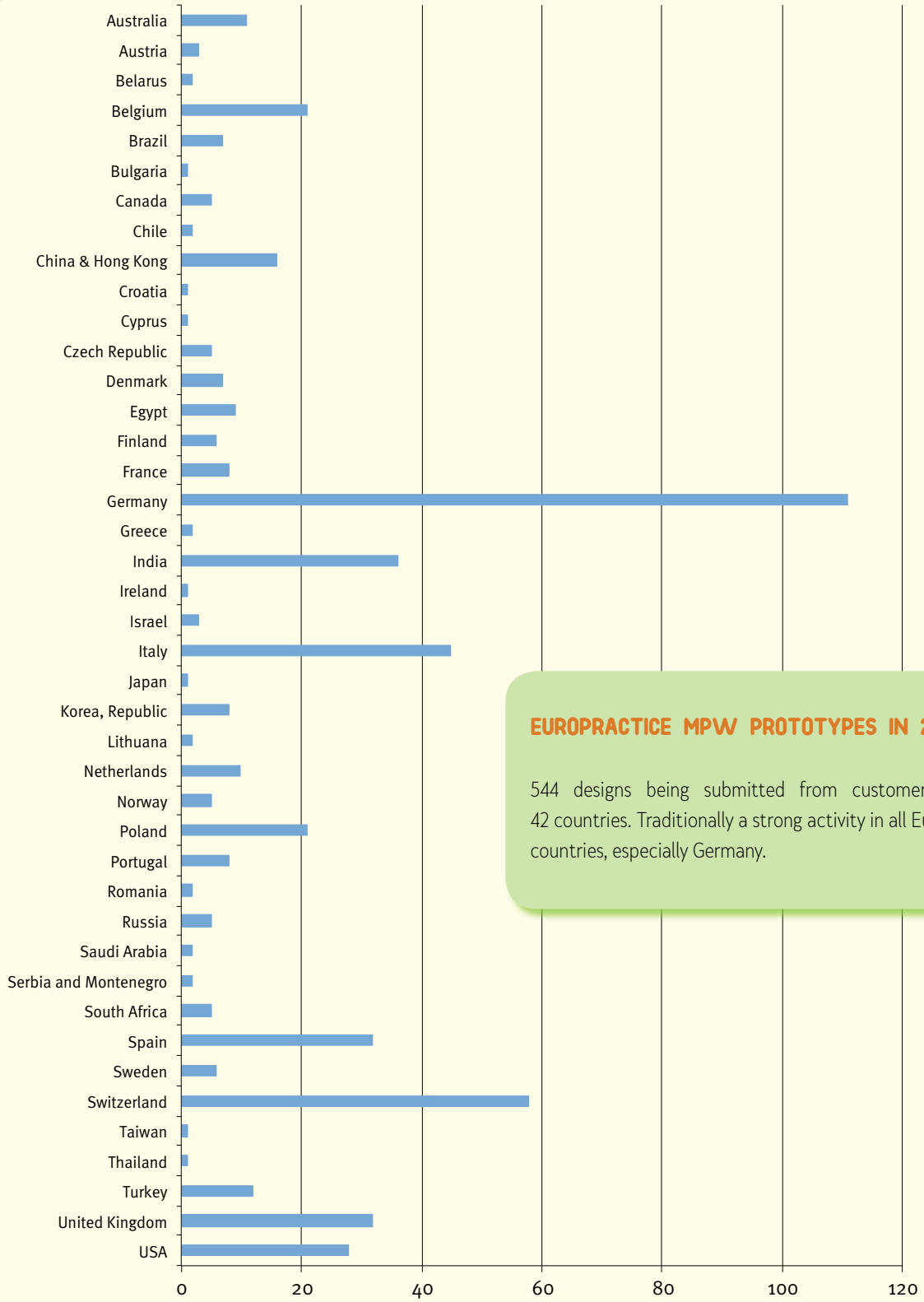
*mini**@sic** designs per gatelength in 2014*



SMALL VOLUME PROJECTS

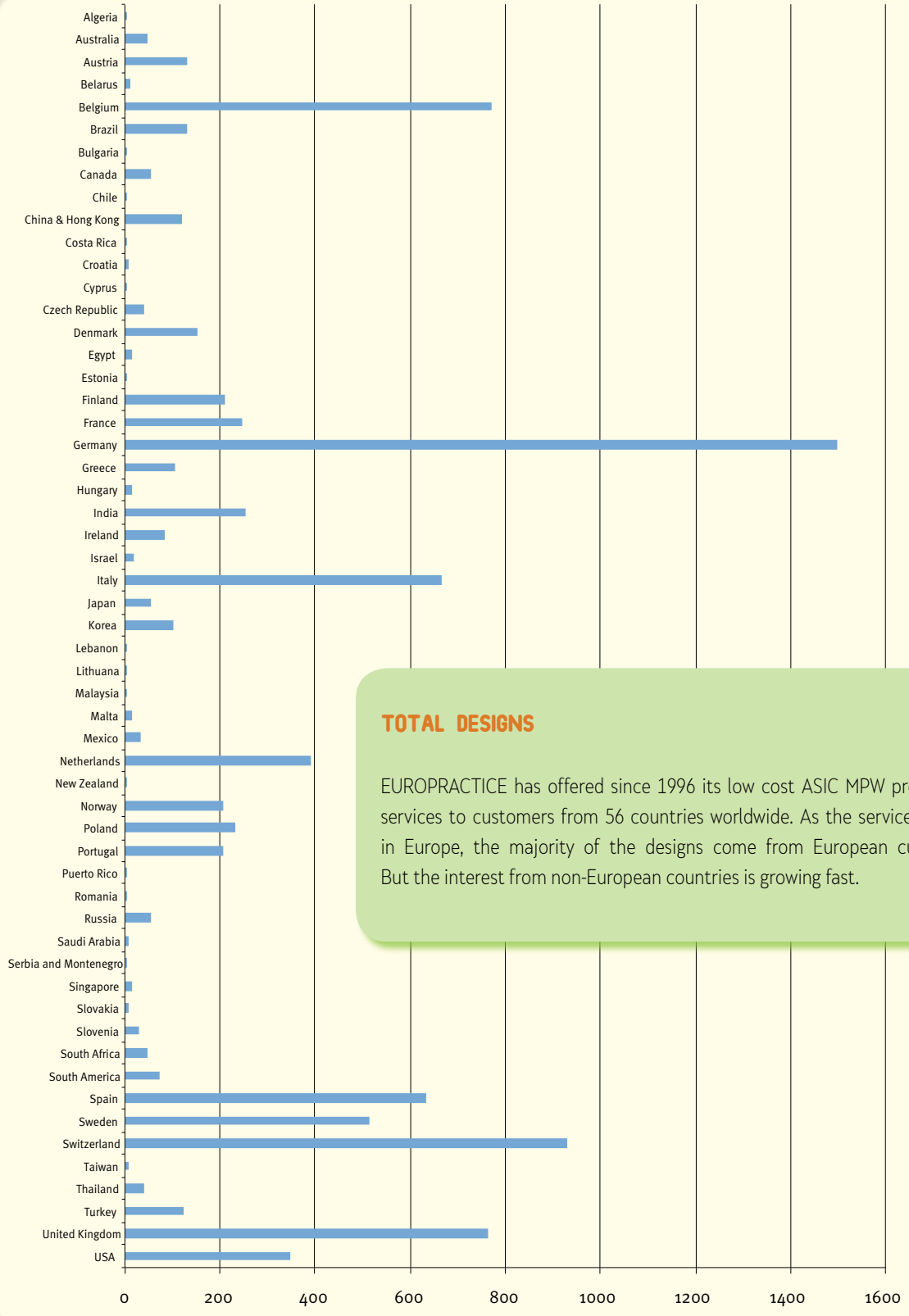
More and more customers are using the COT (Customer Own Tooling) model when they need volume production. Through this COT model they have full control about every aspect of the total design and production flow. Large customers with sufficient ASIC starts and volume production can invest in the COT model as it requires a considerable knowledge and experience about all aspects such as libraries, design kits, transistor models, testing, packaging, yield, etc. For smaller customers the COT model is very attractive but very difficult due to the lack of experience. For those customers EUROPRACTICE offers the solution by guiding the customers through the full production flow applying the COT model. EUROPRACTICE helps you with technical assistance in the selection of the right package, setting up the test solution, yield analysis, qualification, etc.

Through EUROPRACTICE you can also experience the benefits of the COT model.



EUROPRACTICE MPW PROTOTYPES IN 2014

544 designs being submitted from customers from 42 countries. Traditionally a strong activity in all European countries, especially Germany.



TOTAL DESIGNS

EUROPRACTICE has offered since 1996 its low cost ASIC MPW prototyping services to customers from 56 countries worldwide. As the service is based in Europe, the majority of the designs come from European customers. But the interest from non-European countries is growing fast.

EXAMPLES OF ASIC PROJECTS

ams

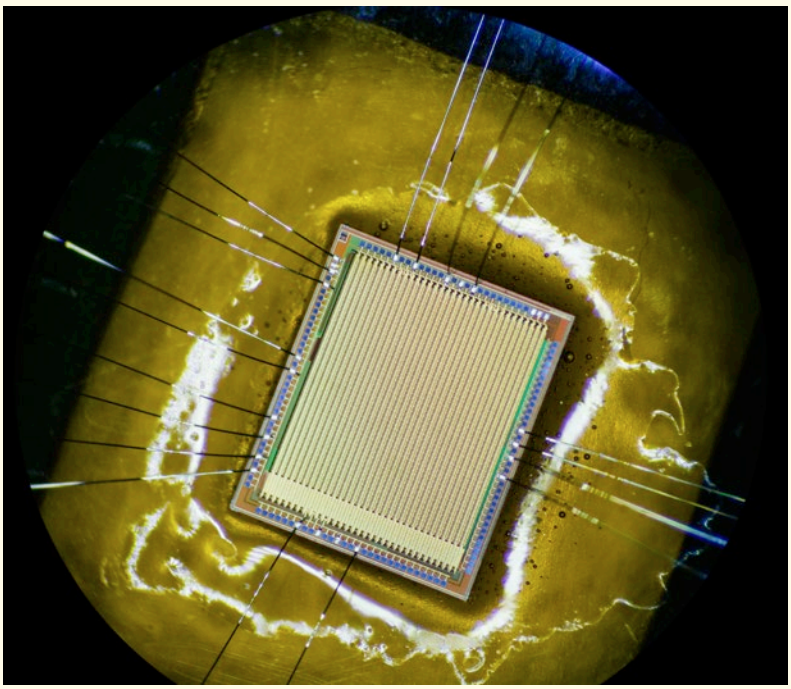


Figure 1: Thinned MuPixel detector

HVCMOS Pixel Sensor for Mu3e Experiment

Karlsruhe Institute of Technology – KIT

Contact: Prof. Dr. Ivan Peric*, Group for Detector Technology and ASIC Design, Institute for Data Processing and Electronics – IPE, PO box 3640, 76021 Karlsruhe, Germany / Phone +49 721 6082 9191 / *) until 2014 University of Heidelberg

Technology: Ams 0.18 HV CMOS

The chip MuPixel is a high voltage CMOS pixel sensor. In contrast to the standard pixel sensors that mostly rely on diffusion as signal collection mechanism, HVCMOS sensors use high voltage to deplete relatively large volume around the pixel electrode. The charge signals generated by ionization are collected by drift.
It is in principle difficult to combine a high voltage and low voltage electronics inside small pixels. To enable this, we have developed the following structure:
The sensor element is an n-well diode in a p-type substrate. The electronics is placed inside the n-well sensor electrode. In this way, the electronics is protected from the high voltage.
HVCMOS sensors are sensitive to single ionizing particles and the signal collection is much faster than in the case of the standard pixel sensors. The high voltage sensors are suitable for the applications where single particles should be detected, such as high energy physics, electron microscopy and soft x-ray detection.
One of the applications of HVCMOS sensors is the Mu3e experiment.
The aim of the Mu3e experiment at Paul Scherrer Institute (PSI), Switzerland, is the search for the “new physics” beyond the Standard Model.

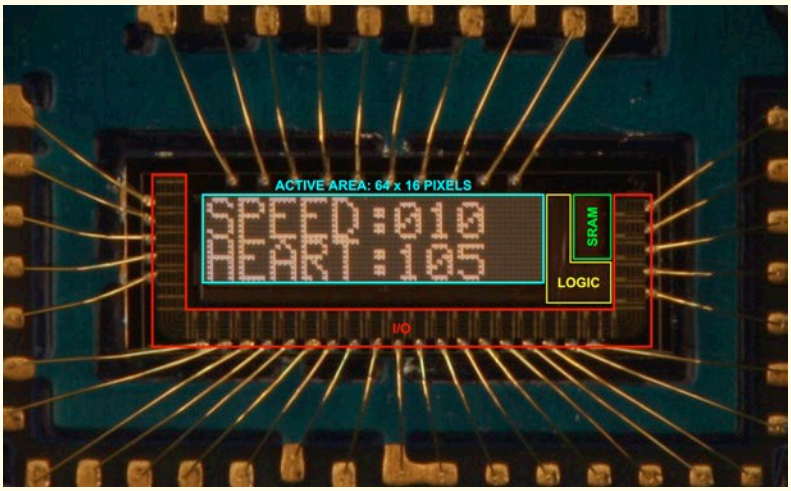
The Mu3e pixel detector should be able to cope with very high particle rate 109/s. It should have a spatial resolution better than 100 µm, and a time resolution of 100ns. There will be four pixel layers with 100 µm x 100 µm pixel size, 275 million pixels and a total area of 1.9 m2. The pixel detector thickness will be only 50 µm. In this way, the sensor will not deflect the particles passing through it. From the trajectory measurement (curvature in magnetic field) a good momentum resolution can be achieved. The project is performed in collaboration between University of Heidelberg, PSI, ETH and university Zuerich, and the Karlsruhe Institute of Technology (KIT).
Within the Mu3e project we have designed several sensor prototypes, the newest is the MuPixel7 submitted in August 2014.

Results

The tests on MuPix prototypes are still ongoing. As example we will mention that in test beam measurement 99% detection efficiency has been shown. Chips have been thinned to < 100 µm and successfully tested. Figure 1 shows a thinned MuPixel detector.

Why Europractice?

Europractice offered us the possibility to fabricate sensor chip under very good conditions – it is for instance possible to fabricate very small and cheap test chips ("miniasic"). In this way, we can test the circuits before employing them on larger designs. Europractice organized thinning of the chips. The last MuPixel prototype has been ordered on substrates of several thicknesses from 50 µm. The customer support, which includes checks of designs for errors, is excellent.



Gaining information from CMOS ICs using visible light

Carl and Emily Fuchs Institute for Microelectronics, Department of Electrical, Electronic and Computer Engineering, University of Pretoria, South Africa, in conjunction with INSiAVA (Pty) Ltd

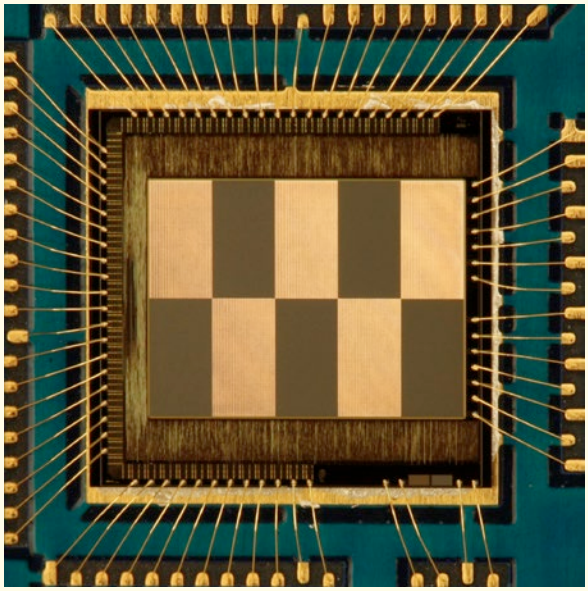
Contact: Dr Jannes Venter, Marius Goosen
E-mail: jannes.venter@up.ac.za, marius.goosen@insiava.com
Technology: ams AG C35 0.35µm CMOS 4M
Die size: 4100x1400 µm

Introduction

Light emission from silicon was first observed in 1955, emanating from reverse biased pn-junctions operating in avalanche breakdown. This phenomenon labelled hot carrier electroluminescence has been shown in our previous work to be successfully leveraged to emit light in standard CMOS processes. This addition of light emitting elements to standard CMOS processes enables a range of applications previously limited to multi-chip modules and exotic materials.
Light emission from standard CMOS technologies feature several characteristics enabling unique value to be unlocked in future integrated circuits. These characteristics include the seamless integration with standard CMOS transistors (3.3 V and 1.8 V), wide operating temperature range (-50 °C to 125 °C) and fast modulation frequency (> 1 GHz).

Description

The showcased design is a 64x16 pixel CMOS information display and the first example of a total chip display system integrated on a single chip. Example applications which may benefit from this design include the display of near-to-eye information (e.g. smart sports glasses) as well as potentially providing visibility into complex electronic systems through visually perceivable feedback (e.g. MCU-based embedded systems) while maintaining a small form factor at a CMOS price.



Our research efforts resulted in an improvement of light emission efficiency to the point where conventional camera modules, such as is found in smartphones, can detect the emitted light. This was successfully demonstrated to not only be feasible but also practical and convenient for a variety of applications. In addition, the emitted light reaches levels of up to 90 cd/m2 providing images easily perceptible to the human eye. By spatial encoding the emissive microdisplay matrix, both a smartphone and a human observer can directly interact, optically and wirelessly, with CMOS integrated circuits.

Results

The current encapsulation features a 40 µm pixel pitch with a typical power consumption of 300 mW at an operating voltage of 7.5 V. The active area produces a luminance of up to 90 cd/m2 with an arbitrary refresh rate limited in this case to 120 Hz. The total chip solution features a SPI interface and an integrated SRAM frame buffer, each bit representing the status of a pixel on the microdisplay. Additionally CMOS QVGA and VGA resolution microdisplays have also been realised in the ams AG 0.35 µm CMOS process, featuring pixel pitches of 15.5 µm and 8 µm respectively, towards greyscale video microdisplays.

Why Europractice?

Through Europractice, access is provided to state-of-the art EDA software and numerous CMOS technologies. The MPW runs administered through Europractice provide a regular, predictable and affordable avenue for research and development.

Acknowledgements

This work was funded by INSiAVA (Pty) Ltd. INSiAVA is a venture capital funded semiconductor company based in Pretoria, South Africa.

Silicon drift detector front-end chip for X-ray spectroscopy

National Research Nuclear University «MEPhI» & Space Research Institute (IKI), Moscow, Russia

Contact: Eduard V. Atkin
E-mail: evatkin@mephi.ru

Technology: AMS 0.35 µm CMOS C35B4C3 4M/2P/HR/5V IO, MPW run 4289
Output: 40 naked dies
Die size: 3755 x 1331 µm^2

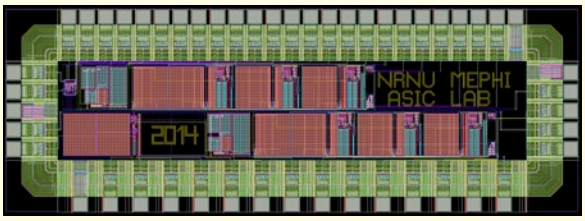


Fig.1 Layout

Introduction

The Silicon Drift Detectors (SDD) are monolithic X-ray detectors widely used in X-ray spectrometry and XRF-analysis. The high energy resolution (close to theoretical limit) at less than one microsecond shaping times, good efficiency up to 20 keV and high count rate ability make them very attractive as X-ray photon detectors in astrophysical applications. The study of X-ray pulsars and gamma-ray bursts with time resolution better than one microsecond is a new task for high time resolution astrophysics. The arrays of SDD can be used as focal plane detectors for astrophysical X-ray telescopes with high time resolution (better than 500 ns) and an energy one (better than 130 eV at 6 keV).

Another application of interest is the connection of the SDD array to a single scintillator. Such device can be used for gamma-ray imaging and spectroscopy in a MeV energy range. It is obvious that creation of multichannel SDD arrays is impossible without the development of ASIC.

Description

The main aim of this work was to design and prototype the front-end analog building IP-blocks for the future ASIC for SDD arrays. The layout of the prototyped chip is shown in Fig.1. The chip structure is composed by two different versions of analog channels. Each one consists of a low-noise

charge sensitive amplifier (CSA), semi-Gaussian 6-th order filtering amplifier (shaper) with eight selectable shaping times, fast two-threshold comparator and a thermostable bias block (Fig. 2).

The most attractive SDDs for arrays creation are designed by PN-Detector GmbH [1]. Those devices include the front-end JFET, built-in to the SDD die to simplify its integration with low noise multichannel system. For this reason the first CSA version was optimized for working with PN-Detector's SDDs.

Another stand-alone CSA version, instead of using a built-in SDD JFET, utilizes an input pMOS transistor available from the AMS CMOS process. Its geometry was optimized for matching with SDD to be used mostly in terms of a compromise between low noise, power consumption and chip area. The CSA converts the charge, created in the SDD volume by an X-ray photon, into the output voltage. The latter is filtered by a shaping amplifier to maximize the signal-to-noise ratio. Variation of the shaping time allows us to adjust the system performance for optimal time-energy resolution level. For obtaining a minimum noise level both CSA versions were designed to work in the pulsed reset mode. A two-threshold comparator can be used to reset signal generation.

The necessity in future for the development of a complex mixed-mode ASIC requires from us the choice of the technology with well verified both analog elements and standard digital cells. The 0.35 μm pure CMOS process of Austria Microsystems gave us the best fit for the required element and cell libraries to be used. Also the flexibility of the AMS MPWs in selecting a chip size with a big aspect ratio has facilitated for us a problem of long channel prototyping, giving us a way to create a future multichannel ASIC as a simple replication of separate channel.

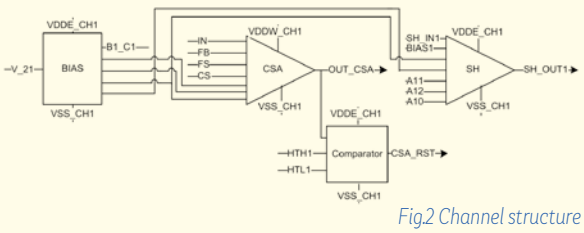


Fig.2 Channel structure

The developed structure allows to avoid the extensive usage of discrete components for detector biasing and signal conditioning.

The main parameters of the channels are:

- Power consumption: 1.3 mW @ 3.3V
- Preamp gain: 100 mV/fC
- Preamp rise time: 20 ns
- Detector capacitance: up to 100 fF
- Detector leakage current: up to 10 pA
- Shaper: 6th order, programmable peaking time
- Equivalent Noise Charge (simulation): 13 e rms at T=-30°C and a peaking time of 8 us

Chips have been supplied as naked dies (Fig. 3) and the corresponding test board developed for studying the main parameters of all building blocks jointly with SDD detectors.

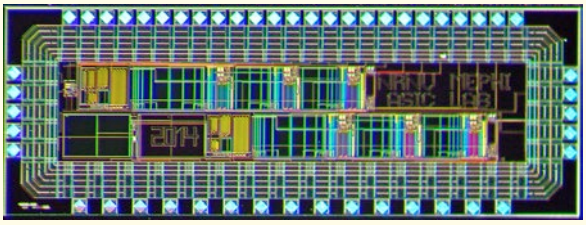


Fig.3 Chip photo

Why Europractice?

The Europractice IC service offers various routes to fabrication at favorable prices for use in the University both for education and research. It provides a unique opportunity for our University to have a well scheduled access to a wide range of state-of-the-art microelectronics technologies. A start-to-finish support of installation and usage of PDKs jointly with advanced CAD tools gives additional benefits to our designers.

The access via Europractice to a high quality mixed-signal CMOS fabrication process of AMS provided us with an invaluable experience for our microelectronic circuit design and further test activities. We are especially thankful to Europractice, which joined Russia since 2014 to the list of countries, getting discounted prices for manufacturing educational or publicly funded projects.

Acknowledgements

The work was done under the support of the Russian Foundation for Basic Research (www.rfbr.ru/rffi/eng), grant No.13-02-12094.

Reference

[1] PNDetector. Product brochure "Silicon Drift Detector". Update 2013. Available at http://pndetector.de/wp-content/uploads/2013/11/Brox_spreads_A4-pub.pdf

IHP

A Spectrum Sensing Platform for Cognitive Radio

Ulm University, Institute of Electron Devices and Circuits, Ulm, Germany

Contact: Peter Lohmiller, Václav Valenta
E-mail: peter.lohmiller@uni-ulm.de, vaclav.valenta@uni-ulm.de

Technology: IHP 0.25µm SG25H3 SiGe:C
Die size: 0.82 mm²

Introduction

A highly reconfigurable spectrum sensing platform is being developed at the Institute of Electron Devices and Circuits at the Ulm University. The platform consists of two principal subsystems: a customized frontend RFIC operating from 100 MHz-6 GHz and a flexible baseband DSP unit with a bank of sensing algorithms. Different sections of the analog front-end IC were implemented in the IHP's 0.25 µm SG25H3 BiCMOS technology in the framework of EUROPRACTICE. The frontend is based on an up/down-heterodyne architecture with the first IF located at 11.5 GHz. The second IF section provides a baseband bandwidth of 250 MHz per I and Q channel. A detailed description of one of the preliminary prototypes of the analog front-end is given in [1]. A simplified block diagram is shown in Fig.1.

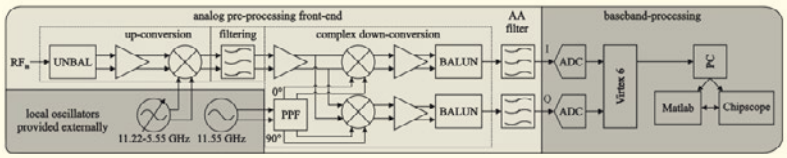


Fig.1: A block diagram of the spectrum sensing front-end. Both, analog and baseband sections are shown.

Description

Multi-chip approach has been adopted for the implementation of the preliminary prototype. A photograph of the realized module is shown in Fig.2. RFIC1 is LNA, RFIC2 is the first up-converting stage and RFIC3 is the complex direct down-converter. The role of the off-chip Microstripline bandpass filter (MSL) is to select the required band and limit the overall signal bandwidth. It thus reduces the integrated input power of subsequent stages and hence relaxes their linearity requirements.

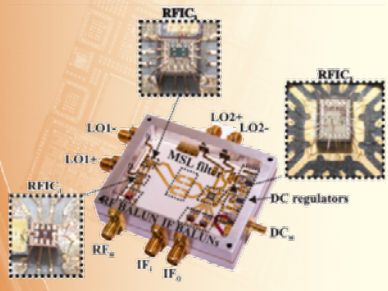
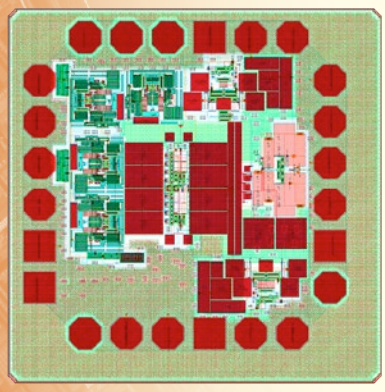


Fig.2: One of the first prototypes of the realized multi-chip sensing module.



In the next step, the individual RFICs will be integrated into a single IC in the SG25H3 technology. The complete sensing units that will integrate both RF and baseband subsystems are intended to be deployed in a collaborative sensing network to monitor the use of the radio spectrum.

Acknowledgement

This project is partially funded by the German Research Foundation DFG under grant no. VA941/1-1.

References

[1] P. Lohmiller, A. Elsokary, S. Chartier, H. Schumacher, "Highly flexible cognitive radio spectrum sensing front-end," Radio and Wireless Symposium (RWS), 2014.

imec

Topological Edge States in Silicon Photonics

Joint Quantum Institute, Department of Electrical and Computer Engineering, University of Maryland, College Park, Maryland, USA

Contact: Sunil Mittal, Mohammad Hafezi
Email: mittals@umd.edu, hafezi@umd.edu

Technology: IMEC Standard Passive, LETI Standard with Heaters
Die size: 3.7 mm x 7 mm

Under the influence of a magnetic field, at low temperatures, charged particles confined in two-dimensional systems exhibit a remarkable range of macroscopic quantum phenomena such as the quantum Hall effects. A hallmark of these phenomena is the presence of unidirectional, topologically robust edge states – states which are confined to the edge of the system.

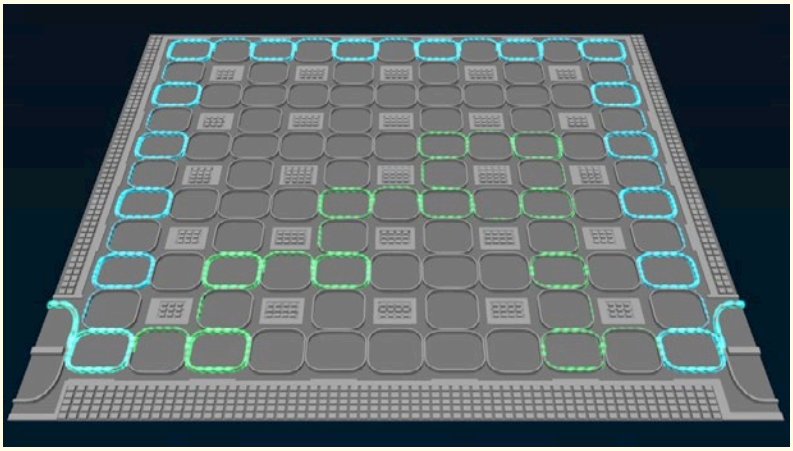


Fig. 1: 2D lattice of ring resonators. The edge state transmission is highlighted in blue. The green shaded path is an example of transmission through bulk states.

At UMD, we engineer a synthetic magnetic field for photons and hence achieve photonic analogs of the robust electronic edge states. We use a two dimensional lattice of ring resonators (Fig. 1), fabricated using the silicon-on-insulator technology from IMEC and LETI. The ring resonators are coupled using evanescent coupling which allows photons to hop from one ring to its neighbors. The rings are asymmetrically placed such that a photon hopping from left to right acquires a different phase than that hopping along the reverse direction. It is this direction dependent phase which simulates a magnetic field for photons and gives rise to topologically robust edge-states.

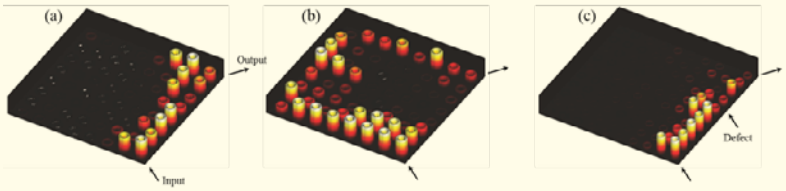


Fig. 2: Experimentally observed ring intensity for an 8 x 8 lattice array. (a) The CW edge state, (b) the CCW edge state, (c) edge state routing around a defect without scattering into bulk.

Fig. 2 shows the experimentally observed ring intensity distribution on a square lattice of 8 x 8 rings. When the input light frequency is in a specific transmission band, we see that the light injected at the input port travels along the edge of the lattice, circulating in a clockwise (CW) direction (Fig. 2(a)). For another transmission band, the input light takes a counter-clockwise (CCW) path along the lattice edge (Fig. 2(b)). These CW and CCW states therefore travel a long and a short path, respectively, from the input to the output port and hence experience different delays. More importantly, we see that the topological nature of these edge states enables these states to traverse sharp corners along the lattice edge, without scattering into the bulk of the lattice.

To further show the robustness of these edge states against lattice disorders, we fabricated a device which had a missing ring along a lattice edge. In the absence of topological protection, such an extreme defect would cause light to scatter into the bulk of the lattice. However, we observe that the edge state in fact routs around the defect, without scattering into the bulk. This demonstrates the topological robustness of the edge states.

Using the LETI passives with heater technology, we can now tune the strength of the local magnetic field and explore various other interesting phenomena which are difficult to access in atomic and electronic systems.

Why Europractice?

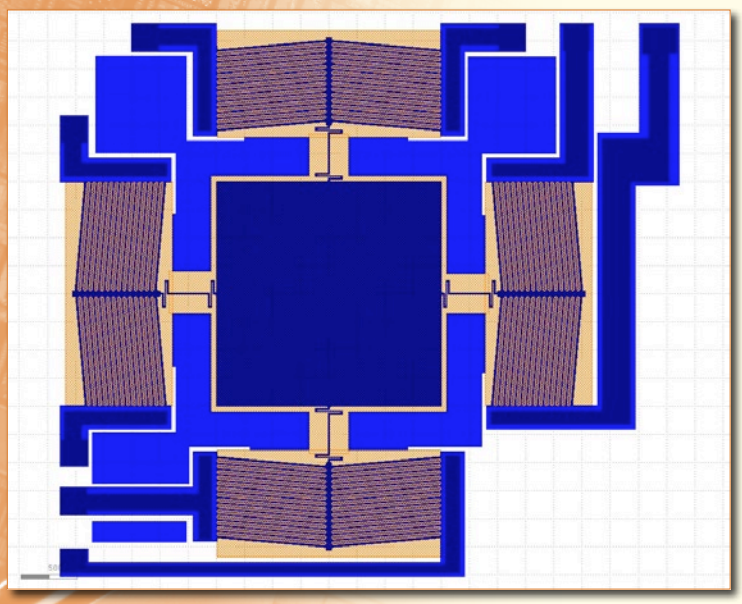
Europractice has enabled us to implement our design in a very short time, without going through the hassles of fabrication. Another big advantage is the availability of a variety of standard library elements, which means we spend less time simulating and optimizing those components.

References

Hafezi, M., Demler, E., Lukin, M. & Taylor, J. Robust optical delay lines with topological protection. Nat. Phys. 7, 907–912 (2011).

Hafezi, M., Mittal, S., Fan, J., Migdall, A. & Taylor, J. M. Imaging topological edge states in silicon photonics. Nat. Photonics 7, 1001–1005 (2013).

MEMSCAP



MEMS Microstage layout

A SOIMUMPS MEMS positional microstage for thermal experiments at high magnifications

National EPSRC XPS User Service (NEXUS), Newcastle University, School of Mechanical and Systems Engineering, United Kingdom

Contact: Dr Jose Portoles
E-mail: jose.portoles@ncl.ac.uk

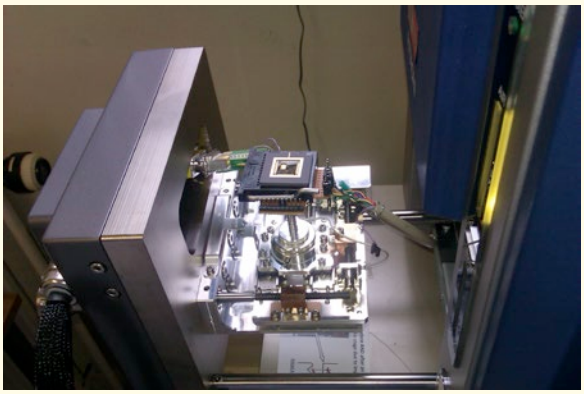
Technology: SOIMUMPS
Die size: 11x11 mm

Introduction

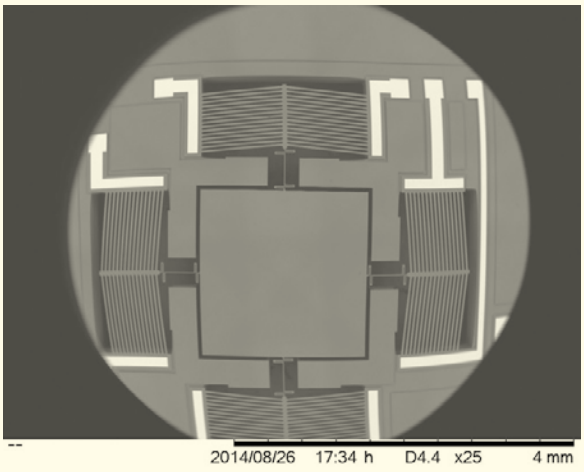
NEXUS is the National EPSRC X-ray photoelectron spectroscopy (XPS) Users Service currently providing XPS measurements and spectral analysis for the UK academic community. In the last years the demand for temperature controlled measurements has been rising significantly. This led us to consider solutions to provide temperature controlled measurements also for other techniques within NEXUS, and in particular in a recently acquired Omicron Nanofab Helium ion microscope.

Application

The magnification achieved with this technique poses the challenge to keep submicron samples steady in the field of view under thermal expansions resulting from temperature control. This problem has been addressed with the design of a SOIMUMPS in-plane MEMS positional microstage manufactured through Europractice. Our design provides a 2x2 mm sample holder for tiny samples such as powder nanoparticles or other nanostructures. In plane position can be smoothly controlled in X and Y inside the micron and submicron range by a set of four thermal actuators. Control of the out of plane position is not critical in the He-ion microscope due to large depth of field which makes a MEMS solution ideal. The device was initially tested inside an SEM microscope with a vacuum electrical feedthrough that provides the connections to control the four thermal actuators with external electronics. The chip was directly mounted on a ceramic microheater for temperature control. The device was succesfully applied to compensate thermal expansion effects up to about 350 °C and it is expected to demonstrate its full performance soon in NEXUS new He-ion microscope instrument. The initial test under the SEM showed also great applicability for the electron microscope.



MEMS Microstage mounted on the analysis chamber of a Hitachi TM-3030 SEM



MEMS Microstage SEM view

Why Europractice?

We have long been involved with the application of MEMS in several research areas [1][2] such as force metrology, mass sensing and instrumentation. Europractice access to Standard process MPW schemes such as PolyMUMPS and SOIMUMPS fulfils most of our needs for prototyping and demonstration of concept at an affordable cost, allowing us to speed up the development process. We have also greatly benefited from the excellent support provided by Europractice staff.

References

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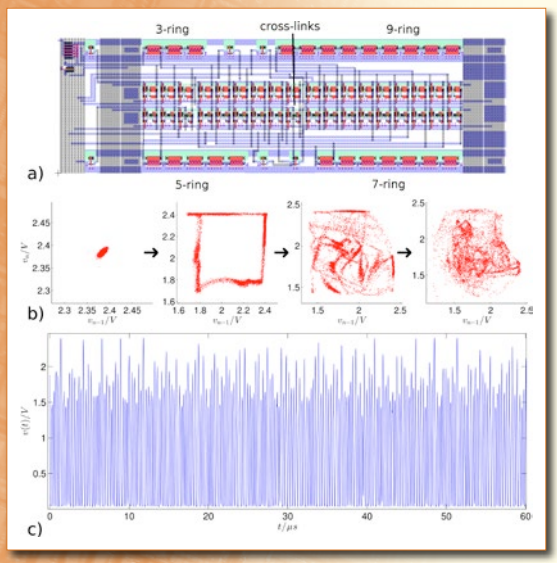
ON Semi

A CMOS spiking chaotic oscillator based on cross-linked inverter rings

University of Trento (academic host institution), **Tecno77 S.r.l.** (design implementation support)

Contact: Ludovico Minati
E-mail: lminati@ieee.org, ludovico.minati@unitn.it
Technology: ON Semi 0.7um
Die size: 5 mm²



Application

Some aspects of the relationship between brain network topology and dynamics can be remarkably recapitulated in small networks (30-90 nodes) of diffusively coupled single-transistor chaotic oscillators tuned at criticality, wherein dense connectivity promotes transition to chaos in regions hardwired as "hubs", as is observed in human functional neuroimaging data [1]. While the results are inspiring, it is necessary to replicate and extend them in a more realistic scenario, involving a larger number of nodes and connections and thus calling for a high-density monolithic implementation. The core feature of the single-transistor oscillators presently in use is that chaos is generated through the "quasiperiodicity" route, that is via overlap of multiple oscillation modes at non-trivial frequency ratios; these oscillators involve large discrete capacitors and inductors [2,3]. Here, this concept was re-engineered in an architecture that is very area-efficient for CMOS integrated implementation, in particular given that it does not involve any capacitors or inductors.

Results

The prototype chaotic oscillator is based on four inverter rings having n=3, 5, 7 and 9. These are "cross-linked" by means of diodes with diverse strength enabled via pass-gates (layout cell in Fig. a). The architecture of the "cross-links" is such that the higher n rings can be progressively coupled to the 3-ring, leading to a gradually more complex signal in the form of positive spikes of approximately constant periodicity but very variable amplitude (Fig. b,c for Poincaré plots and example waveform). This is very similar to observations on the single-transistor oscillator currently in use [2,3]. Multiple oscillator cells can be coupled easily and preliminary results on the current IC including 24 cells suggest that spontaneous formation of preferentially-synchronized communities occurs. These results provide motivation for further work on a much larger chip with neuromorphic connectivity.

Why EuroPractice?

This was an exploratory design initiated on personal initiative partly for own development and study, and partly to spearhead a future individual grant application, and as such the investigator chose to self-fund it directly. Without the availability of the *mini***@sic** MPW program this would simply not have been economically feasible.

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[3] L. Minati, Chaos 24, 043108 (2014)

TSMC

A 1/f Noise Up-conversion Reduction Technique Applied to Class-D Oscillator

Delft university of Technology, Delft, The Netherlands

Contact: Mina Shahmohammadi, Masoud Babaie, Robert Bogdan Staszewski

Technology: TSMC 40nm CMOS LP

The 1/f (flicker) noise up-conversion degrades the close-in spectrum of CMOS RF oscillators. The resulting $1/f^3$ phase noise (PN) can be an issue in PLLs with a loop bandwidth of ‹1MHz, which practically implies all cellular phones. Noise filtering technique [1] and adding resistors in series with gm-devices drain [2] have demonstrated significant reduction of $1/f^3$ oscillator PN corner. However, the former needs an additional tunable inductor and the latter degrades PN in the 20 dB/dec region, especially in the oscillators with low VDD and high current consumption.

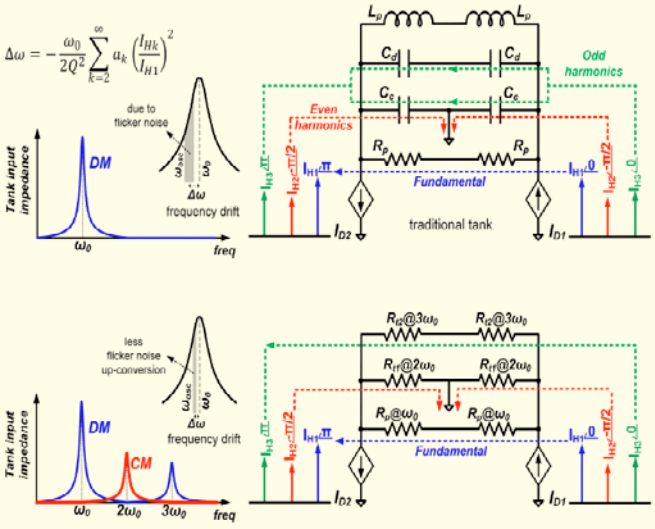

Fig. 1. Current harmonic paths and frequency drift.

The flicker noise can up-convert via two major phenomena. First, tail current flicker noise can modulate the oscillating waveform amplitude, which can convert to PN through a nonlinear C-V characteristic of varactors and active devices. The second mechanism is the Groszkowski effect [3]: The presence of harmonic components of the active device current can cause a frequency drift of the tank resonance (see Fig. 1-top). The fundamental drain current I_{H1} flows into R_p (equivalent parallel resistance of the tank), while its 2nd and 3rd harmonic components, I_{H2} and I_{H3}, mainly take the capacitance path due to its lower impedance. As a consequence, the reactive energy stored in the inductance and capacitance is perturbed, shifting the oscillation frequency $\Delta\omega$ lower to satisfy the resonance condition. This shift is static but any variation in the I_{H2} (or I_{H3}) to I_{H1} ratio due to the 1/f noise can modulate $\Delta\omega$ and show itself as the $1/f^3$ PN, see Fig. 1 (top-left). This phenomenon is clearly visible and now *dominant* in oscillators with the customary tail current source transistor removed, which is the trend in nanoscale CMOS.

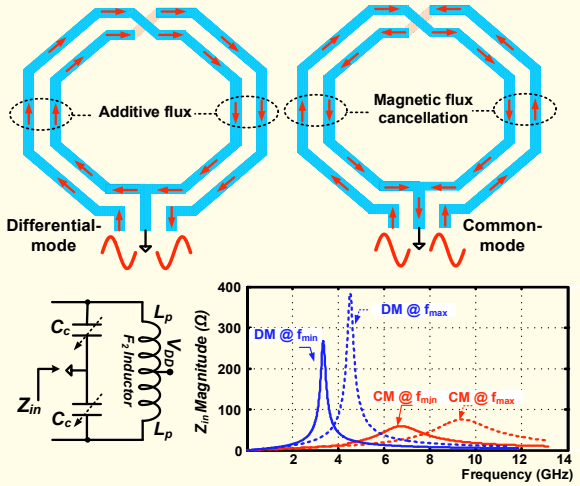

Fig. 2. F2 inductor, F2 tank and its input impedance. F2 inductor.

Suppose the tank input impedance Z_{in} demonstrates other peaks at the strong harmonics of the fundamental frequency ω0. These harmonics would mainly flow into their relative equivalent resistance of Z_{in} instead of its capacitive part, as is shown in Fig. 1- bottom. Consequently, Groszkowski's effect on the 1/f noise up- conversion will reduce significantly. Specifically core transistor flicker noise modulates the 2nd harmonic of oscillator's virtual ground. This modulation generates 2nd harmonic current in the parasitic C_{gs} capacitors and gets injected to the tank. Consequently, the I_{H2} component is usually the main contributor to the frequency shift. In this work we introduce a tank topology that effectively traps I_{H2} in its resistive part without the cost of an extra area. The tank derives this characteristic from the different behavior of inductors and transformers in differential (DM) and common mode (CM) excitations.

Fig. 2 shows a 2-turn inductor in DM and CM excitations. In DM, the currents in each turn are in the same direction resulting in an additive flux, while in CM, the opposite currents cancel each other's magnetic flux. Due to this cancellation, the effective CM inductance is very low. The "F_2 inductor" is designed with appropriate spacing between the windings and demonstrates a 4x smaller effective inductance for CM inputs than for DM inputs. The CM input signals cannot see the differential capacitances, hence to be able to set a CM resonance, the capacitors across the tank have to be single-ended. The input impedance of the F_2 tank, Z_{in}, demonstrates two resonant frequencies, $\omega_{DM}=\omega_0$, and $\omega_{CM}=2\omega_0$. The precise inductor geometry controlled by lithography maintains $L_{DM}/L_{CM}\approx 4$ and hence $\omega_{CM}/\omega_{DM}\approx 2$ over the full tuning range, TR. The lower and broader CM impedance, compared to that of DM, guarantees the 2nd harmonic current flowing mainly to the additional resistive part, even if CM resonant frequency is mistuned by 10%.

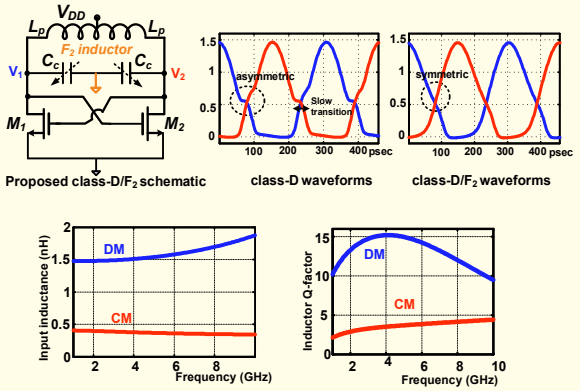

Fig. 3. Class-D/F2 oscillator, its waveform and inductance characteristics.

To demonstrate how this technique can reduce the flicker noise up-conversion, we employ the F_2-tank to a class-D [4]. This class of oscillator is chosen for its strong amount of I_{H2}. The original class-D oscillator shows promising performance in the $1/f^2$ region but it suffers from the strong 1/f noise up-conversion and frequency supply pushing. All known mitigation techniques (e.g., [5]) seem either ineffective or unsuitable. As shown in Fig. 3- top, the class-D/F_2 oscillator adopts the F_2 tank. The gm-devices M_1 and M_2 inject a large I_{H2} current into the tank due to the ground- clipping of signals. Fig. 3 also compares class-D and D/F_2 waveforms. Clearly the rise/fall times are more symmetric in the class-D/F_2 oscillator, which translates to lower DC value of gm- transistors' ISF function and thus lower the 1/f noise up-conversion. The class-D oscillator shows 0.8~2.5MHz $1/f^3$ corner frequency. A version of class-D with a tail filter technique [5] was also designed in [4]. A resonator at 2ω0 is interposed between the common source of the transistors and ground. This method is only partially effective, lowering $1/f^3$ PN corner to 0.6~1MHz, since it only linearizes the gm device and partially reduces the I_{H2} amount. Our method traps IH2 in the tank and simulations predict the $1/f^3$ PN corner of ‹50 kHz.

The class-D/F_2 oscillator was prototyped in 40 nm 1P8M CMOS process without ultra-thick metal layers. The chip micrograph is shown in Fig. 6. The tank employs a 1.5nH inductor with simulated Q-factor of 12 at 3GHz. $M_{1,2}$ are (200/0.04) μm low-V_t devices which guarantee start-up and class-D operation over PVT. The oscillator is tunable between 3.3– 4.5GHz (31% TR) with a 6-bit MOM capacitor bank.

Fig. 4 shows the PN plots at f_{max} and f_{min} oscillation frequencies, with V_{DD}=0.5V. The $1/f^3$ PN corner is ~100 kHz at f_{max} and reduces to 60 kHz when all switches are on at f_{min}.

In the oscillator the PN in the $1/f^2$ region fits well with the simulations. However, the $1/f^3$ PN corner is at least ~2x higher than expected mainly due to a $2\omega_0$ disturbance on the supply rail created by the oscillator output buffer.

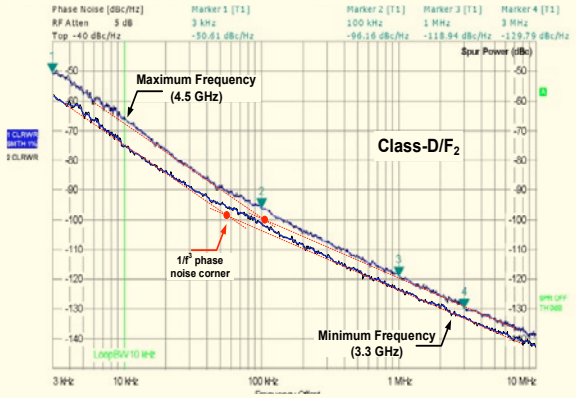

Fig. 4. Class-D/F2 measured PN.

		Class-D/F_2		Class-D [4]		Noise Filtering Class-D [4]	
Technology		40 nm		65 nm		65 nm	
Thick metal		No		Yes		Yes	
V_{DD} (V)		0.5		0.4		0.4	
Tuning range (%)		31		45		45	
OSC core area		0.1 mm²		0.12 mm²		0.15 mm²	
Freq. (GHz)		f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}
		3.3	4.5	3	4.8	3	4.8
P_{DC} (mW)		4.1	2.5	6.8	4	6.8	3.6
PN (dBc /Hz)	100kHz	-101.2	-96.2	-101	-91	-102	-92.5
	1MHz	-123.4	-119	-127	-119	-128	-121
	10MHz	-143.4	-139	-149.5	-143.5	-150	-144.5
FoM† (dB)	100kHz	185.4	185.3	182.2	178.6	183.2	180.56
	1MHz	187.6	188	188.2	186.6	189.2	189.06
	10MHz	187.6	188	190.7	191.1	191.2	192.56
1/f³ corner (kHz)		60	100	800	2100	650	1500
Freq. pushing (MHz/V)		40 @0.5V	60 @0.5V	140 @0.5V	480 @0.5V	90 @0.5V	390 @0.5V

†FOM= $|PN|+20\log_{10}(\omega_0/\Delta\omega)-10\log_{10}(P_{DC}/1mW)$

Fig. 5. Performance comparison with relevant oscillators.

Fig. 5 summarizes the oscillator performance and compares it with the counterpart reference designs. Even with the performance degradation due to the unavoidable supply sharing, this technique demonstrates ›10–15x improvement in the 1/f³ PN corner in class-D with no extra area penalty. It also significantly improves supply pushing.

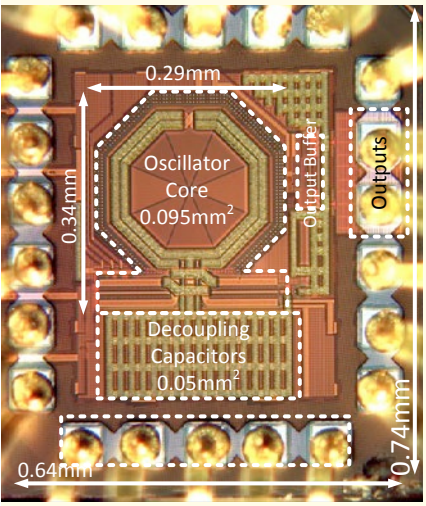

Fig. 6. Chip micrograph.

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An 8 bit current-steering DAC for a GSM transmitter

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[2]Politehnica University of Bucharest, Department of Electrical Engineering, Romania

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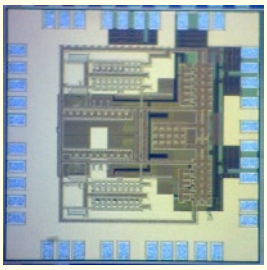
Technology: TSMC 0.18 mixed signal
Die size: 1570 x 1570µm



Note

This text is part of the same title and authors paper published on ISFEE 2014 Conference, Nov 28-29, Bucharest, Romania.

Description of the chip and the application

The placement of the digital to analog converter (DAC) as close to the antenna as possible improves the performances of wireless transmission chains [1]. A common solution is to use a current steering DAC, which provides a large resolution range, high speed and an adequate spurious free dynamic range (SFDR) [1]. In previous works [2, 3] a segmented 5+3 architecture of the current steering DAC has been discussed, the main blocks being designed using a generic design kit of a 90µm technology provided by CADENCE. A new calibration method with using two algorithms for correction current value has been proposed [2, 3]. In [7] a complete layout design of this segmented 5+3 architecture of the current steering DAC is presented. This design has been done using the TSMC 0.18 mixed signal 1P6M technology. The IO pads were provided by TSMC. The simulations were done using SPECTRE and SPECTRE APS, and the layout was done using Virtuoso Layout Editor and verified with an ASSURA flow. A value for the SFDR of at least 50dB in the 10MHz bandwidth has been targeted.

A single current cell includes a latch in the top, MOS switches in the middle and the current source in the bottom. For a better matching of the MOS switches the transistors are split into fingers that are mixed. The current cells are arranged in a

matrix of 4 rows and 8 columns. Dummy cells were also added to minimize grading effects and to keep the same neighbors, so that the resulting matrix now has 6 rows and 10 columns. In order to avoid latchup all NMOS transistors are surrounded by a p-plus guard ring connected to ground and all the PMOS transistors are surrounded by an n-plus guard ring connected to the supply source. The routing was done solely on the metal layers, because the poly layer would add an unwanted parasitic resistance. The layout of the clock and the outputs lines for the calibration circuit has been designed using an H-tree structure, which ensures an equal delay for all the matrix cells. Plus, the differential output lines were routed in parallel on the third and fourth metal layers. The top metal is an ultra-thick layer and was used for the ground routing because of the lower resistivity. Moreover, small capacitors have been added at the 31 outputs of the thermometric decoder for filtering purposes. The correction current sources used for the DAC calibration are controlled using a serial to parallel interface. This was implemented using 72 latches, 62 for the correction sources control, and the remaining ones for other functions.

The dimensions of one DAC are 750 x 300µm. The die (see the figure) contains two DACs and the serial to parallel interface with 72 cells, as well as decoupling capacitors that reduce the noise on the digital supply. The digital domains are separated from the analog domain in order to improve the noise characteristic [1], while also providing an adequate ESD protection. The IO pads have been provided by TSMC and were chosen to have the smallest capacitance (few hundreds fF) so it would not influence the circuit.

Results

The following table presents a comparison with other DAC implementations in the same or close technology nodes. It can be observed that for the same technology, the converter in this paper has a better SFDR, while using a much higher sample rate.

If it is compared with a converter designed in a smaller technology node [6], our converter has a similar SFDR value, occupying an area three times smaller.

Why Europractice?

Europractice offers to universities and research laboratories the chance to prototype their ASIC designs at affordable prices, using the *mini***@sic** concept. Packaging services are available also. In addition, the excellent support was of valuable help for our project.

Acknowledgment

This work has been funded partially by a grant of the Romanian National Authority for Scientific Research, CNCS – UEFISCDI, project number PN-II-RU-PD-2011-3-0246. The contribution of M.-E. Marin has been supported by the Sectorial Operational Programme Human Resources Development 2007-2013 of the Ministry of European Funds through the Financial Agreement POSDRU/159/1.5/S/134398.

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Parameter	This work	[4]	[5]	[6]
Technology	180nm	180nm	180nm	130nm
Supply voltage	1.5V/2.5V	1.8V	1.8V	1.2V
Sample rate	1GSPs	500MSPs	500MSPs	650MSPs
SFDR	51.5dB @10MHz	35.42dB @10MHz	44.83dB @10MHz	56dB @3MHz
Power	15mW	-	7.88mW	18mW
Area	0.23mm	-	-	0.6mm

UMC

IC Design Projects as part of Master Curriculum

ETH Zurich, Integrated Systems Laboratory (IIS), Switzerland

Contact: Hubert Kaeslin, Norbert Felber, Frank K. Gurkaynak, Luca Benini
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Description of the project

For more than 25 years, the Integrated Systems Laboratory has been offering a VLSI Design course in three parts. The course follows a top-down approach and in the first part offered during the 6th semester the students learn how to map algorithms to hardware architectures and learn the basics of HDL design. The second course during the 7th semester focuses on the back-end design and implementation issues while the final part of the course covers testing and manufacturing. The unique aspect of our course is that we are able to offer practically all students that are interested to develop their own ASICs as part of an accompanying semester thesis. Teaching materials for this course have been collected in a textbook that has recently appeared as a second edition [1].

Towards the end of the first course, research assistants from our institute present possible design ideas to the students. Interested students can then select one of these topics and work on these projects (interested students can also suggest their own ideas). We prefer that students work in groups of two. Each group is assigned at least one supervisor who is working on the field. This allows the students

to be part of the research activities in our group as well. Assisted by laboratory exercises that explain various stages of the design flow, the students are able to finish a standard cell based digital design within a semester that lasts for 14 weeks. At the end of the semester the designs are taped out (in January), and if there are no unexpected delays, the fabricated chips arrive back from fabrication during the following semester. This allows the students to test their own ASICs as part of the exercises of the last part of the course that focuses on testing. Students that take advantage of this course will have designed and tested their own ASICs even before starting their Master Thesis projects. Each year 6 to 10 student designs are realized this way.

For the 2013-2014 edition of our VLSI lecture series, a total of 7 ASIC projects were realized using the UMC 180nm process. We have chosen to reserve a 5mm x 5mm frame through Europractice IC service and asked this frame to be subdivided into nine equal parts (compatible with the *mini***@sic** sizes used by Europractice). All except one design use an identical padframe of roughly 1.5mm on one side. The remaining design is larger, twice the size of the other designs. The student designs therefore accounted for eight out of the nine subdivided regions. The last part was occupied by a design from our own research group. A photomontage of fabricated chips can be seen in Fig. 1.

Results

The chips manufactured for the 2013-2014 VLSI lecture series have diverse application fields such as cryptography, low power processors, audio systems and telecommunication. Cronorx (a) implements one of the candidate algorithms for the Caesar competition that is evaluating authenticated encryption with associated data algorithms. Zorro (d) and Halley (g) are also designs from the cryptography field. Zorro implements different countermeasures against differential power analysis attacks, while Halley is an Application Specific Instruction set Processor (ASIP) tailored to verify digital signatures according to the Elliptic Curve Digital Signature Algorithm (ECSDA). Or10n is an efficient low-power implementation of the Open-RISC processor core, and Sir10us (c) is a re-implementation of Halley that couples the ECSDA ASIP with the Or10n processor.

As its name implies, 3Daudio (h) is a co-processor that has been designed to calculate Head Related Transfer functions which are used to transform a multi-channel audio recording to create a two-channel output for surround headphone listening. The largest student chip, Lazy Gonzales (b) is a turbo decoder for the LTE/LTE-Advanced standard. Finally, Thermite (e), a test chip for physically unclonable functions used in the crypto, is the only chip not developed by students of the VLSI course. More detailed specifications of past and present chips can be found on our chip gallery http://asic.ethz.ch.

All chips have been tested by the students that have designed them using our own in house Advantest SoC93000 ASIC tester and were found to be fully functional. The results of one chip (Sir10us) has already been published [2] and we expect the results of several other chips to be published in the near future as well.

Why Europractice?

We have been using the MPW services of Europractice as well as EDA tools licensed to ETH Zurich through the Europratice software services for more than 10 years. In addition to the standard services, Europratice members have been instrumental in helping us explore new technologies, plan MPW tape-out dates so that student chips can come back within the semester allowing the students to test them. With their help, for the 2014-2015 edition of the VLSI course we have moved to UMC 65nm technology for the student designs.

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Dual-mode Blocks of the Integrated Circuit GALILEO and GPS Signal Receiver for Precise Positioning of Mobile Objects

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Technology: UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V
Die size: 2 dies: 1525 x 1525 µm each

Description - application

Commercial navigation systems have become very popular in recent years. For that reason low-cost multistandard Galileo/GPS fully integrated receiver is desirable. Usage of two Global Navigation Satellite Systems (GNSS) improves accuracy and reliability of positioning devices. It is especially important in highly urbanized areas where signal quality is reduced by high buildings.

This work presents two full RF Front-Ends for both E1/L1 (Fig. 1) and E5/L5 (Fig. 2) bands and two navigation systems Galileo and GPS. It employs Low-IF architecture and works with 1.2 V ±10% power supply only. The aim was to achieve the minimum power consumption in the receiver by using the newest analogue design techniques and new allocation schemes of individual specifications of the building blocks.

In this case we have a couple of blocks on each die: a single-ended LNA stage followed by a Balun to create differential signal for a Mixer block designed as a quadrature Gilbert-cell. Each chip contains fully integrated PLL to provide LO frequency for the down-conversion mixer. The satellite signal from the passive 50 Ω antenna on the test PCB (Fig. 3) is amplified by the on chip LNA. Its implementation is based on the design methodology presented in [1]. Next, the amplified signal is filtered by external SAW filter and returns to on chip active Balun stage, which delivers differ-

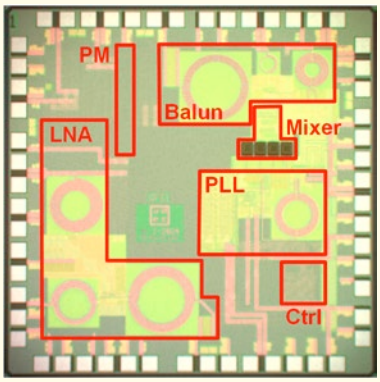

Fig. 1.: GFE1 top chip microphotography of RF Front-End for E1/L1 Galileo/GPS bands

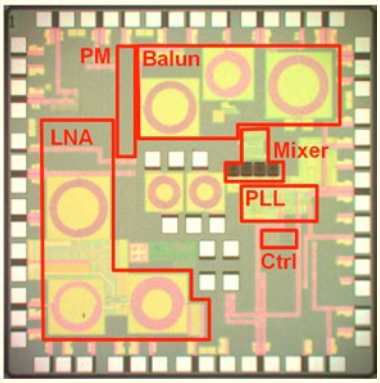

Fig. 2.: GFE5 top chip microphotography of RF Front-End for E5/L5 Galileo/GPS bands

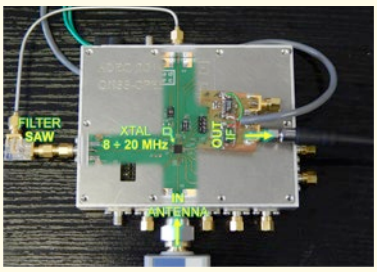

Fig. 3.: Test PCB for RF measurements of GNSS blocks

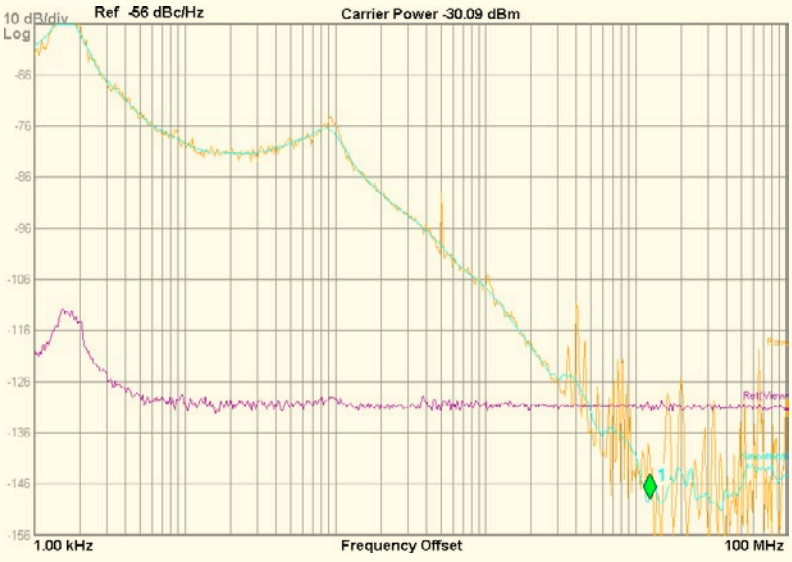

Fig. 4.: Measurements results of phase noise from E1/L1 PLL

ential RF signal to the Mixer cell. The last block is the LO generator – PLL, which core is based on LC-VCO (for E1/L1 bands). The VCO works on 3.142656 GHz frequency and contains quadrature RF divider to achieve IF frequency at 4.092 MHz. The silicon proven LC-VCO and design methodology of the PLL were described in [2, 3]. This Fractional-N PLL uses the newest patented phase noise cancelation technique [4]. The measurement results of packed test chip shows that the phase noise of the PLL working in fractional mode is almost the same as in integer mode, so almost no fractional phase noise is introduced to the system (fig. 4). These two chips together with the third one (prototyped in *mini***@sic** run in 2013 via Europractice IC Service), which contains fully integrated IF receiver path for E1/L1+E5/L5 (LPF, VGA, ADC), create chipset for dual-band multi-constellation GNSS receiver. The next step will be full integration of those 3 chips together with in house developed 32-bits multi-core navigation processor into one silicon die.

Why Europractice?

The Europractice service was the best choice because offers MPW *mini***@sic** prototyping as well as low cost access for professional ASIC CAD design tools. Our University uses Eurochip – Europractice since 1993.

References

[1] J. Grądzki, T. Borejko, W. A. Pleskacz: "Low Voltage LNA Implementations in 90 nm CMOS Technology for Multistandard GNSS," Proceedings of the 2009 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems – IEEE DDECS 2009, pp. 78-83, Liberec, Czech Republic, April 2009.

[2] K. Siwiec, T. Borejko, W. A. Pleskacz: "PVT Tolerant LC-VCO in 90 nm CMOS Technology for GPS/Galileo Applications," Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2011, pp. 29-34, Cottbus, Germany, April 2011.

[3] K. Siwiec, T. Borejko, W. A. Pleskacz: "CAD Tool for PLL Design," Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2011, pp. 283-286, Cottbus, Germany, April 2011.

[4] K. Siwiec, W. A. Pleskacz: "Niskoszumny układ ułamkowej syntezy częstotliwości", Patent application no. P-410584, 17th December 2014.

[5] T. Borejko, W. A. Pleskacz: "A Resistorless Voltage Reference Source for 90 nm CMOS Technology with Low Sensitivity to Process and Temperature Variations," Proceedings of the 2008 IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems – IEEE DDECS 2008, pp. 38-43, Bratislava, Slovakia, April 2008.

LIST OF CUSTOMERS PER COUNTRY AND NUMBER OF DESIGNS THEY HAVE SENT IN FOR MPW FABRICATION

CUSTOMER	TOWN	Number of ASICs
Algeria		
CDTA	Algiers	1
Australia		
Edith Cowan University	Joondalup	11
La Trobe University	Bundoora, Victoria	3
Monash University	Clayton	9
Motorola Australian Ressearch Centre	Botany	1
Royal Melbourne Institute of Technology (RMIT)	Victoria	1
University of Adelaide	Adelaide	1
University of Melbourne	Melbourne	1
University of New South Wales	Sydney	12
University of Sydney	Sydney	6
University of Western Australia	Crawley	1
Austria		
A3Pics	Vienna	1
ARC Seibersdorf Research	Vienna	5
austriamicrosystems	Unterpremstaetten	74
Austrian Academy of Sciences	Wiener Neustadt	1
Austrian Aerospace	Vienna	2
Austrian Institute of Technology - AIT	Vienna	1
Carinthia Tech Institute	Villach-St.Magdalen	1
Fachhochschule Technokum Kaernten	Villach-St.Magdalen	5
FH Joanneum Graz	Graz	1
IEG	Stockerau	1
Johannes Keppler University	Linz	3
MED-el	Insbruck	2
Riegl Laser Measurement System	Horn	4
RUAG Aerospace Sweden	Vienna	1
Securiton	Wien	1
TU Graz	Graz	4
TU Wien	Vienna	20
University of Applied Sciences Technikum Wien	Vienna	1
Belarus		
NTLab	Minsk	11

CUSTOMER	TOWN	Number of ASICs
Belgium		
AnSem	Heverlee	3
Antwerp Space	Hoboken	4
Audax Technologies	Leuven	1
Browning International SA	Herstal	1
Caeleste	Antwerp	1
Cochlear Technology Centre Europe	Mechelen	9
ED&A	Kapellen	3
EqcoLogic	Brussels	52
FillFactory	Mechelen	2
ICI - Security Systems	Everberg	6
ICSense	Leuven	1
IMEC	Leuven	218
K.U. Leuven	Heverlee	155
Katholieke Hogeschool Brugge-Oostende	Oostende	23
KHK	Geel	13
KHLim	Diepenbeek	9
KIHA	Hoboken	2
Macq Electronique	Brussel	1
Neurotech	Louvain-la-Neuve	2
Q-Star Test nv	Brugge	2
SDT International	Bruxelles	1
SEBA Service N.V.	Grimbergen	1
SIEMENS ATEA	Herentals	2
SIPEX	Zaventem	4
Societe de Microelectronique	Charleroi	1
Universite Catholique de Louvain	Louvain-la-Neuve	19
Université de Mons, Faculte Polytechnique	Mons	9
Universiteit Gent	Gent	113
University of Antwerp	Wilrijk	3
Vrije Universiteit Brussel	Brussels	92
Xenics	Leuven	1
Brazil		
Centro de Tecnologica da Informacao Renato Archer Brasil	Sao Paulo	5
Centro Universitario da FEI	São Bernardo do Campo	1
CPqD - Telebras	Campinas	7
Federal University of Minas Gerais (UFMG)	Belo Horizonte	3
Genius Instituto de Tecnologia	Manaus - Amazonas	3
State University of Campinas - CenPRA	Campinas	29
UNESP/FE-G	Guaratingueta - SP	4
UNICAMP- University of Campinas	Campinas, SP	34
Universidade de Sao Paulo	Sao Paulo-SP	32
Universidade Federal de Santa Maria	Santa Maria	1
University Federal Pernambuco	Recife	8
University Fedral Santa Catrina	Santa Catrina	1
University of Brasilia	Brasilia	1
Bulgaria		
Technical University of Sofia	Sofia	5
Canada		
Canadian Microelectronics Corporation	Kingston, Ontario	25
Epic Biosonics	Victoria	4
NanoWattICs	Quebec	1
Queens University	Kingston, Ontario	1
Scanimetrix	Edmonton	12
TBI Technologies	Waterloo	1
TeraXion	Québec	1
University of Alberta	Edmonton	1
University of Toronto	Toronto	1
University of Waterloo	Waterloo	6
Chile		
Universidad Catolica de Chile	Santiago	2
China		
Beelab Semiconductor	Hong Kong	1
CETC38	Heifei	4
Chinese Academy of Science, Institute of Semiconductors	Beijing	1
Dept.Computer Science and Technology	Beijing	1
Fudan University	Shanghai	2
Hirain	Beijing	1
Hong Kong University of Science and Technology	Hong Kong	34
Microelectronics Center	Harbin	1
Peking University	Peking	1
Sun Yat-sen University	Guangzhou	1
The Chinese Univ. of Hong Kong - ASIC Lab	Hong Kong	19
The Chinese University of Hong Kong	Shatin-Hong Kong	44
Tsinghua University	Beijing	1
University of Macau	Macau	8
Xi'an Inst. of Optics & Precision Mechanics (CAS)	Xi'an	1
Zhejiang University	Yuquan	1
Costa Rica		
Instituto Tecnologico de Costa Rica	Cartago	1
Croatia		
University of Zagreb	Zagreb	6
Cyprus		
University of Cyprus	Nicosia	3
Czech Republic		
ASICentrum s.r.o.	Praha 4	6
Brno University of Technology	Brno	20
Czech Technical University-FEE	Prague	12
Institute of Physics ASCR	Prague	2
Denmark		
Aalborg University	Aalborg	52
Aarhus University	Aarhus	1
Aalto University	Aalto	9
Algo Nordic A/S	Copenhagen	1
Bang & Olufsen	Struer	4
DELTA	Hoersholm	11
GN-Danavox A/S	Taastrup	4
Microtronic A/S	Roskilde	1
Oticon A/S	Hellerup	14
PGS Electronic Systems	Frb.	1

CUSTOMER	TOWN	Number of ASICs
Techtronic A/S	Roskilde	1
Technical University of Denmark	Lyngby	18
Thrane&Thrane	Lyngby	1
Egypt		
American university of Cairo	Cairo	10
Bahgat Group - IEP	Cairo	4
Estonia		
Tallinn Technical University	Tallinn	1
Finland		
Aalto University	Espro	3
Detection Technology Inc.	Li	1
Fincitec Oy	Oulu	4
Kovilta Oy	Salo	1
Helsinki University of Technology	Espoo	9
Nokia Networks	Espoo	2
Tampere University of Technology	Tampere	8
University of Oulu	Oulu	23
University of Turku	Turku	3
VTI Technologies	Vantaa	2
VTT Electronics	Espoo	110
France		
Atmel	Nantes, Cedex 3	3
C4i	Archamps	14
CCESMAA -IXL	Talence	2
CEA	Grenoble	40
CMP-TIMA	Grenoble	7
CNES	Toulouse Cedex 01	4
CPPM	Marseille	2
Dibcom	Palaiseau	1
Dolphin Integration	Meylan	4
EADS Defense&security		1
Ecole Polytechnique route de Saclay , LPP	Palaiseau	1
ELA Recherche	Meylan	4
ENSEA	Cergy Pontoise	2
ENST Paris	Paris	2
ESIEE	Noisy Le Grand	3
IN2P3 - LPNHE - Universites 6 et 7	Paris Cedex 5	9
Institut de Physique Nucleaire	Villeurbanne	7
Institut des Sciences Nucleaires	Grenoble	5
Institut Sup. d Electronique de Bretagne	Brest	2
IRAP	Toulouse	1
ISAE	Toulouse Cedex	22
ISEN Recherche	Lille cedex	5
LAAS/CNRS	Toulouse	10
Labo PCC CNRS/IN2P3	Paris cedex05	2
Laboratoire de l Accelerateur Lineaire	Orsay	6
Laboratoire de Physique des Plasmas, LPP	Saint-Maur des Fossés	2
LAPP	Annecy-le-Vieux	7
LEA	Cesson Sevigne	1
LEPSI	Strasbourg	15
LETI-CEA	Grenoble	4

CUSTOMER	TOWN	Number of ASICs
LIRMM	Montpellier	2
Midi Ingenierie	Labege	1
MXM Laboratories	Vallauris	3
NeoVision France	Bagneux	3
NXP Semiconductor	Caen	2
PMIPS - IEF	Orsay	2
SODERN	Limeil-Brevannes	2
Subatech - IN2P3	Nantes	1
Supelec	Gif-sur-Yvette	3
TTPCOM	Sophia Antipolis	1
Universite Joseph Fourier	Grenoble	1
Universite Louis Pasteur - InESS	Strassbourg	3
Universite Pierre et Marie Curie	Paris	4
Vision Integree	Nogent sur Marne	3
Germany		
Acam	Stutensee	2
AEG infrarot-module		1
Albert-Ludwig University - IMTEK	Freiburg	7
ALV-Laser Vertriebsgesellschaft mbH	Langen	1
austriamicrosystems	Dresden	2
Balluff		1
Bergische Universitaet Wuppertal	Wuppertal	2
Biotronik GmbH & Co	Erlangen	9
Bruker AXS	Karlsruhe	3
Bruker Biospin		6
Cairos Technologies	Karlsbad	8
Comtech GmbH	St. Georgen	3
Daimler-Benz AG	Ulm	3
Darmstadt University of Technology	Darmstadt	3
Dr. Johannes Haidenhain		1
Escrypt	Bochum	1
ESM Eberline	Erlangen	1
ETA	Erlangen	1
Fachhochschule Aalen	Aalen	3
Fachhochschule Aschaffenburg	Aschaffenburg	3
Fachhochschule Augsburg	Augsburg	1
Fachhochschule Brandenburg	Brandenburg	15
Fachhochschule Bremen	Bremen	3
Fachhochschule Darmstadt	Darmstadt	9
Fachhochschule Dortmund	Dortmund	3
Fachhochschule Esslingen	Goeppingen	2
Fachhochschule Furtwangen	Furtwangen	6
Fachhochschule Giessen-Friedberg	Giessen	16
Fachhochschule Koeln	Gummersbach	3
Fachhochschule Mannheim	Mannheim	5
Fachhochschule Nuernberg	Nuernberg	1
Fachhochschule Offenburg	Offenburg	30
Fachhochschule Osnabrueck	Osnabrueck	4
Fachhochschule Pforzheim	Pforzheim	1
Fachhochschule Ulm	Ulm	19
Fachhochschule Wilhelmshaven	Wilhelmshaven	1
Fachhochschule Wuerzburg	Wuerzburg	1
FAG-Kugelfischer	Schweinfurt	3
FH Hannover	Hannover	5

CUSTOMER	TOWN	Number of ASICs
FH Karlsruhe	Karlsruhe	1
FH Niederrhein	Krefeld	5
FH-Münster	Steinfurt	1
FORMIKROSYS	Erlangen	2
Forschungszentrum Juelich GmbH	Juelich	3
Fraunhofer Heinrich - Hertz	Berlin	42
Fraunhofer IIS	Erlangen	257
Fraunhofer institute silicontechnology	Itzehoe	18
Fraunhofer IPMS	Dresden	7
Fraunhofer ISC		1
Friedrich-Schiller-University	Jena	3
GEMAC	Chemnitz	7
Gesellschaft für Schwerionenforschung	Darmstadt	45
Geyer	Nuernberg	6
GMD	St. Augustin	1
Hella		1
Helmholtz Zentrum München	Munchen	1
Hochschule Rhein Main	Rüsselsheim	1
Hochschule TWG	Konstanz	2
Hyperstone AG	Konstanz	1
iAd GmbH	Grosshabersdorf	1
IHP	Frankfurt(Oder)	1
IIP-Technologies GmbH	Bonn	6
IMKO Micromodultechnik GmbH	Ettlingen	3
IMMS	Ilmenau	3
IMST GmbH	Kamp-Lintfort	4
INOVA Semiconductor	Munich	1
Institut fuer Mikroelectronik Stuttgart	Stuttgart	2
Institut fur Mobil- und Satellitenfunktechnik	Kamp-Lintfort	13
Institute for Integrated Systemes	Aachen	1
Institute of Microsystem Techology	Freiburg	2
Jakob Maul GmbH	Bad Koenig	1
Joh.-Wolfgang-Goethe-Universitaet	Frankfurt	6
Johannes Gutenberg-Universitaet	Mainz	9
Karlsruher Institut fuer Technologie (KIT)	Karlsruhe	2
KVG Quatrz Crystal	Neckarbisch	1
Lenze GmbH	Aerzen	2
LHR Comtech	St. Georgen	1
MAN	Nüremberg	1
Marquardt GmbH	Rietheim-Weilheim	1
Max Planck Institute	Munchen	19
MAZ Brandenburg	Brandenburg	2
Med-El GmbH		1
MEODAT	Ilmenau	2
Metzeler Automotive		3
MPI-Halbleiterlabor	Munich	2
NeuroConnex	Meckenheim	2
Optek Systems Innovations		1
OPTRONICS		1
Phisikalisches Institut	Bonn	2
Preh Werke	NA	2
Rechner Industrieelektronik GmbH		1
Rohde & Schwarz	München	2
Ruhr-University Bochum	Bochum	8
RWTH Aachen	Aachen	61
Scanditronix Wellhöfer	NA	3
Schleicher GmbH & Co Relais-Werke KG		1
Schleifring und Apparatebau GmbH		3
Seuffer	Calw-Hirsau	5
Sican Braunschweig GmbH	Braunschweig	1
Siemens		4
Technical University Ilmenau	Ilmenau	78
Technical University of Berlin	Berlin	12
Technical University of Cottbus-Senftenberg	Brandenburg	1
Technische Hochschule Mittelhessen	Friedberg	1
TESAT-Spacecom	Backnang	4
Trias	Krefeld	1
Trinamic	Hamburg	1
TU Berlin	Berlin	16
TU Braunschweig	Braunschweig	26
TU Chemnitz	Chemnitz	12
TU Darmstadt	Darmstadt	18
TU Dresden	Dresden	34
TU Hamburg-Harburg	Hamburg	57
Universitaet Dortmund	Dortmund	2
Universitaet Duisburg - Essen	Duisburg	3
Universitaet Hannover	Hannover	14
Universitaet Kaiserslautern	Kaiserslautern	21
Universitaet Paderborn	Paderborn	18
Universität Rostock	Rostock	8
University of Bielefeld	Bielefeld	1
University of Bonn	Bonn	12
University of Bremen	Bremen	38
University of Erlangen-Nuernberg	Erlangen	39
University of Freiburg	Freiburg	11
University of Hamburg, HAW - Applied Sciences	Hamburg	2
University of Heidelberg	Heidelberg	99
University of Kassel	Kassel	5
University of Magdeburg	Magdeburg	13
University of Mannheim	Mannheim	36
University of Munich	Munich	1
University of Oldenburg	Oldenburg	1
University of Saarland	Saarbruecken	4
University of Siegen	Siegen	20
University of Stuttgart	Stuttgart	5
University of Ulm	Ulm	50
University of Wuppertal	Wuppertal	2
Vishay semiconductor	Heilbronn	2
Wellhoeffer	Schwarzenbruck	2
Work Microwave GmbH	Holzkirchen	1
Greece		
ACE Power Electronics LTD	AG Dimitrios	1
Aristotle Univ. of Thessaloniki	Thessaloniki	12
Athena Semiconductors SA	Alimos - Athens	2
Crypto SA	Marousi	1
Datalabs	Athens	1
Democritus University of Thrace	Xanthi	6
Found. for Research and Techn.-Hellas	Heraklion	1
HELIC SA	Athens	1
Hellenic Semiconductor Applications	Athens	2
InAccess	Athens	1

CUSTOMER	TOWN	Number of ASICs
Intracom	Paiania	1
National Tech. Univ. of Athens	Athens	17
NCSR	Athens	23
NTNU	n/a	2
RETECO LTD.	Athens	1
Technical University of Crete	Crete	1
Technological Educational Institute of Chalkis	Chalkis	3
Unibrain SA	Athens	1
University of Athens	Athens	1
University of IONNINA	Ioannina	2
University of Patras - VLSI Laboratory	Rio - Patras	24
Hungary		
Hungarian Academy and Science	Budapest	2
Peter Pazmany Catholic University	Budapest	5
Computer and Automation Inst.	Budapest	6
JATE University	Szeged	1
India		
Bengal Engineering and Science University	Shibpur	1
Birla Institute of Technology and Science	Pilani	1
CEERI	Pilani	10
College of Eng. Guindy Anna Univesity	Chennai	2
Concept2Silicon Systems	Bangalore	1
Electronics Corporation of India	Hyderabad	19
imec India	Bangalore	2
Indian Institute of Science	Bangalore	25
Indian Institute of Science	New Dehli	13
Indian Institute of Technology - Bombay	Mumbai	26
Indian Institute of Technology - Gandhinagar	Gandhinagar	1
Indian Institute of Technology - Madras	Chennai	48
Indian Institute of Technology - New-Dehli	New Dehli	30
Indian Institute of Technology, Kanpur	Assam	5
Indian Institute of Technology, Kharagpur	Kharagpur	13
Integrated Microsystem	Gurgaon	1
International Institute of Info. Technology	Hyderabad	1
National Institute of Technology Trichirappalli	Trichirappalli	4
National Institute of Technology Warangal	Warangal	1
National Institute of Technology, Hyderabad	Hyderabad	5
National Institute of Technology, Karnataka	Surathkal	1
SITAR	Bangalore	28
TIFR	Colaba	1
VECC	Kolkata	6
Ireland		
ChipSensors Ltd	Limerick	3
Cork Institute of Technology	Cork	4
Duolog LtD	Dublin	2
National University of Ireland	Kildare	3
Farran Technology	Ballincollig	1
Tyndall National Institute	Cork	21
Parthus Technologies (SSL)	Cork	7
TELTEC	Cork	1
University College Cork	Cork	15
University of Limerick	Limerick	17
Waterford Institute of Technology	Waterford	8

CUSTOMER	TOWN	Number of ASICs
Israel		
Bar Ilan University	Ramat Gan	1
Check - Cap Ltd	Isfiya	1
CoreQuest	Petach Tikva	2
DSP Semiconductors	Givat Shmuel	1
Technion - Israel Institute of Techn.	Haifa	4
Tel Aviv University	Tel Aviv	10
Italy		
Agemont	Amaro	2
Alcatel Alenia	L'Aquila	1
Alimare SRL	Favria Canavese (Torino)	1
Aurelia Microelettronica S.p.A.	Navacchio PISA	18
BIOTRONIC SRL	San Benedetto	1
Cesvit Microelettronica s.r.l.	Prato	2
DEEI - University of Trieste	Trieste	2
Elements	Cesena	1
Eye-Tech	Portenone	2
Fondazione Bruno Kessler	Trento	58
Fondazione CNAO	Pavia	1
IIT Genova	Genova	6
IIT Torino	Torino	4
INFN	Bari	1
INFN	Bologna	1
INFN	Cagliari	3
INFN	Catania	15
INFN	Ferrara	1
INFN	Genova	2
INFN	Milano	14
INFN	Padova	4
INFN	Pavia	3
INFN	Pisa	1
INFN	Roma	7
INFN	S.Piero a Grado (PISA)	2
INFN	Torino	11
INFN	Trieste	11
Instituto di Sanita	Roma	4
ISE	Vecchiano	1
Italian Institute of Technology	Genova	12
LABEN S.p.A.	Vimodrone (MI)	3
Microgate S.r.L	Bolzano	6
Microtest	Altopascio	1
Neuricam	Trento	3
Optoelettronica Italia	Terlago	1
Politecnico di Bari	Bari	8
Politecnico di Milano	Milano	138
Politecnico di Torino	Torino	7
Scuola Superiore Sant'Anna	Pisa	5
Silis s.r.l	Parma	1
Sincrotrone Trieste SCpA	Trieste	3
SITE Technology s.r.l.	Oricola	1
SYEL S.r.l.	Pontadera	1
Tecno 77	Brendola	1
Universita degli Studi Dell Aquila	L Aquila	3
Universita di Torino	Torino	7
Università degli Studi di Ancona	Ancona	4

CUSTOMER	TOWN	Number of ASICs
Universita degli Studi di Firenze	Firenze	3
Universita della Calabria	Arcavacata di Rende	3
Universita di Cagliari	Cagliari	19
Universita di Catania	Catania	38
University of Bologna	Bologna	31
University of Brescia	Brescia	12
University of Genova	Genova	15
University of Milano-Bicocca	Milano	11
University of Modena and Regio Emilia	Modena	4
University of Naples	Napoli	7
University of Padova	Padova	30
University of Parma	Parma	13
University of Pavia	Pavia	20
University of Perugia	Perugia	7
University of Pisa	Pisa	31
University of Rome La Sapienza	Roma	2
University of Rome Tor Vergata	Roma	10
University of Salento	Lecce	6
University of Siena	Siena	2
XGLab	Milano	8
Japan		
MAPLUS	Kitsuki-City	1
Marubeni Solutions	Osaka	11
Hokkaido University	Sapporo	23
Kobe University	Kobe	9
NTT Corporation	Atsugi-Shi	1
Rigaku Corporation	Tokyo	7
Tokyo Institute of Technology	Tokyo	1
Yamatake	Kanagawa	1
Korea		
3SoC Inc.	Seoul	1
Electronics & Telecommunications Research Inst.	Taejon	2
JOSUYA TECHNOLOGY	Taejon	1
KAIST	Daejeon	5
Korean Elektrotechnology Research Institute	Changwon	1
Macam Co., Ltd	Seoul	2
M.I.tech Corp.	Gyeonggi-do	1
Nurobiosys	Seoul	10
Radtek	Yusung-Ku, Daejeon	1
Samsung Advanced Institute of Technology	Yongin-si Gyeonggi-do	5
Samsung Electro-Mechanics	Suwon	1
Seoul National University	Seoul	10
Seloco	Seoul	54
SoC8611	Gyeonggi-do	3
SML	Seoul	7
Lebanon		
American university of Beirut	Beirut	1
Lithuana		
Center for Physical Sciences and Technology	Vilnius	1
Kaunas University of Technology	Kaunas	1
Vilnius University	Vilnius	1

CUSTOMER	TOWN	Number of ASICs
Malaysia		
MIMOS	Kuala Lumpur	1
SunSem Sdn. Bhd.	Kuala Lumpur	1
University of Technology	Skudai	1
Malta		
University Of Malta	Msida	16
Mexico		
INAOE	Puebla	32
Universidad Autonoma de Baja California	Tijuana	1
Universidad Autonoma de Puebla	Puebla	1
Netherlands		
Aemics	Hengolo	8
ASTRON	Dwingeloo	1
Catena Microelectronics BV	Delft	1
Cavendish Kinetics	s Hertogenbosch	1
Delft University of Technology	Delft	195
ESA - ESTEC	AG Noordwijk ZH	6
GreenPeak Technology	Utrecht	12
Hogeschool Heerlen	Heerlen	1
IMEC-NL	Eindhoven	55
Intrinsic-ID	Eindhoven	1
Lucent Technologies Nederland BV	Huizen	1
Mesa Research Institute	Twente	5
NFRA	Dwingeloo	1
Nikhef	Amsterdam	5
Smart Telecom Solutions		1
Sonion	Amsterdam	3
SRON	Utrecht	14
Technische Universiteit Eindhoven	Eindhoven	51
TNO - Delft	Delft	1
TNO - FEL	The Hague	18
TNO Industrie	Eindhoven	1
University of Amsterdam	Amsterdam	1
University of Twente	Enschede	5
Xensor Integration	Delfgauw	3
New Zealand		
Industrial Research Ltd	Lower Hutt	4
Massey University	Albany	1
Norway		
AME As	Horten	1
IDE AS	Oslo	2
Interon	Asker	19
Nordic VLSI	Trondheim	38
Norwegian Institute of Technology	Trondheim	22
Novelda	Oslo	1
Nygon	Asker	2
SINTEF	Trondheim	19
University of Bergen	Bergen	6
University of Oslo	Oslo	93
Vestfold University College	Tonsberg	2

CUSTOMER	TOWN	Number of ASICs
Poland		
AGH University of Science and Technology	Krakow	97
Institute of Electron Technology	Warsaw	52
Military University of Technology	Warsaw	3
Technical University of Gdansk	Gdansk	12
Technical University of Lodz	Lodz	10
University of Mining and Metallurgy	Krakow	24
University of Technology & Agriculture	Bydgoszcz	1
University of Technology - Poznan	Poznan	2
Warsaw University of Technology	Warsaw	27
Portugal		
Acacia Semiconductor	Lisboa	6
Chipidea	Oeiras	22
INESC	Lisboa	44
INETI	Lisboa	1
Instituto de Telecomunicacoes	Lisboa	35
Instituto Superior Tecnico	Lisboa	6
Universidade de Aveiro	Aveiro	19
University of Minho	Guimaraes	10
University of Porto	Porto	18
ISEL-IPL	LIsboa	1
University of Tras-os-Montes e Alto	Vila Real	3
Universidade Nova de Lisboa - Uninova	Caparica	13
Puerto Rico		
University of Puerto Rico	Mayaguez	1
Romania		
Gheorghe Asachi Technical University of Iasi	Iasi	1
National Inst. for Physics and Nuclear Engineering	Bucharest	2
Polytechnic inst. Bucharest	Bucharest	2
Russia		
Budker Institute of Nuclear Physics	Novosibirsdk	3
IPMCE	Moscow	3
JSC "NTLAB"	Moscow	2
Moscow Institute of Electronic Technology	Moscow	5
Moscow Institute of Physics and Technology	Moscow	5
Moscow Engineering Physics Institute	Moscow	17
N.I. Lobachevsky State Univ	Nizhni Novgorod	8
SRIET-SMS CJSC	Voronezh	6
University St Petersburg	St Petersburg	5
Vladimir State university	Vladimir	1
Saudi Arabia		
King Abdullah Univ. of Science and Technology	Thuwal	7
King Saud University	Riyadh	1
Serbia and Montenegro		
University of Novi Sad	Novi Sad	3
University of Nis	Nis	2
Singapore		
Agilent	Singapore	2
DSO National Laboratories	Singapore	6
Nanyang Technology University	Singapore	6
Slovakia		
Inst. of Computer Systems	Bratislava	1
Slovak University of Technology	Bratislava	5
Slovenia		
Iskraemeco d.d.	Kranj	19
NOVOPAS	Maribor	1
University of Ljubljana	Ljubljana	8
University of Maribor	Maribor	1
South Africa		
CSIR Material Science and Manufacturing	Pretoria	1
Solid State Technology	Pretoria	8
University of Pretoria	Pretoria	38
South America		
CNM/Iberchip		74
Spain		
Acorde S.A.	Santander	30
Anafocus	Sevilla	2
Arquimea Ingenieria	Madrid	4
CIEMAT	Madrid	2
CNM	Bellaterra	91
Design of Systems on Silicon	Paterna	7
EUSS	Barcelona	1
Facultad de Informática UPV/EHU	San Sebastián	2
Oncovision	Valencia	2
Technical University of Madrid	Madrid	3
Univ. Las Palmas Gran Canaria	Las Palmas de Gran Canaria	22
Universidad Autonoma de Barcelona	Barcelona	23
Universidad Carlos III Madrid	Madrid	1
Universidad de Cantabria	Santander	36
Universidad de Extremadura	Badajoz	29
Universidad de Navarra	San Sebastian	36
Universidad de Santiago de Compostela	Santiago de Compostela	2
Universidad del Pais Vasco	Bilbao	3
Universidad Politecnica de Cartagena	Cartagena	4
Universidad Politecnica de Madrid	Madrid	3
Universidad Publica de Navarra	Pamplona	16
Universitat de Barcelona	Barcelona	54
Universitat Illes Balears	Palma Mallorca	3
Universitat Politecnica de Catalunya	Barcelona	52
Universitat Ramon Llull - La Salle	Barcelona	1
Universitat Rovira i Virgili	Tarragona	2
University of Malaga	Malaga	3
University of Seville	Sevilla	94
University of Valencia	Valencia	4
University of Valladolid	Valladolid	1
University of Vigo	Vigo	3
University of Zaragoza	Zaragoza	35
Sweden		
Aeroflex Gaisler	Goteborg	3

CUSTOMER	TOWN	Number of ASICs
Bofors Defence AB	Karskoga	2
Chalmers University	Goteborg	6
Chalmers University of Technology	Gothenburg	66
Defence Researh Establishment	Linkoping	5
Ericsson	Molndal	2
Ericsson Microelectronics	Kista	2
Halmstad University	Halmstad	2
Institutet for Rymdfysik	Kiruna	1
Imego AB	Goteborg	1
Lulea University of Technology	Lulea	13
Lund University	Lund	180
Malardalens University	Vasteras	2
Mid Sweden University	Sundsvall	12
Royal Institute of Technology	Kista	38
RUAG Aerospace Sweden	Goteborg	2
SiCon AB	Linkoping	4
Svenska Grindmatriser AB	Linkoping	3
University of Trollhattan	Trollhattan	3
University of Linköping	Linköping	157
Uppsala University	Uppsala	11
Switzerland		
Agilent Technologies	Plan-les-Ouates	2
Asulab SA	Marin	22
austriamicrosystems		2
Bernafon	Bern	1
Biel School of Engineering	Biel	9
CERN	Geneva	37
CSEM	Zurich	60
CT-Concept		9
Dectris	Baden	1
Ecole d'ingenieurs de Geneve	Geneve	1
Ecole d'ingenieurs et d'Archtectes	Fribourg	7
EPFL IMT ESPLAB	Neuchatel	32
EPFL Lausanne	Lausanne	324
ETH Zurich	Zurich	173
HMT Microelectronics Ltd	Biel/Bienne	4
Hochschule Rapperswill	Rapperswill	1
HTA Luzern	Horw	2
HTL Brugg-Windisch	Windisch	2
id Quantique	Carouge	19
Innovative Silicon S.A.	Lausanne	1
Institut MNT	Yverdon-les-Bains	1
Institute of Microelectronics, Uni. of Applied Sciences Northwest	Windisch	2
Landis + Gyr AG		1
Leica Geosystems	Heerbrugg	1
LEM	Plan-les-Ouates	3
MEAD Microelectronics S.A.	St-Sulpice	2
MICROSWISS	Rapperswil	2
Paul-Scherrer-Institute	Villigen	19
Photonfocus	Lachen	3
Senis	Zurich	1
Sensima technologies	Nyon	8
Sensirion	Staefa	2
Sentron AG	Lausanne	7

CUSTOMER	TOWN	Number of ASICs
siemens	Zug	2
Smart Silicon Systems SA	Lausanne	2
SUPSI-DIE	Manno	2
Suter IC-Design AG	Waldenburg	4
University of Applied Sciences HES-SO	Valais	3
University of Neuchatel	Neuchatel	22
University of Zurich	Zurich	65
Uster Technolgies	Uster	1
Xemics SA - CSEM	Neuchatel	33
Taiwan		
Feng Chia University	Taichung	1
National Cheng Kung University		1
National Sun Yat-Sen University	Kaohsiung	2
National Tsing Hua University	Hsinchu	4
Thailand		
Kasetsart University	Chatuchak, Bangkok	1
Microelectronic Technologies	Bangkok	2
NECTEC	Bangkok	36
Turkey		
ASELSAN	Ankara	1
Bahcesehir Universitesi	Istanbul	1
Bilkent University	Ankara	6
Bogazici University	Istanbul	22
Istanbul Technical University	Istanbul	27
Kardiosis	Ankara	1
KOC University	Istanbul	1
Kocaeli University	Izmit	1
Middle East Technical Univ.	Ankara	15
Sabanci University	Istanbul	23
Tubitak Bilten	Ankara	4
Yeditepe University	Istanbul	11
United Kingdom		
Aberdeen University	Aberdeen	1
Barnard Microsystems Limited	London	2
Bournemouth University	Poole	3
Bradford University	Bradford	7
Brunel university	Uxbridge	1
Cadence Design Systems Ltd	Bracknell	1
Cambridge Consultants Ltd.	Cambridge	3
Cardiff University	Cardiff	5
CML Microcircuits Ltd.	Maldon	20
Control Technique	Newtown	4
Data Design & Developmentsq	Stone	1
Dukosi	Edinburgh	2
Edinburgh University	Edinburgh	74
ELBIT Systems Ltd.		1
Epson Cambridge research lab	Cambridge	2
Heriot-Watt University	Edinburgh	2
Imperial College	London	68
Jennic Ltd	Sheffield	1
K.J. Analogue Consulting	Malmesbury	1
King's College London	London	1

CUSTOMER	TOWN	Number of ASICs
Lancaster University	Lancaster	7
Leicester University	Leicester	1
Middlesex University	London	6
Napier University	Edinburgh	4
National Physical Laboratory	Teddington	3
Nokia Research Center	Cambridge	2
Nortel	Harlow	1
Plextek Ltd	Essex	4
Polatis	Cambridge	1
Positek Limited	Glos	1
Roke Manor Research Ltd.	Southampton	11
Saul Research	Towcester	22
Sheffield Hallam University	Sheffield	1
Sofant Technologies	Edinburgh	1
STFC - RAL	Didcot	59
Swansea University	Swansea	1
Swindon Silicon Systems Ltd	Swindon	3
Tality	Livingston	1
The Queens University of Belfast	Belfast	5
The University of Hull	Hull	1
The University of Liverpool	Liverpool	14
UMIST	Manchester	58
University College London-UCL	London	2
University of Bath	Bath	29
University of Birmingham	Birmingham	6
University of Brighton	Brighton	1
University of Bristol	Bristol	7
University of Cambridge	Cambridge	33
University of Dundee	Dundee	1
University of East London	London	1
University of Glasgow	Glasgow	47
University of Hertfordshire	Hatfield	1
University of Kent	Canterbury	14
University of London	London	38
University of Newcastle upon Tyne	Newcastle upon Tyne	21
University of Nottingham	Nottingham	43
University Of Oxford	Oxford	28
University of Plymouth	Plymouth	2
University of Reading	Reading	1
University of Sheffield	Sheffield	7
University of Southampton	Southampton	39
University of Stirling	Stirling	1
University of Surrey	Guildford	6
University of the West of England	Bristol	2
University of Wales, Aberystwyth	Aberystwyth	5
University of Warwick	Coventry	5
University of Westminster	London	7
University of York	Heslington	2
Walmsley (microelectronics) Ltd	Edinburgh	1

USA

Analog	Phoenix	1
Arizona State University	Tempe	26
austriamicrosystems USA		1
Boston university	Boston	14
Brookhaven National Laboratory	Upton, NY	1
Carnegie Mellon University	Pittsburgh	1
Columbia University	Irvington, New York	19
Discera		1
Duke Universtity	Durham	1
Eutecus Inc	Berkeley	3
Exelys Ilc	Los Angeles	2
Flextronics	Sunnyvale	1
Forza Silicon Corporation	Pasadena	1
Fox Electronics	Fort Myers	5
Future Devices		1
General Electric	Niskayuna	3
Glacier Microelectronics	San Jose	1
Goddard Space Flight Center, NASA	Greenbelt	1
Intellectual Property, LLC	Cross Plains	1
Intrinsix	Fairport	1
Iwatsu	Irving	4
Johnson Space Center, NASA	Houston	1
Kaiam Corporation	Newark	2
Lawrence Berkeley National Laboratory	Berkeley	8
Linear Dimensions, Inc.	Chicago	1
Micrel Semiconductor	San Jose	11
Microchip Technology		1
MIT - Lincoln Lab	Cambridge	29
MOSIS	Marina del Rey, CA	63
Neofocal Systems	Portland	8
Nova R&D	Riverside	3
Oklahoma State University	Stillwater	1
Omega Optics	Austin	3
Parallax Inc.	Rocklin	2
Philips Medical Systems	Andover	1
PhotonIC Corporation	Culver City	1
Princeton University	Princeton, NJ	4
Purdue University	Lafayette	1
Rockwell Scientific	Thousand Oaks, CA	13
Signal Processing Group	Chandler	1
Stanford Linear Accelerator	Meno Park	11
Symphonix	San Jose	5
Tachyon Semiconductor	Naperville, IL	2
Tekwiss USA, Inc	Costa Mesa	2
Telemetric Medical Applications	Los Angeles	1
Triad Semiconductor		1
TU Dallas	Richardson	3
University of California	Santa Cruz	1
University of Chicago	Illinois	3
University of Colorado	Boulder	7
University of Delaware	Newark	3
University of Florida	Gainesville	9
University of Maryland - Joint Quantum Institute	Maryland	3
University of Pennsylvania	Philadelphia, Pa.	2
University of Texas at Austin	Austin	35
University of Washington	Seattle	2
USRA	Washington	1
Vectron International Inc.	Hudson NH	5
Western Cryptographic	Berkeley	1
Xerox	El Segundo	1
Yanntek	San Jose, CA	5

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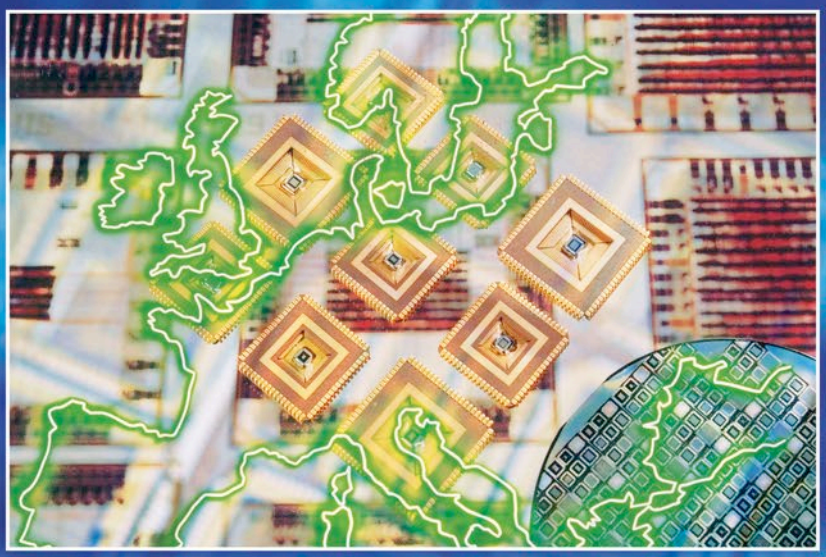

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