



TSMC 28nm HPC CMOS MICRO BLOCK



Features and Benefits

- TSMC 28 nm CMOS LOGIC High Performance Compact Mobile Computing ELK
 - ◆ 1.8V IO voltage
 - ◆ 0.9V core voltage
 - ◆ 1P8M_5X1Z1U UTRDL (28kÅ thick AP layer)
- Full PDK and library support
- On Silicon area as small as 1 mm²
 - ◆ Designed area 1.23mm²
- 2 runs per year
 - ◆ Timing tuned towards **key conferences**
- 100 parts per participation
- **9,600 EUR** for European academia, **11,805 EUR** for non European academia
- **Guaranteed Leadtimes** of 106 days (including verification and consolidation at imec)
- Larger designs can be accommodated by
 - ◆ Regular Mini@sic (2mm²)
 - ◆ Combining Micro block and Mini@sic
- Flexible extension to small volume manufacturing

Micro Blocks runs in 2019	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
TSMC 28nm CMOS Logic HPL/HPC, RF HPL/HPC —Micro-block (reserve 4 months in advance)			27							23		

Data in RED color are preliminary scheduled

All documentation & design kits available on:
For more information: mpc@imec.be

www.europactice-ic.com