GLOBALFOUNDRIES TECHNOLOGY PORTFOLIO

Updated version 2.0 from12 July 2019

130nm Technology Overview (MPW):

Technology	130nm BCDLite	130nm LP
Geometry	130nm	130nm
Drawn Geometry	130nm	130nm
Device Application	Bipolar-CMOS-DMOS Technology for Mobile and Consumer applications	Low Power for Analog and RF
Core Voltage (V)	1.5V/5V/30V	1.2V/1.5V
I/O Voltage (V)	1.5V/5V/30V	1.8V/2.5V/3.3V
Poly Layers	1	1
Metal Layers	4-8	2-8
Metal (1x)	1	1
Thick Metal (1.3x)	2-6	2-6
Top Metal (9kA)	1-2	1-2
Top Metal (30kA)	0-1	0-1
Recommended Metal Stack on MPW (Please contact us for other metal stack options)	1P7M TM30K, Dual Passivation	1P7M TM30K, Dual Passivation
Mandatory Metal Stack on mini@sic	**1P7M TM30K, Dual Passivation**	**NA**
Metal	Cu, Al(LB)	Cu, Al(LB)
Core transistor Vt	Regular Vt, Native Vt	Regular Vt, Low Vt
Special devices	High Gain LV MOSFET, EDMOS, LDMOS low RDson and RF MOSFET, Bipolar: LV and HV VNPN,VPNP BJTs Resistor: P+ Poly,N+ Poly, N+ Diff, Nwell Capacitor: NMOSCAP, Single-Mask MIM, APMOM Diodes: Zener, Schottky ESD: diodes, NMOS, PMOS, VPNP SRAM: HC, HD, LV Fuse: Efuse Inductors	RF MOSFETs Bipolar: LV and MV VNPN,VPNP BJTs Resistor: P+ Poly,N+ Poly, N+ Diff, Nwell Capacitor: NMOSCAP, Single-Mask MIM, APMOM 5V LDMOS ESD: diodes, NMOS, PMOS, VPNP SRAM: HC, HD, LV Fuse: Efuse Inductors
Digital Core Libraries*	ARM	ARM
I/O Libraries*	GLOBALFOUNDRIES	Aragio
SRAM*	ARM	ARM/Synopsys
Available Design Flows	Cadence and Synopsys, including Physical Verification tools from Mentor Graphics	Cadence and Synopsys, including Physical Verification tools from Mentor Graphics

*To get Aragio I/O libraries, send an email request to Jennifer Blakeman: jennifer@aragio.com.

*To download the digital core libraries and SRAM generators from Synopsys, use the Memory & Logic IP Selector to choose the component. Then download the component using your registered Synopsys id.

*The ARM libraries can be downloaded from ARM DesignStart.

55nm Technology Overview (MPW):

Technology	55nm-LPe	55nm LPe-RF	55nm LPx-NVM
Geometry	55nm	55nm	55nm
Drawn Geometry	65nm	65nm	65nm
Device Application	Low Power Enhanced	Low Power RF	Low Power with eFlash
Core Voltage (V)	1.2	1.2	1.2
I/O Voltage (V)	1.8V/2.5V/3.3V	1.8V/2.5V/3.3V	1.8V/2.5V/3.3V
Poly Layers	1	1	1
Metal Layers	6-8	6-8	6-8
Metal (1x)	4-7	4-7	4-7
Thick Metal (2x)	0-2	0-2	0-2
Thick Metal (4x)	0-2	0-2	0-2
Ultra Thick Metal (12x)	-	0-1	-
Recommended Metal Stack on MPW (Please contact us for other metal stack options)	6LM (5L1x_1T4x_LB) 7LM (6L1x_1T4x_LB)	6LM (5L1x_1T4x_LB) 7LM (6L1x_1T4x_LB)	6LM (5L1x_1T4x_LB) 7LM (6L1x_1T4x_LB)
Mandatory Metal Stack on mini@sic	**7LM (6L1x_1T4x_LB)**	**NA**	**NA**
Metal	Cu, lowK, Al(LB)	Cu, lowK, Al(LB)	Cu, lowK, Al(LB)
Vertical Natural Capacitor	Yes	Yes	Yes
HRes Resistor	Yes	Yes	Yes
Core transistor Vt	High-Vt, Std-Vt, Low-Vt	High-Vt, Std-Vt, Low-Vt	High-Vt, Std-Vt, Low-Vt
Special devices	NFET is isolated p-well, shallow trench isolation, vertical PNP bipolar transistor, native inductors, 5V LDMOS, Efuse, different kind of SRAMSs	FETs : LVt, RVt, HVt, DG. Resistors : P+ Poly, N+ diff, Nwell Resistors, Precision Poly Resistors. Decoupling/Varactors : Thin/thick ncaps, varactors, pcap. BEOL capacitors : vertical native capacitors, APMOM, MIM Capacitors. Inductors : Native inductors (2x/4x wires), 3µm thick Cu wire.	Capacitor: MOSCAP, APMOM, MIM Resistor: Poly and Diffusion Inductor**:** Native, Aluminum thick wire inductor High voltage FET: HV N/P, Native-N (5V full operation, BVDSS > 12V) Flash EDMOS**:**5V N/P, Body Iso-N Native FET: 1.2V N; 2.5V N
Digital Core Libraries*	Synopsys / ARM	Synopsys / ARM	ARM/NanGate
I/O Libraries*	Aragio	Aragio	Aragio
SRAM generator available*	Synopsys / ARM	Synopsys / ARM	ARM
Available Design Flows	Cadence and Synopsys, including Physical Verification tools from Mentor Graphics		

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*The ARM libraries can be downloaded from ARM DesignStart.

40nm Technology Overview (MPW):

Technology	40nm-LP	40nm-LP RF	40nm RF mmWave
Geometry	40nm	40nm	40nm
Drawn Geometry	45nm	45nm	45nm
Device Application	Low Power	Low Power RF	RF millimeter Wave
Core Voltage (V)	1.1	1.1	1.1
I/O Voltage (V)	1.5V/1.8V (Medium Gate Oxide) OR 1.8V/2.5V/3.3V (Thick Gate Oxide)	1.5V/1.8V (Medium Gate Oxide) OR 1.8V/2.5V/3.3V (Thick Gate Oxide)	1.5V/1.8V (Medium Gate Oxide) OR 1.8V/2.5V/3.3V (Thick Gate Oxide)
Poly Layers	1	1	1
Metal Layers	6-8	6-8	6-8
Metal (1x)	5-7	5-7	5-7
Thick Metal (2x)	0-1	0-1	0-1
Thick Metal (6x)	0-2	0-2	0-2
Ultra Thick Metal (18x)	0-1	0-1	0-1
Recommended Metal Stack on MPW (Please contact us for other metal stack options)	6LM (5L1x_1T6x_LB) 7LM (6L1x_1T6x_LB) 7LM (5L1x_2T6x_LB) 8LM (6L1x_1T6x_1T18x_LB)	6LM (5L1x_1T6x_LB) 7LM (6L1x_1T6x_LB) 7LM (5L1x_2T6x_LB) 8LM (6L1x_1T6x_1T18x_LB)	6LM (5L1x_1T6x_LB) 7LM (6L1x_1T6x_LB) 7LM (5L1x_2T6x_LB) 8LM (6L1x_1T6x_1T18x_LB)
Mandatory Metal Stack on mini@sic	**NA**	**NA**	**NA**
Metal	Cu, lowK, Al(LB)	Cu, lowK, Al(LB)	Cu, lowK, Al(LB)
Vertical Natural Capacitor	Yes	Yes	Yes
HRes Resistor	Yes	Yes	Yes
Core transistor Vt	High-Vt, Std-Vt, Low-Vt, Super-Low-Vt	High-Vt, Std-Vt, Low-Vt, Super-Low-Vt	High-Vt, Std-Vt, Low-Vt, Super-Low-Vt
Special devices	NFET is isolated p-well, shallow trench isolation, vertical PNP bipolar transistor, native inductors, 5V LDMOS, Efuse, different kind of SRAMSs	SG NFET, PFET; DG NFET, PFET; Noise; SG NFET; Silicided/Unsilicided P+ Poly Resistor; Precision Resistor Inductor (3mm Cu + LB Termination); MOS Var; (SGNCAP) VNCAP; APMOM; MIM	Core FET:Regular-Vt NFET/PFET, Low-Vt NFET/PFET MOS Cap: Thin/Thick-oxide NCAP , Thin/Thick-oxide PCAP APMOM, PPolyRes Inductor Transmission Line
Digital Core Libraries*	Synopsys / ARM	Synopsys / ARM	Synopsys / ARM
I/O Libraries*	Aragio	Aragio	Aragio
SRAM generator available*	Synopsys / ARM / GLOBALFOUNDRIES	Synopsys / ARM / GLOBALFOUNDRIES	Synopsys / ARM / GLOBALFOUNDRIES
Available Design Flows	Cadence and Synopsys, including Physical Verification tools from Mentor Graphics		

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*To download the digital core libraries and SRAM generators from Synopsys, use the Memory & Logic IP Selector to choose the component. Then download the component using your registered Synopsys id.

*The ARM libraries can be downloaded from ARM DesignStart.

28nm Technology Overview (MPW):

Technology	28nm-SLP	28nm-SLP RF
Geometry	28nm	28nm
Drawn Geometry	32nm	32nm
Device Application	Super Low Power	Super Low Power RF
Core Voltage (V)	1.0	1.0
I/O Voltage (V)	1.5V/1.8V	1.5V/1.8V
Poly Layers	1	1
Metal Layers	6-11	6-11
Metal (1x)	5-6	5-6
Thick Metal (2x)	0-3	0-3
Thick Metal (8x)	1-2	1-2
Ultra Thick Metal (30x)	-	0-1
Recommended Metal Stack on MPW (Please contact us for other metal stack options)	8LM (6U1x_2T8x_LB)	8LM (6U1x_2T8x_LB) 8LM (6U1x_1T8x_1T30x_LB)
Mandatory Metal Stack on mini@sic	**NA**	**NA**
Metal	Cu, Al(LB)	Cu, Al(LB)
Vertical Natural Capacitor	Yes	Yes
HRes Resistor	Yes	Yes
Core transistor Vt	High-Vt, Std-Vt, Low-Vt, Super-Low-Vt	High-Vt, Std-Vt, Low-Vt, Super-Low-Vt
Special devices	Inductors, vertical PNP bipolar transistor, efuse, varactors, different kind of SRAMSs	Core devices (SG): LVt, RVt, HVt; LDMOS 5.0V; Resistor, Capacitor, VNCAP, Inductor, APMOM
Digital Core Libraries*	ARM / NanGate	ARM / NanGate
I/O Libraries*	Aragio / ARM	Aragio / ARM
SRAM generator available*	ARM / Mobile Semi	ARM / Mobile Semi
Available Design Flows	Cadence and Synopsys, including Physical Verification tools from Mentor Graphics	

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*The ARM libraries can be downloaded from ARM DesignStart.

22nm Technology Overview (MPW):

Technology	22nm-FDX
Geometry	22nm
Drawn Geometry	22nm
Device Application	Ultra Low Power Ultra Low Leakage RF/mmWave eMRAM
Core Voltage (V)	0.4V-0.8V
I/O Voltage (V)	1.2V/1.5V/1.8V
Poly Layers	1
Metal Layers	7-10
Metal Mx (1x)	2
Metal Cx(1.1x)	3-6
Thick Metal Bx (2.2x)	0-2
Thick Metal Ix (9x)	0-2
Thick Metal Jx (11x)	0-2
Ultra Thick Metal Qx (30x)	0-2
Ultra Thick Metal Ox (34x)	0-1
Recommended Metal Stack on MPW (Please contact us for other metal stack options)	Option #3 (for general applications) Option #19 (for RF/mmWave) Option #20 (for eMRAM and/or RF/mmWave)
Mandatory Metal Stack on mini@sic	**Option #19** **10M_2Mx_5Cx_1Jx_2Qx_LB**
Metal	Cu, Al(LB)
Core transistor Vt	eLVt, SLVt, LVt, RVt, HVt, UHVt
Special devices	SRAM: HD, LV, ULV Resistor: N+ Poly, N+ Diff, Nwell Varactor: NCAP, EGNCAP Bipolar: VPNP Fuse: RX Efuse ESD: STI bounded Diodes (N+/PW & P+/NW) RF/mmWave: MOSFET, Resistor, Inductor, Varactor, APMOM, Tx Line
Digital Core Libraries*	INVECAS / Synopsys
I/O Libraries*	INVECAS
SRAM generator available*	INVECAS
Available Design Flows	Cadence and Synopsys, including Physical Verification tools from Mentor Graphics

*For INVECAS foundational IPs contact: virtual-asic@iis.fraunhofer.de