Simple SoC (SSoC)

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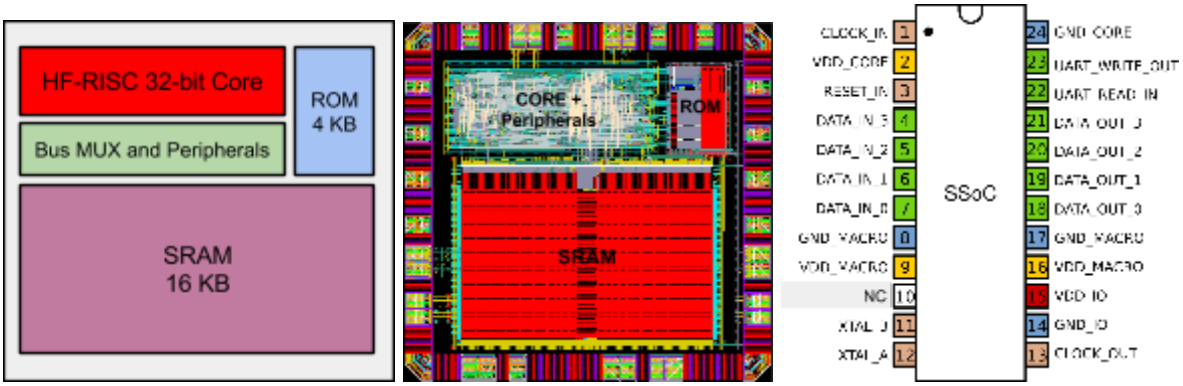
Type of Circuit Design: **(x) Digital**; ( ) mixed signal; ( ) analog; ( ) RF
Date of the circuit tape-out of the run: **18 March 2015**
Date of the report and/or of later update: **10 April 2015**
Date of receiving the chips at your institution: **16 August 2015**

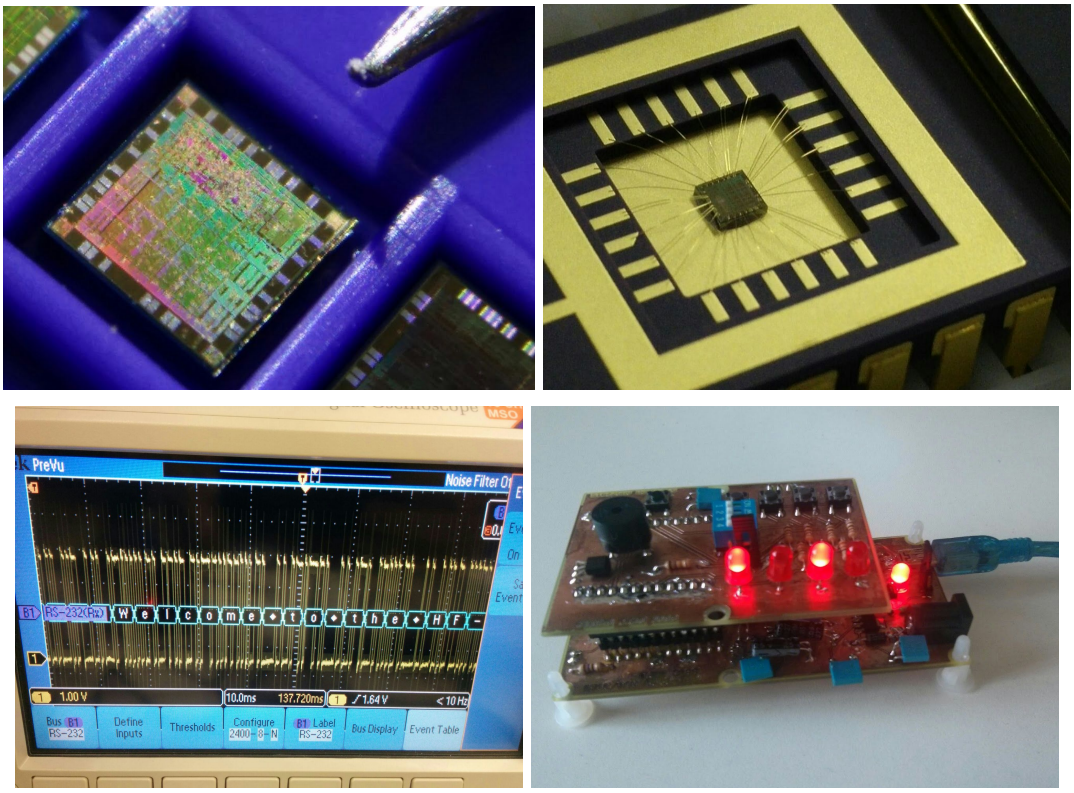
The goal of the project was to build a microcontroller, an instance of a configurable SoC proposed by Sergio Johann Filho during his MSc dissertation and PhD Thesis. The SoC design objective is reducing the overall chip power consumption to enable the use of the SoC in low-end IoT applications. To verify this requirement, the chip backend design eases the task of separately measuring power of each of the soC blocks. Another requirement was to validate the skill of the team to build a fully working IC, covering all of the chip development steps. The SoC includes a 3-stage pipe 32-bit HF-RISC processor Core, 16 KB SRAM, 4 KB ROM (for the bootloader and test software). HF-RISC implements a subset of the MIPS-I ISA. It contains peripherals such as counters, compare registers, external I/Os, a UART and an interrupt controller. It takes 5530 gates. The Figure below shows the SSoC blocks diagram (left), the final IC layout (center) and the package pinout (right). There are 24 pins for power rails, clock, reset, and I/Os.



The first tests were conducted to certify that the clock, reset and UART were working properly using a breadboard. After that, we developed a simple (Arduino-like) platform to validate all of the SSoC blocks through a simple C library[1] and demos. All planned features are working well except for minor problems caused by the first reset and the system power-up sequence, due to

[1] We have a modified gcc compiler 4.9.0 to work with SSoC.

some problems originating from our board design. The Figure below shows the SSoCs die compared to the tip of a pin (upper left) and the package open cavity with its pin to pad connections (upper right). The second row shows the first feedback received from the SSoC using a logic analyzer (lower left - “Welcome to the HF-RISC Bootloader”) and the modular platform working attached to an USB cable (right). All tested chips worked as expected, and we were able to run real benchmarks (such as Coremark and others), SRAM tests and applications, which stress the peripherals and interrupt controller.



The main faced design challenges were a lack of information about the technology. We missed required documents and files until a few days before the tapeout date. Thus, we started using a wrong library, which implied to redo the whole backend design. Another related issue was that the tapeout deadline changed to an earlier date. We acknowledge the great help provided to us by Prof. Jacobus Swart to solve these and other issues, ensuring the success of this project. Two publications about the configurable SoC mention this project. They have been approved for publication in the journal Microprocessors and Microsystems (Elsevier) and the LASCAS conference. A more thorough measurement environment will enable other publications.

Bibliography:

1. JOHANN Fo., S., MOREIRA, M. T., HECK, L. S., CALAZANS, N. L. V., HESSEL, F. P. A Processor for IoT Applications: An Assessment of Design Space and Trade-offs. Microprocessors and Microsystems. Approved for publication in Jan 2016, final version in preparation.
2. JOHANN Fo., S., MOREIRA, M. T., CALAZANS, N. L. V., HESSEL, F. P. The HF-RISC Processor: Performance Assessment. In: VII IEEE Latin American Symposium on Circuits and Systems, Florianópolis (LASCAS), 2016. Accepted for publication.