IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuit: **IoT Edge Device with Power Domain Separation based on the HF-RISC Processor – C-SoC**

Adviser Professor(s): **Ney Laert Vilar Calazans**

Students involved (names and aimed degrees):

- **Ricardo Guazzelli (MSc student at the PPGCC, PUCRS, presently taking a PhD Course at the TIMA Laboratory in the Grenoble-Alpes University, France)**
- **Felipe Bortolon (CE student in the School of Technology, PUCRS, then MSc student at the PPGC in UFRGS, now hired by Silvaco. Inc.)**
- **Leandro heck (PhD at the PPGCC, PUCRS)**
- **Matheus Moreira (MSc and PhD student at the PPGCC, PUCRS, now Technical Director at the ChronosTech startup in San Diego, CA, USA)**

Institution (University/Faculty): **PUCRS – Porto Alegre, RS, Brazil**

Type of Circuit Design: (**X**) Digital; ( ) mixed signal; ( ) analog; ( ) RF

Date of the circuit tape-out of the run: **March 23rd, 2016**
Date of receiving the chips at your institution: **August 29th, 2016**
Date of the report and/or of later update: **August 21st, 2018**

Short description of the circuit: (function, proposed innovation, number of transistors, passive components, screen shot of the chip layout, etc.)

HF-RISC [1] is a 32-bit processor proposed by Sergio Johann Filho during his graduate studies (MSc and PhD). It has been validated in FPGAs and it is currently used in several academic embedded applications, and as a resource in PUCRS undergraduate and graduate courses. The C-SoC design objective was to employ this processor as the core of a prototype IoT edge device, showing its capability to achieve the performance [2] of a 32-bit programmable processor associated with a potential for low power consumption [3].

This is the second prototype of a series. The first one, S-SoC, was a fully digital implementation of HF-RISC with associated ROM, RAM and a minimum set of peripherals for communication with the external world. This second implementation of HF-RISC the Crypto-SoC (C-SoC), is a 32-bit architecture with a 3-stage pipeline compatible with the MIPS-I ISA, 16 KB of SRAM and 4 KB of ROM containing a bootloader software (SW). C-SoC can operate at 200 MHz but for simplicity the design target was set at 50 MHz. In addition to the S-SoC hardware blocks, C-SoC contains an XTEA cryptographic core. Also, the chip comprises test mode support through a scan chain and 8 extra pins for I/O. Also, previous design issues detected in the S-SoC prototype were fixed in C-SoC. The block power domains are now fully split in three regions (processor core, XTEA and memories) to enable easy power consumption measurements. The reset circuit was improved to become more robust, a problem detected in S-SoC.

Figure 1 below details the final layout of C-SoC, highlighting the main SoC blocks.

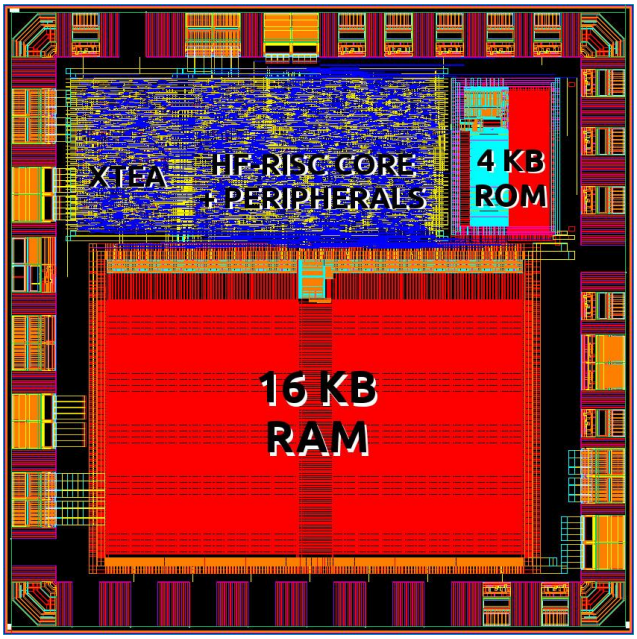

Figure 1: The C-SoC final layout.

To allow for a low cost IoT edge device, C-SoC is a chip with low pin count. While S-SoC had 24 pins, C-SoC is originally available in a 40-pin package. An evaluation printed circuit board developed to validate S-SoC was enhanced to accept C-SoC as well as S-SoC DIP packages. As S-SoC, C-SoC can be programmed and debugged through a USB connection and its SW is built using a specific versions of the GNU gcc compiler and libraries.

Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc.

The circuit was tested and is fully operational as far as all conducted tests are concerned. The IC was installed in a specific printed circuit board (PCB) and used to control peripherals inside and outside of the IC. The board connects through a USB cable to a Linux laptop where lies the gcc-based specific programming environment. The environment was employed to develop SW applications, cross-compile these applications for the C-SoC processor, download the executable code to the C-SoC and control the application execution results. Dozens of programs (including standard benchmarks) were run on the C-SoC successfully. Another test fixture was constructed where the C-SoC and another specific PCB are interfaced to an FPGA development board. The Figure 2 below displays the mentioned C-SoC test environments. The IC comprises a scan-chain that allows advanced SW debugging features such as step-by-step instruction execution, instruction backtrack and block execution.

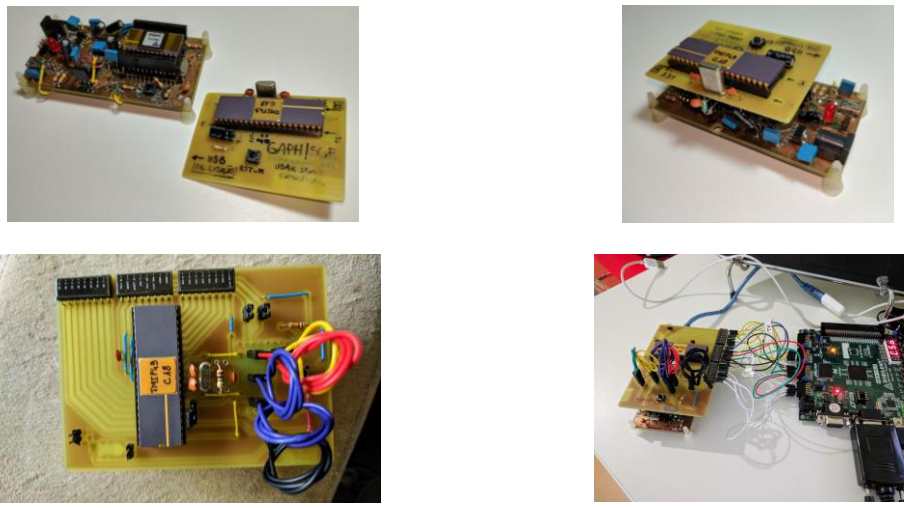

Figure 2: The test fixtures for the C-SoC IC.

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit:

In terms of IC design, the use of the RAM/ROM generators made available by ARM (from the Artisan libraries) was quite challenging. This is due to the outdated nature of this SW that required us to set up a Solaris environment to achieve the generation of the RAM and ROM. Particularly, the way to specify the ROM contents in a way to have it influencing the design of the bootloader ROM was a tough step. The sign-off of the chip design was challenging, even after we considered the design ready for fabrication, since not all layer views are available for the ARM libraries. Interaction with the IMEC team to solve several issues was instrumental here.

Resulting publications (submitted, accepted or published):

[1] JOHANN, F. S.; MOREIRA, M. T.; HECK, L. S.; CALAZANS, N. L. V. and HESSEL, F. P. A Processor for IoT Applications: An Assessment of Design Space and Trade-offs. Microprocessors and Microsystems, vol. 42, pp. 156-164, May 2016.

[2] JOHANN, F. S.; MOREIRA, M. T.; CALAZANS, N. L. V. and HESSEL, F. P. The HF-RISC Processor: Performance Assessment. In: VII IEEE Latin American Symposium on Circuits and Systems (LASCAS), Florianópolis, 2016, pp 95-98.

[3] BORTOLON, F.; GIBILUKA, M.; JOHANN FILHO, S.; BAMPI, S.; CALAZANS, N. L. V.; HESSEL, F. P.; MOREIRA, M. T. Design and Analysis of the HF-RISC Processor Targeting Voltage Scaling Applications. In: Symposium on Integrated Circuits and Systems Design (SBCCI), 2016.

Degrees earned by students:

Matheus Trevisan Moreira	**PhD (PUCRS)**
Leandro Sehnem Heck	**MSc (PUCRS)**
Ricardo Guazzelli	**MSc (PUCRS)**
Felipe Bortolon	**MSc (UFRGS)**