IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuit: Microcontroller and Voltage References for Low Power Applications

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Students involved:

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Institution: Federal University of Pampa - UNIPAMPA

Type of Circuit Design: ( ) Digital; (x) mixed signal; ( ) analog; ( ) RF

Date of the circuit tape-out of the run: March, 2016.
Date of receiving the chips at your institution: September 02, 2016.
Date of the report and/or of later update: August 22, 2017.

Short description of the circuit:

This prototyped chip is composed of a set of circuits designed by master students from the Computer Architecture and Microelectronic Group (GAMA) at UNIPAMPA and also from the Microelectronics Group at UFRGS (collaborative research project). It includes the following main blocks: a customized microcontroller for low-power applications and two voltage references. The microphotography of the prototyped chip can be seen in Fig. 1.

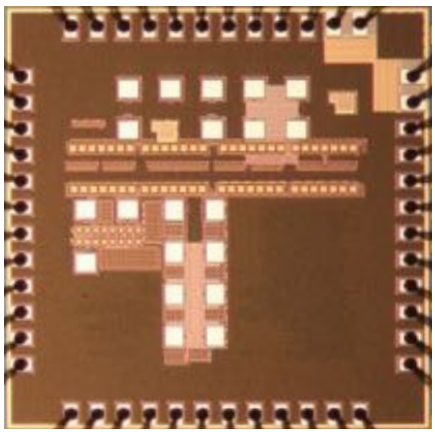


Fig. 1 – Photography of the prototyped chip.

Main results

a) PAMPIUM Microcontroller

The PAMPIUM IC processor was fabricated in order to validate in silicon the design methodology using ASIPAMPIUM, which is a tool developed by our group for the semi-automatic generation o ASIPs. The application is a motion detection system using MPU6050 sensors, with the possibility of reading 6 sensors and transmitting the information using the RS232 protocol. A PAMPIUM customized processor was generated, with three I2C communication modules and one RS232 module. The processor architecture is of the 16-bit integer type, with a 24-bit instruction word, and can be map up to 16,384 program lines. There are 64 registers implemented, in which nine are of specific use, such as literal input, program memory pointer and configuration, and the remaining are general purpose registers.

For the development of the processor it was decided to use external memory modules with SPI communication for data memory and program memory. So, there are only two small cache memories inside the chip. The program cache memory consists of 8 positions, each one containing 24 bits. Each position has a register that stores its address. The use of 8 storage positions allows small loops to be performed without the need for additional external readings. The data cache memory consists of sixteen 16-bit positions. These positions were divided into four banks. Each bank has a register that stores the most significant part of the address. Thus, the reading and writing in the external memory is always made in blocks of 4 consecutive accesses. This type of access maximizes performance by exploiting data locality. The implementation of data cache memories and programs with SPI access allows such interfaces to use only 8 pins. Adding the standard pins of "clk", "rst", "Vdd" and "gnd" results in a total of 12 pins. In this way it is possible to include in the circuit up to 4 communication modules with the remaining 8 pins available, since there were 20 pins reserved for this module in the prototyped chip. Figure 2 shows the final result of the implementation.

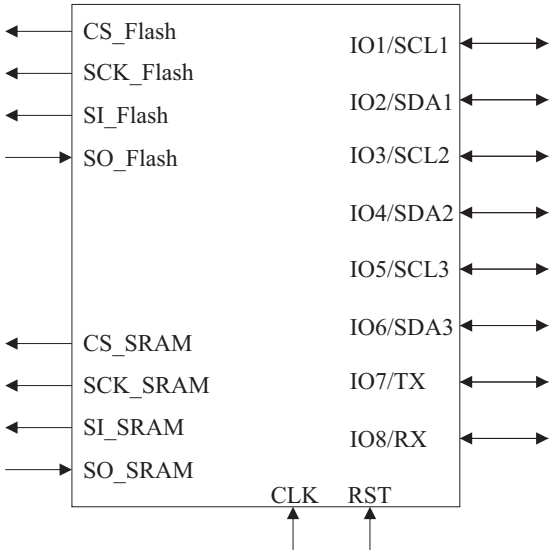


Figure 2 - The PAMPIUM IC processor I/O pins.

The resulting layout obtained after the physical synthesis in TSMC technology 0.18µm is shown in the figure 3.

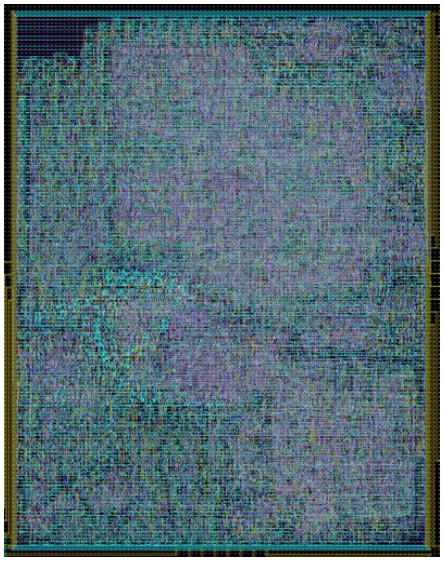


Figure 3 - PAMPIUM IC layout

For the physical synthesis, three different clock trees were considered: flash memory clock, SRAM memory clock and main PAMPIUM IC clock. The layout has an area of 500µm x 627µm = 0.314mm^2, which meets the imposed area criterion defined in the floorplanning.

The maximum operating frequency achieved 79MHz and the chip consumed 28mW with a 1.8V supply voltage. Figure 4 shows the PAMPIUM IC test setup.

Figure 4 - PAMPIUM IC board test setup.

Using the Agilent 16803A Logic Analyzer and a multimeter, supply current values were sampled as a function of the clock frequency, always verifying the correct response of the control signals of the developed processor. Figure 5 shows the measured power consumption in relation to the operating frequency of PAMPIUM IC. A linear trend of power consumption can be observed with the increasing of the operating frequency.

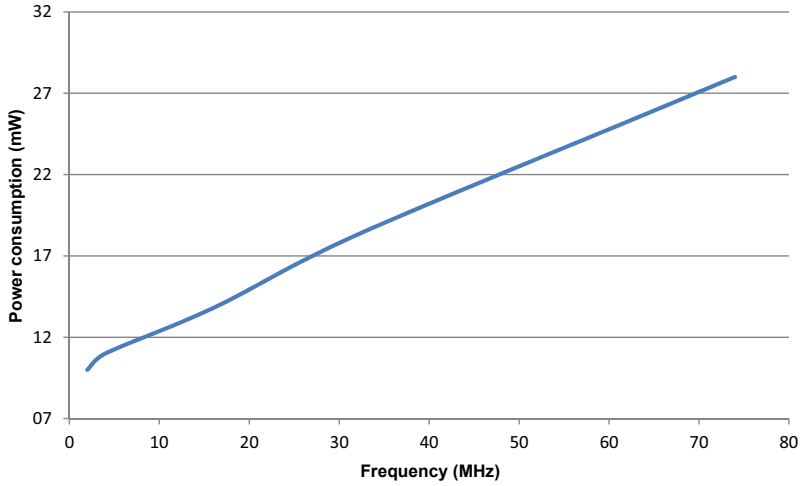


Figure 5 – Measured power consumption versus operating frequency of PAMPIUM IC.

b) Voltage References

This work proposes novel temperature-compensated subthreshold voltage references for ultra-low power and ultra-low voltage applications. The core of the proposed circuits is the self-cascode MOSFET (SCM) since it can operate at very low current levels. To reduce the power consumption, self-biasing and zero-VT leakage biasing schemes are exploited. This resulted in two main structures: a self-biased SCM (SBSCM) and a self-biased NMOS load (SBNMOS). The reference voltage generation is achieved by using the SCM with different threshold voltages. Even though these solutions present good performance and low power consumption, the usage of different V_T transistors makes the circuits too sensitive to process variations. To obtain a temperature-compensated voltage reference using the same type of device, we use the reverse short-channel and narrow-width effects of the MOS transistor, where V_T is larger for short/narrow-channel devices. Measurement results for 24 samples show that the proposed self-biased circuits can operate at 0.45-0.6 V minimum supply voltages, consuming merely 54.8 and 184 pW at room temperature. Without trimming, from 0 to 120^{o}C the circuits presented a temperature coefficient of 104 and 495 ppm/^{o}C, while after trimming these values were reduced to 72.4 and 11.6 ppm/^{o}C, respectively.

The measurement results were performed using a Keysight-4156 Semiconductor Parameter Analyzer for DC sweep and a Tenney Jr. thermal chamber for temperature control. The standard measurement setup can be seen in Fig. 6. The parameter analyzer is configured with a large integration time in order to get as many data as possible for each DC sweep. Triaxial and coaxial cables are used to connect the parameter analyzer to the test fixture, and coaxial cable from the fixture into the thermal chamber. A DC sweep from 0-VDD_{MAX} was performed for each temperature point.

Fig. 6 - Standard measurement setup for voltage references.

The chip photo and the layout of the proposed circuits are shown in Fig. 7. The total occupied areas are 0.0020mm² and 0.0017mm² for the SBSCM and SBNMOS, respectively. A total of 24 chips from the same batch were packaged in ceramic and measured.

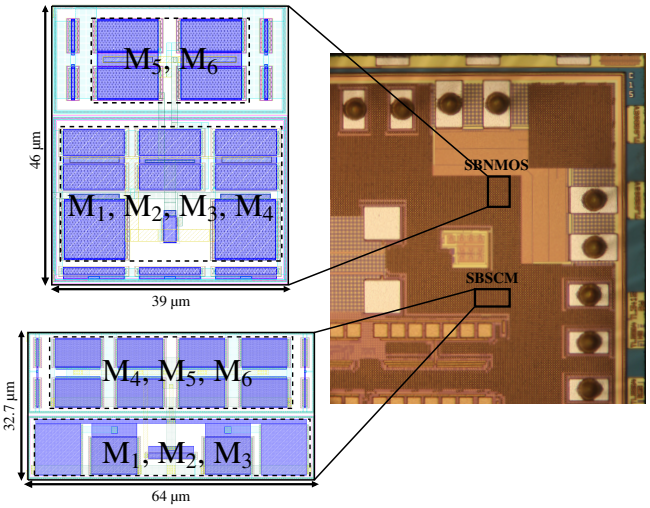


Fig. 7 - Chip photo of the proposed voltage references and their layouts.

Fig. 8(a) shows the measured results of the supply voltage dependence for average samples of both proposed circuits at 20ºC. The SBSCM starts to operate at 0.45 V supply, while the SBNMOS at 0.6 V supply. The average measured line sensitivity (LS) from VDDMIN to 3.3 V was 0.15%/V (SBSCM - Fig. 8(b)) and 0.11 %/V (SBNMOS - Fig. 8(c)).

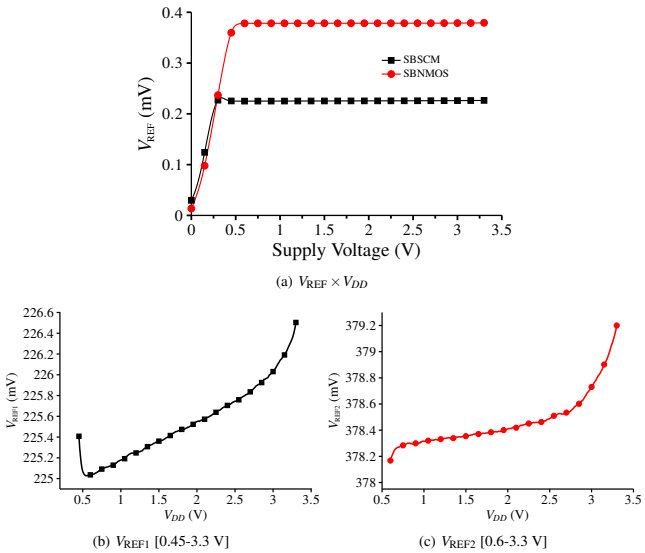
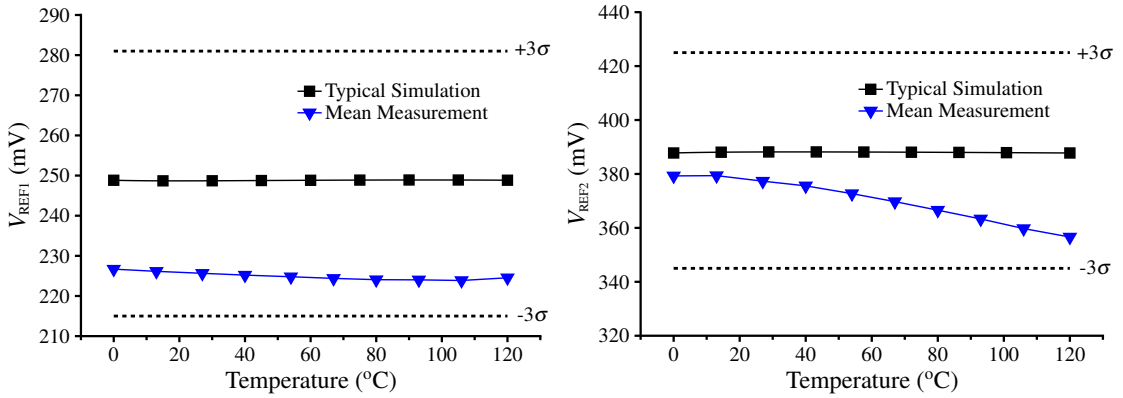


Fig. 8 - Measured supply voltage dependence of the proposed voltage references.

The simulated and measured temperature dependence from 0ºC to 120ºC for both circuits is shown in Fig. 9. A temperature coefficient (TC) between 68 ppm/ºC and 150 ppm/ºC, with a mean of 104 ppm/ºC was measured from the 24 samples in the case of the SBSCM, as shown in Fig. 9(a), while for the SBNMOS the mean measured TC was 495 ppm/ºC (Fig. 9(b)).



(a) SBSCM (b) SBNMOS

Figure 4.6: Measured temperature behavior for an average sample of the proposed voltage references.

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit.

There were no significant difficulties during the design implementation, submission or import process stages. The support from IMEC Brazil was very efficient when some questions have arisen.

Resulting publications (submitted, accepted or published) and degrees earned by students.

The chip prototyping supported valuable results for two master degrees (Alian Engroff and Arthur Campos).

A paper describing ASIPAMPIUM and including the measurement results of the PAMPIUM IC implementation is being submitted to Microprocessors and Microsystems (Elsevier).

The voltage reference circuits produced the following publications:

OLIVEIRA, A. C.; CORDOVA, DAVID ; BAMPI, SERGIO ; KLIMACH, HAMILTON . A 0.45 V, 93 pW Temperature-Compensated CMOS Voltage Reference. In: 8th IEEE Latin American Symposium on Circuits and Systems, 2017, Bariloche. Proceedings of the 8th IEEE Latin American Symposium on Circuits and Systems, 2017.

OLIVEIRA, A. C.; CORDOVA, DAVID ; BAMPI, SERGIO ; KLIMACH, HAMILTON . An Ultra-Low Power High-Order Temperature- Compensated CMOS Voltage Reference. In: 15th IEEE International New Circuits and Systems Conference (NEWCAS), 2017, Strasburg. Proceedings of the 15th IEEE International New Circuits and Systems Conference, 2017.

CORDOVA, DAVID ; OLIVEIRA, A. C. ; TOLEDO, PEDRO ; KLIMACH, HAMILTON ; BAMPI, SERGIO ; FABRIS, ERIC . A Sub-1 V, Nanopower, ZTC Based Zero-VT Temperature-Compensated Current Reference. In: IEEE International Symposium on Circuits and Systems (ISCAS), 2017, Baltimore. Proceedings of the IEEE International Symposium on Circuits and Systems, 2017.