

1-GHz CMOS Differential Ring Oscillator

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Chip Identification

- Ref.nr. : 77839/103020/01
- Serv.Center: IMEC
- Technology: TSMC 180 nm CMOS Logic or MS/RF(mini@sic)
- Run nr.: 5839
- Subm.Date: 2017/9
- Topcell/Project name: LRF_UFSC_2017

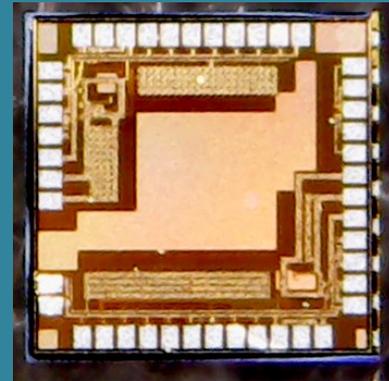
Description

The integrated circuit is a 1-GHz ring oscillator designed in a differential topology, fabricated in the TSMC 180 nm MS/RF CMOS technology. In addition to the main oscillator, accessory circuits were included for easier testing. Notably, a narrowband phase locked loop was included to stabilize the carrier frequency, as well as a 50- Ω buffer for interfacing with 50- Ω equipment. The purpose of the designed oscillator is to provide a stable signal to a miniaturized wireless power transfer system envisaged to supply energy to implanted circuits.

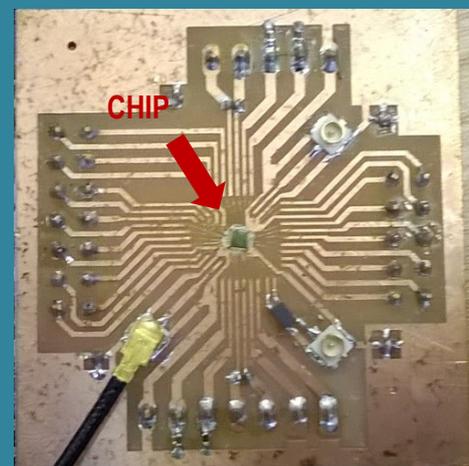
The chip was assembled on the

surface of a printed circuit board using a FR4 substrate, Ohm). The connections were done with gold wires, using a wire-bonding machine.

Chip Photography



Photography of the PCB



Experimental setup and Results

Two DC power supplies were used to provide energy to the circuit. The oscillator was powered with 1,5 V and the buffer and additional circuits used 1,8 V. The test board was designed as a shield to an Altera DE-2 FPGA development board. A digital circuit was synthesized on FPGA to provide the control signals necessary to configure the oscillator. A

spectrum analyzer was used to verify the oscillator output signal.

The circuit oscillated at 1.14 GHz and the measure power was -8.5 dBm. This output is very close to the results predicted from post layout simulations..

A new testbench is being developed to measure the oscillator phase noise and explore it in the target application.

