IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuit: A comparison of ISM radio-band oscillators based on: ring oscillator, passive and active inductor LC-VCOs.

Title of the Mini@sic project: Active Inductor LC-VCO

Adviser Professors: Dr. Fabiano Fruett.

Students involved (names and aimed degrees)

- Miguel Gómez (Msc student).
- José Ramirez (PhD student).

University Name: University of Campinas (UNICAMP).
Faculty Name: School of Electrical and Computer Engineering (FEEC).

Type of Circuit Design: ( ) Digital; ( ) mixed signal; (**X**) analog; (**X**) RF.

Date of the circuit tape-out of the run: 2017/04/25
Date of receiving the chips at your institution: 2017/09/12
Date of the report and/or of later up-date: 2018/08/17

Short Description of the circuit:

The main goal of this work is to compare the performance of three different oscillator typologies: ring oscillator, passive and active inductor LC-VCOs for ISM radio-band oscillator applications.

The die is composed of the following blocks:

1. Voltage and current references: These blocks are required to bias the other blocks within the chip. The required voltage reference of 0.9V is composed of a CMOS Operational Amplifier, a resistive voltage divider, an output buffer and bipolar transistors to generate the ΔV_{BE} voltage. The 10µA current reference uses a temperature compensated topology to bias the current source for the passive LC-VCO.
2. Passive Inductor LC-VCO: This circuit implements an RF wide tuning band LC-VCO for the ISM radio band. It uses a passive inductor available in the TSMC technology. A binary weighted capacitor array is used as tunable element to achieve the desired frequency. The capacitor array is implemented using RF metal capacitors. The core of the oscillator uses a cross-coupled complementary differential pair with RF transistors.
3. Active Inductor LC-VCO: This circuit also implements an RF LC-VCO for the ISM radio band, but instead of a passive inductor implements an active inductor using a differential Gm-C topology. As fine tuning element uses a voltage controlled varactor available in the process.
4. Ring Oscillator: This oscillator uses a differential CML ring oscillator as topology and was designed to operate inside the ISM radio band.

Figure 1 shows the layout and a photograph of the fabricated die with the 180nm CMOS RF-Mixed signal process. The die holds the five blocks previously described: Voltage Reference, Current Reference, Passive inductor LC-VCO, Active inductor LC-VCO and CML Ring Oscillator. The die has an area of 1660µm x 1660µm.

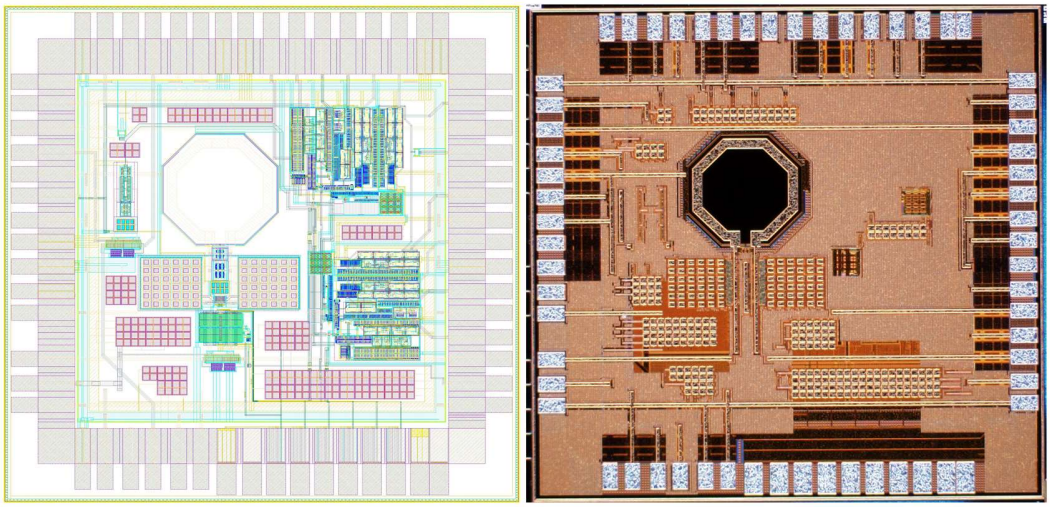

Figure 1 – Designed layout and die photograph for the LC-VCO project.

Figure 2 shows the simulation results for the Active and Passive inductor LC-VCOs. Fig. 2(a) show the tuning sensitivity and output frequency regarding to the Active LC-VCO, the surface shows the dependence of the output frequency to the continuous control signals: "coarse tuning" and "fine tuning". In this case, as both control signals are continuous voltages it is possible to obtain a surface as a result. Fig. 2(b) shows the output frequency and tuning sensitivity for the Passive LC-VCO.

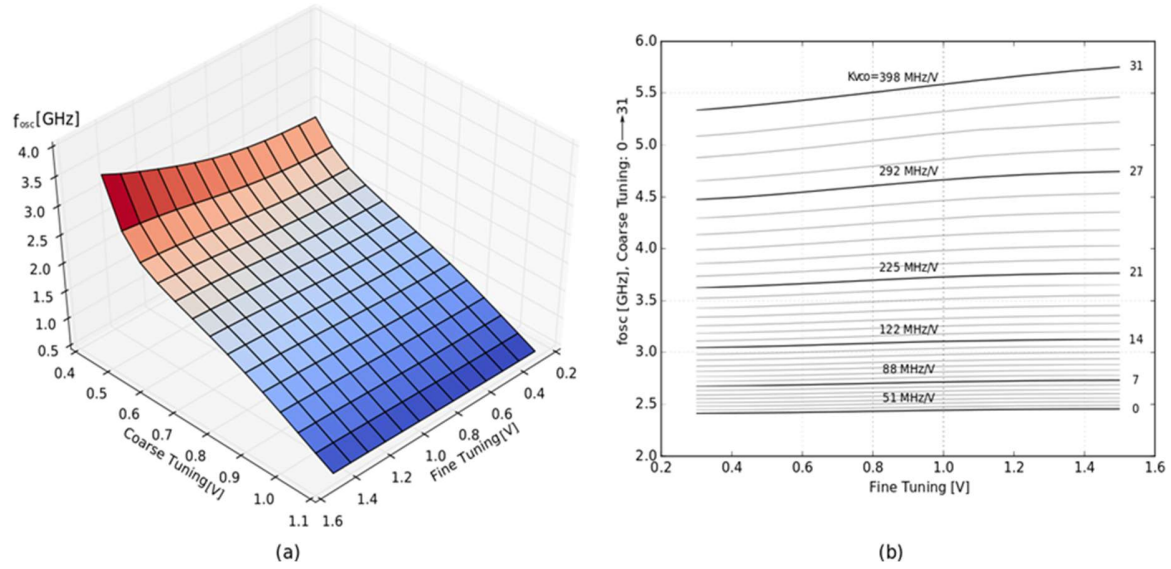

Figure 2 – Output frequency and tuning sensitivity for the active and passive LC-VCO.

This circuit sweeps a discrete signal for the coarse tuning and a continuous voltage signal for the fine tuning. In this case, the graph is better represented with several continuous curves of the fine control signal, each belonging to a particular value of the discrete signal varying between 0 and 31, as indicated in Figure 2b. The measurements on silicon for all the oscillators is a work in progress and for that purpose two methodologies are available: one uses the GSG pattern implemented with the pads, in this case it is necessary to use RF probes to connect the measurement instrument. The second option uses a RF test board with SMA connectors to connect the measurement instruments.

Table 1 resumes the measurements results, obtained in silicon, for the voltage and current references.

Table 1. Voltage and Current reference silicon results.

VDD	1,7		1,8		1,9		Humidity [%]
Temperature	I [µA]	V [mV]	I [µA]	V [mV]	I [µA]	V [mV]	
5°	10,36	968	10,36	970	10,36	968	60
20°	10,38	960	10,37	952	10,35	951	
40°	10,54	982	10,57	1020	10,7	1050	
60°	10,55	1320	10,58	1400	10,6	1520	20
80º	10,86	1230	10,78	1230	10,8	1280	
90°	10,8	1260	10,82	1370	10,9	1400	
90°	12,55	N/A	12,4	N/A	12,6	N/A	60
90°	15,7	N/A	N/A	N/A	N/A	N/A	70
90°	N/A	N/A	17	N/A	N/A	N/A	73
90°	N/A	N/A	N/A	N/A	19,3	N/A	75
90°	18,2	N/A	18,6	N/A	19,1	N/A	80
Iref nominal	**10 [µA]**						
Vref nominal	**900 [mV]**						

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit:

- The TSMC process divides the pad structure between two different instances: I/O pads and bondingpads, as opposed to other technologies that implement the pad structure on a single instance. This is not obvious at first because we access the pad as a blackbox. Also, This issue imposes a challenge when doing the DRC and LVS verification at top level.
- The measurement of RF circuits is challenging by itself. Also, the lack of documentation regarding the pads, bring some challenges to obtain a passive model to predict the losses and the impact of the pad on the measurements.

Resulting publications (submitted, accepted or published) and degrees earned by students:

- Miguel Gómez, "A Wide Tuning Range LC-VCO for the ISM Radio Band", SBMicro 2018.
- José Ramirez, "CML Ring Oscillator for the ISM band", WCAS 2017.

Obs: The measurements are still in progress along 2018. The main results of this work will be the core os a master Thesis in course.