TUTORIAL: All-GaN GaN-ICs in the IMEC’s GaN-on-SOI technology
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### WHAT IS THIS TUTORIAL ABOUT?

#### INTRODUCTION

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<th>GaN discrete components</th>
<th>Monolithic integration</th>
<th>Technological problems to solve</th>
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| * Dominate the GaN market today  
  * Off-the-shelf components or customized designs through foundry | * To unlock full potential of fast switching GaN technology:  
  - Reduction of parasitics between driver and power device  
  - Reduction of parasitics on switching node of half-bridge  
  - For those applications where it makes sense, both performance wise as cost-wise | * Back-gating effects in half-bridges  
  * Low-voltage control and diagnostics circuits monolithically integrated with high-voltage power devices  
  * Suite of passive components |

| Circuit design problems to solve | |
|---------------------------------| |
| * Design of gate driver without complementary devices  
  * Level shifting for high-side driver/switch  
  * Logic gates / Analog sub-circuits without complementary devices |
WHAT IS THIS TUTORIAL ABOUT?
FROM DISCRETE COMPONENTS TO GaN-ICs

THIS IS WHAT THIS TUTORIAL IS ABOUT!
WHAT IS THIS TUTORIAL ABOUT?
FROM DISCRETE COMPONENTS TO GaN-ICs

3 dies

Driver IC in Si technology

HS

LS

2 dies

HS driver in GaN

LS driver in GaN

1 die

Ramp generator
Error amplifier
Comparator
Dead-time control

2 dies

Driver IC in Si technology

HS

LS

30-mm HS

100-mm LS

And one step further (and its all in GaN)
BACK-GATING EFFECT IN HALF-BRIDGES
**KNOWN EFFECT IN CMOS**

**BODY EFFECT**

Change in threshold voltage ...When $V_{SB} \neq 0$ Volt

Body effect

The body effect is the change in the threshold voltage by an amount approximately equal to the change in the source-bulk voltage, $V_{SB}$, because the body influences the threshold voltage (when it is not tied to the source). It can be thought of as a second gate, and is sometimes referred to as the back-gate effect.

For an enhancement-mode nMOS MOSFET, the body effect upon threshold voltage is computed according to the Shiromizu-Hodges model, which is accurate for older process nodes, using the following equation:

$$V_{TN} = V_{TO} + \gamma \left( |V_{SB}| - 2\phi_F - \sqrt{2\phi_F} \right)$$

where $V_{TN}$ is the threshold voltage when substrate bias is present, $V_{SB}$ is the source-to-body substrate bias, $2\phi_F$ is the surface potential, and $V_{TO}$ is threshold voltage for zero substrate bias. $\gamma = (\varepsilon_{ox}/\varepsilon_{Si}) \sqrt{2\phi_F}$ is the body effect parameter, $\varepsilon_{ox}$ is oxide permittivity, $\varepsilon_{Si}$ is the permittivity of silicon, $N_A$ is a doping concentration, $q$ is elementary charge.

**Example:** nmos in pwell

If pwell is not connected to same potential as source

![Diagram showing nmos in pwell](image)

$V_S$, $V_D$, $V_B$
BACK-GATING EFFECT IN P-GAN HEMT?

Example: nmos in pwell
If pwell is not connected to same potential as source

Example: p-GaN HEMT on Silicon substrate
WHY IS IT IMPORTANT FOR MONOLITHIC INTEGRATION OF HALF-BRIDGES?

Example for $V_{in} = 200$ Volt.

**When HS switch is ON**, and LS switch is OFF:

- $V_{S_LS} = 0$ Volt
- $V_{SB_LS} = 0$ Volt
- $V_{S_HS} \approx 199$ Volt

- Current in substrate
- Disconnect substrate from Source_HS, then $V_{SB} = 199$ Volt

Discrete devices: $V_{SB} = 0$ Volt

Monolithic half-bridge: $V_{SB} \neq 0$ Volt
- Loss in substrate?
- Back-gating in HS switch?
Deep silicon contact for $V_{SB}=0$ Volt for each power transistor in the half-bridge.

Buried oxide and oxide filled deep trench isolate the HS and LS devices from each other and from the silicon substrate.
The backgating effect can be fully **eliminated** by connecting the source terminals to their respective Si(111) device layer.
The backgating effect **cannot** be removed by simply **floating** the Si(111) device layer;

The substrate contact is **indispensable**.
ELECTRICAL CHARACTERISTICS P-GAN POWER HEMT AND ISOLATION
Buffer leakage in spec over temperature range and voltage range. Stress and recovery measurements on the buffer using a 2DEG resistor shows that the buffer is low in dispersion over temperature range. (Trapping effects in buffer under control)
ISOLATION

HIGH BREAKDOWN VOLTAGE FOR LATERAL AND VERTICAL ISOLATION OF HEMTs

(a) Trench lateral isolation
(b) Vertical buried SiO$_2$ iso.
P-GAN HEMT KEY CHARACTERISTICS

HEMT with $W_{EF} = 40\text{mm}$

Power devices are modeled using the MVSG model, supported by the Compact Modeling Coalition.
DEVICE DISPERSION
DYNAMIC $R_{ON}$

Pulse conditions for measurement of the dynamic $R_{DS\_ON}$

Normalized dynamic $R_{DS\_ON}$ as a function of the quiescent voltage. Very low dispersion is observed.
INTEGRATED PASSIVE COMPONENTS (FREE COMPONENTS)
INTEGRATED PASSIVE COMPONENTS THAT COME FREE WITH THE TECHNOLOGY

High-ohmic Resistor

Resistor using the 2-dimensional electron gas.  600 Ω/

Spice model including:
• Linear and quadratic voltage linearity coefficients
• Linear and quadratic temperature coefficients

Low Ohmic Resistor

Resistor using the metal layer of the ohmic contacts.  1.7 Ω/

Spice model including:
• Linear voltage linearity coefficient
• Linear and quadratic temperature coefficients

MIM capacitor

Back-end capacitor using the metal layers for the ohmic contacts, gate metal and metal 1.  0.3 fF/μm²

Layout recommendation:
• Electrode in Ohmic metal has large series resistance
• Use stripe geometry capacitor unit cells for Rs reduction
EXAMPLES: P-GAN HEMTS WITH INTEGRATED DRIVERS
P-GAN HEMT WITH INTEGRATED DRIVER
DEMONSTRATION

(a) RTL Push-pull

(b) GaN IC

(c) Voltage waveforms at different frequencies:
- 1 MHz
- 5 MHz
- 10 MHz
- 20 MHz

Diagrams showing the integration of GaN HEMT with an integrated driver, demonstrating key components and waveforms.
HALF-BRIDGE WITH INTEGRATED DRIVERS
DEMONSTRATION IN 48 TO 1 VOLT BUCK CONVERTER
EXAMPLES : LOGIC GATES
Using the 2DEG resistor and a low voltage GaN HEMT, basic logic functions can be designed in RTL (Resistor-Transistor Logic):

- The low voltage GaN HEMT is designed with small effective gate width (e.g. 6μm) and $L_{GD} = 1.5\mu m$.
- Threshold voltage is approximately the same as for the power device.
EXAMPLES : ANALOG FUNCTIONS / PROTECTION CIRCUITS / ...
ANALOG BLOCK DESIGN USING TRANSISTORS/RESISTORS/CAPACITORS

Example 1: 48 to 1 Volt (monolithic) buck converter

(a) Ramp generator

(b) (Simulation result)
## Diagnostic and protection circuits examples

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<th>Undervoltage lock-out</th>
<th>Over-Temperature protection</th>
<th>Over-current protection</th>
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<td><strong>All – GaN</strong></td>
<td><strong>... Monolithically integrated!</strong></td>
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HOW TO GET ACCESS TO THIS GaN-IC TECHNOLOGY?
GaN-IC PROTOTYPING AND VOLUME PRODUCTION
TECHNOLOGY ACCESS (PROTOTYPING)

• MULTI-PROJECT WAFER SERVICE (MPW)

- Access to low cost prototyping runs through MPW service
- Mask and wafer fabrication costs are shared between customers
- Small NRE costs
- Extensive check on all submitted designs
- Limit on max number of wafers processed

Contact: ganmpw@imec-int.com

http://europractice-ic.com/mpw-prototyping/power-electronics/
TECHNOLOGY ACCESS (LOW VOLUME PRODUCTION)

• DEDICATED RUNS

- Dedicated mask runs which return approximately 12 x 200 mm/8 inch wafers. Prices on request

- For even larger production runs, we offer the possibility of engaging with external manufacturing partners

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