TUTORIAL: All-GaN GaN-ICs in the IMEC's GaN-on-SOI technology

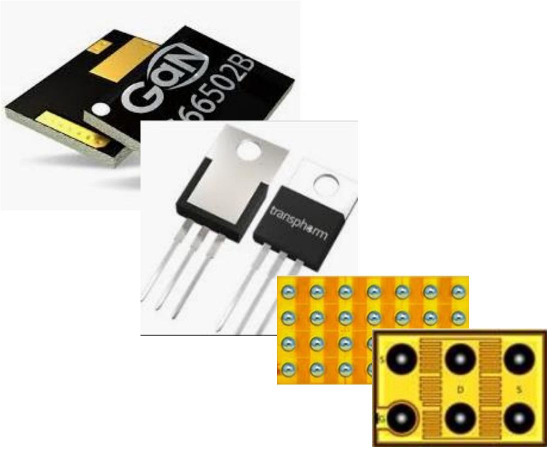
STEFAAN DECOUTERE AUG' 2019

WHAT IS THIS TUTORIAL ABOUT ?

INTRODUCTION

GaN discrete components

- Dominate the GaN market today
- Off-the-shelf components or customized designs through foundry



Monolithic integration

- To unlock full potential of fast switching GaN technology:
    - Reduction of parasitics between driver and power device
    - Reduction of parasitics on switching node of half-bridge
- For those applications where it makes sense, both performance wise as cost-wise

Technological problems to solve

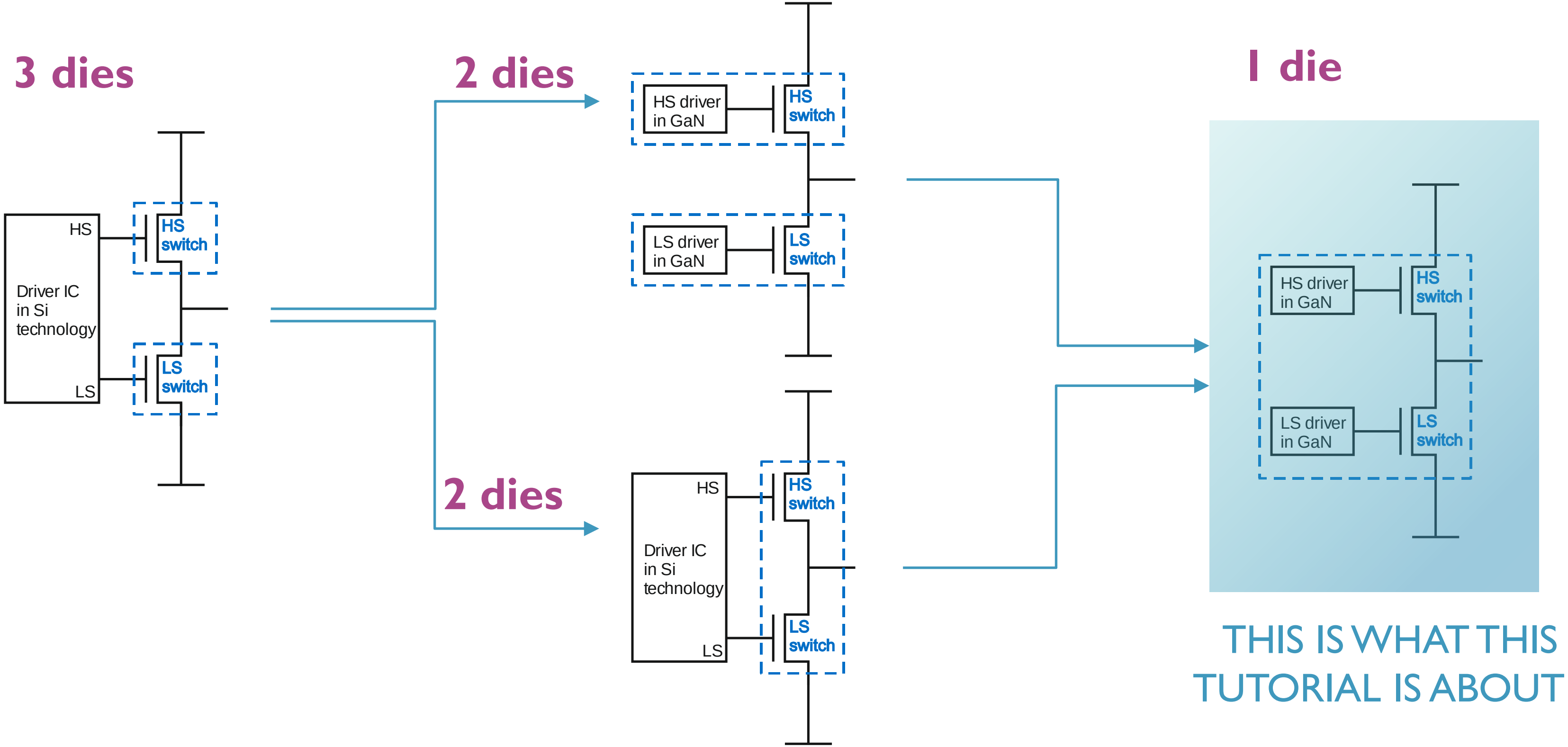
- Back-gating effects in half-bridges
- Low-voltage control and diagnostics circuits monolithically integrated with high-voltage power devices
- Suite of passive components

Circuit design problems to solve

- Design of gate driver without complementary devices
- Level shifting for high-side driver/switch
- Logic gates / Analog sub-circuits without complementary devices

WHAT IS THIS TUTORIAL ABOUT ?

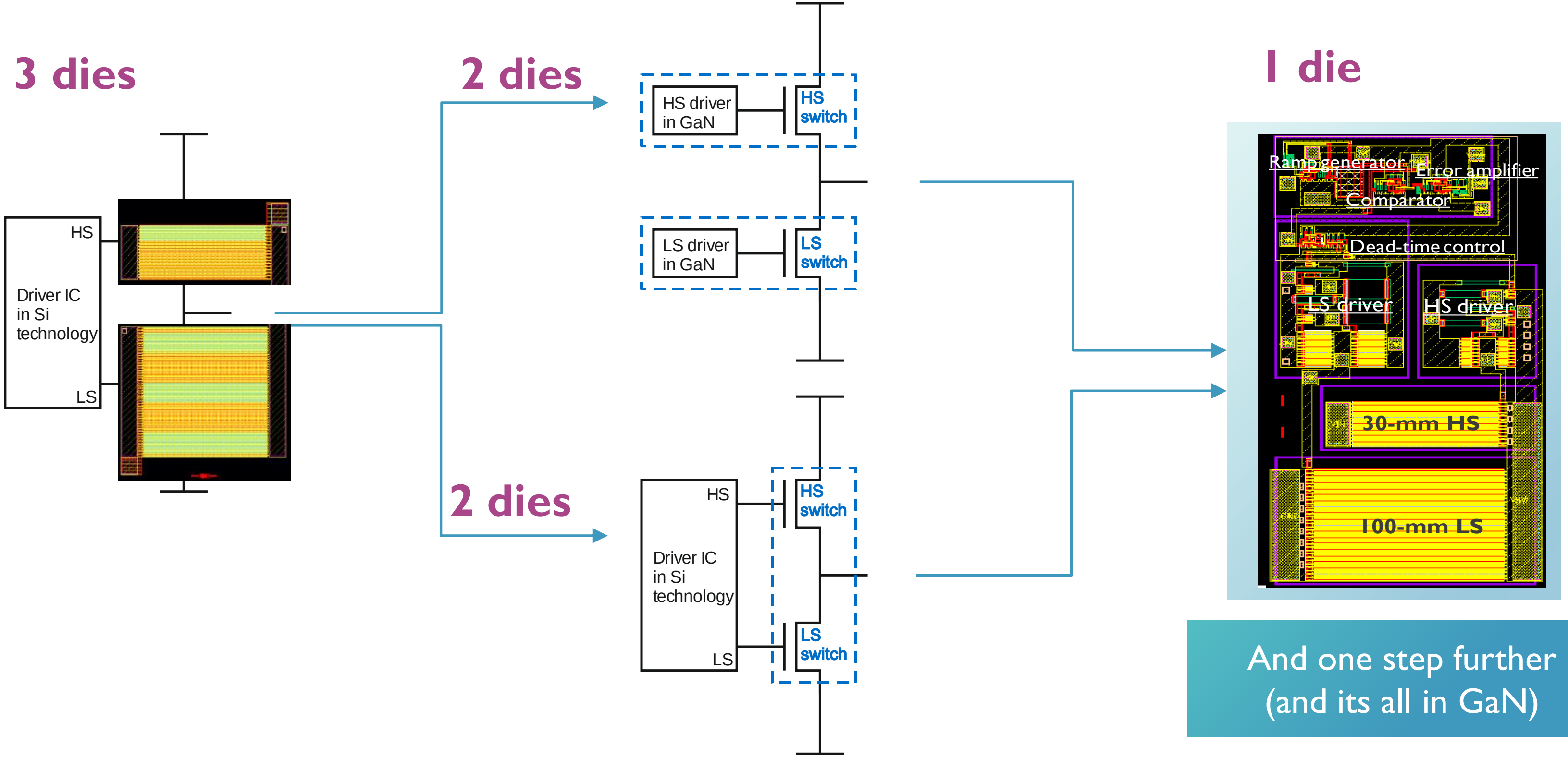
FROM DISCRETE COMPONENTS TO GaN-ICs



THIS IS WHAT THIS TUTORIAL IS ABOUT !

WHAT IS THIS TUTORIAL ABOUT ?

FROM DISCRETE COMPONENTS TO GaN-ICs



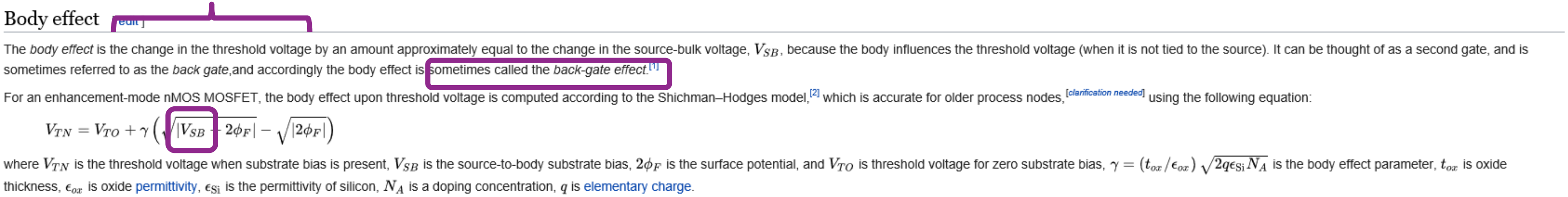
And one step further
(and its all in GaN)

BACK-GATING EFFECT IN HALF-BRIDGES

KNOWN EFFECT IN CMOS

BODY EFFECT

Change in threshold voltage …When $V_{SB} \neq 0$ Volt



Body effect [edit]

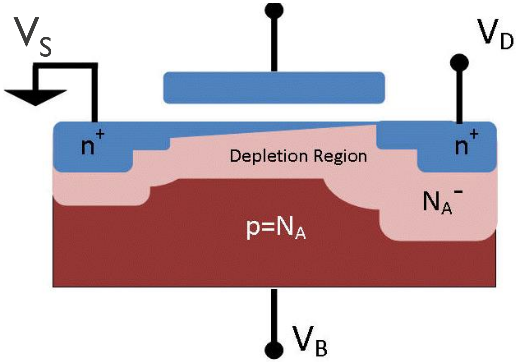
The *body effect* is the change in the threshold voltage by an amount approximately equal to the change in the source-bulk voltage, V_{SB}, because the body influences the threshold voltage (when it is not tied to the source). It can be thought of as a second gate, and is sometimes referred to as the *back gate*,and accordingly the body effect is sometimes called the *back-gate effect*.[1]

For an enhancement-mode nMOS MOSFET, the body effect upon threshold voltage is computed according to the Shichman–Hodges model,[2] which is accurate for older process nodes,[clarification needed] using the following equation:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

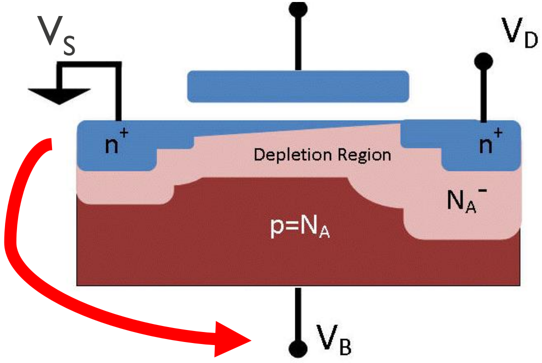
where V_{TN} is the threshold voltage when substrate bias is present, V_{SB} is the source-to-body substrate bias, $2\phi_F$ is the surface potential, and V_{TO} is threshold voltage for zero substrate bias, $\gamma = (t_{ox}/\epsilon_{ox})\sqrt{2q\epsilon_{\text{Si}}N_A}$ is the body effect parameter, t_{ox} is oxide thickness, ϵ_{ox} is oxide permittivity, ϵ_{Si} is the permittivity of silicon, N_A is a doping concentration, q is elementary charge.

Example : nmos in pwell
If pwell is not connected to same potential as source

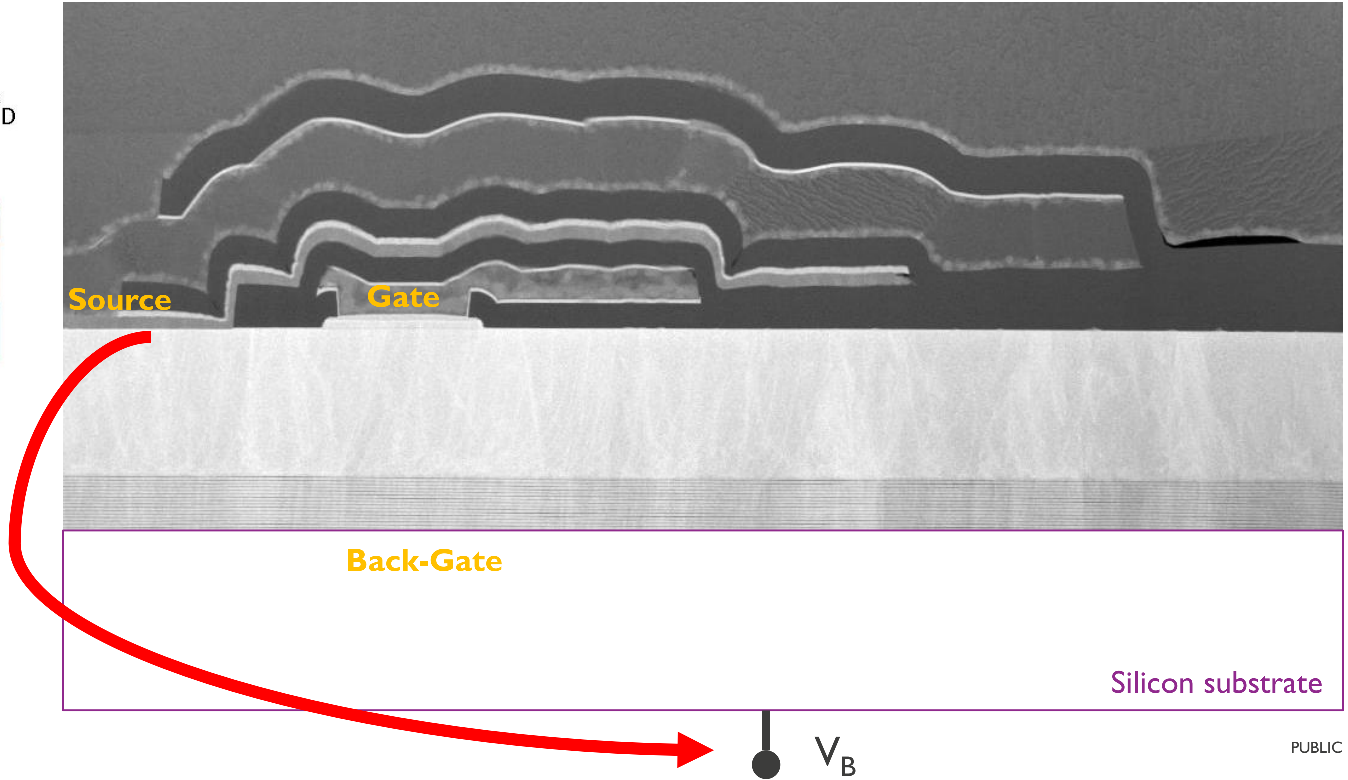


BACK-GATING EFFECT IN P-GAN HEMT ?

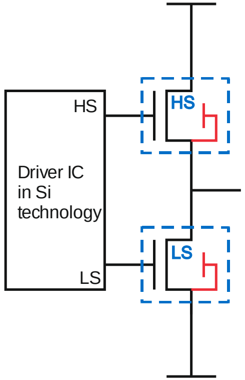
Example : nmos in pwell
If pwell is not connected to same potential as source



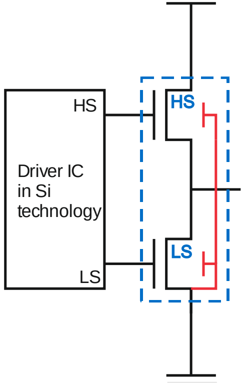
Example : p-GaN HEMT on Silicon substrate



WHY IS IT IMPORTANT FOR MONOLITHIC INTEGRATION OF HALF-BRIDGES ?



Discrete devices :V_{SB} = 0 Volt



Monolithic half-bridge : VSB ≠ 0 Volt
Loss in substrate ?
Back-gating in HS switch ?

Example for Vin = 200 Volt.
When HS switch is ON, and
LS switch is OFF :

VS_LS = 0 Volt

VSB_LS = 0 Volt

VS_HS ~ 199 Volt

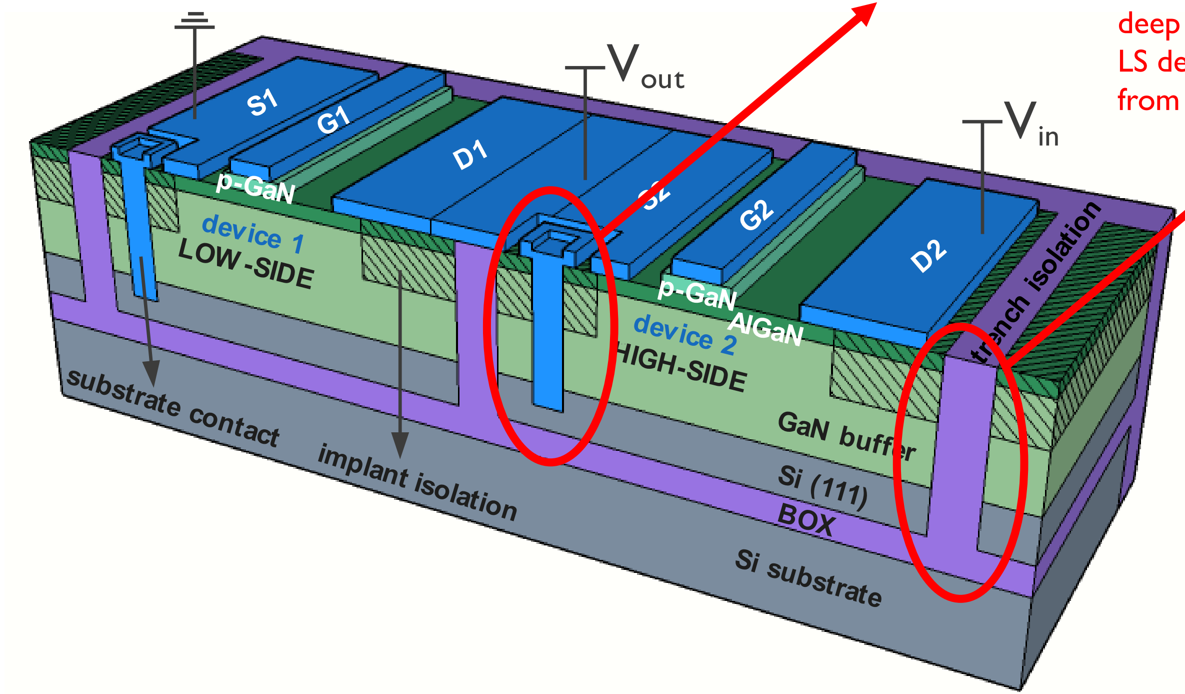
- Current in substrate
- Disconnect substrate from Source_HS, then VSB = 199 Volt

PROPOSED SOLUTION

GaN-on-SOI WITH DEEP TRENCH ISOLATION

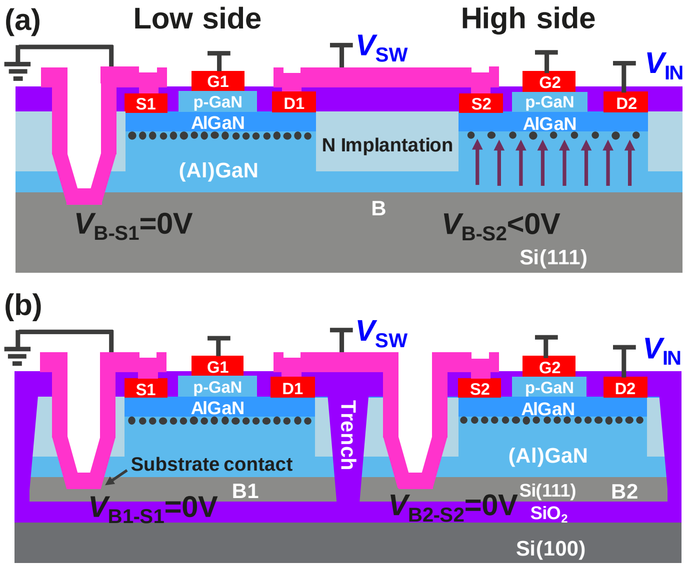
Deep silicon contact for V_{SB}=0 Volt for each power transistor in the half-bridge.

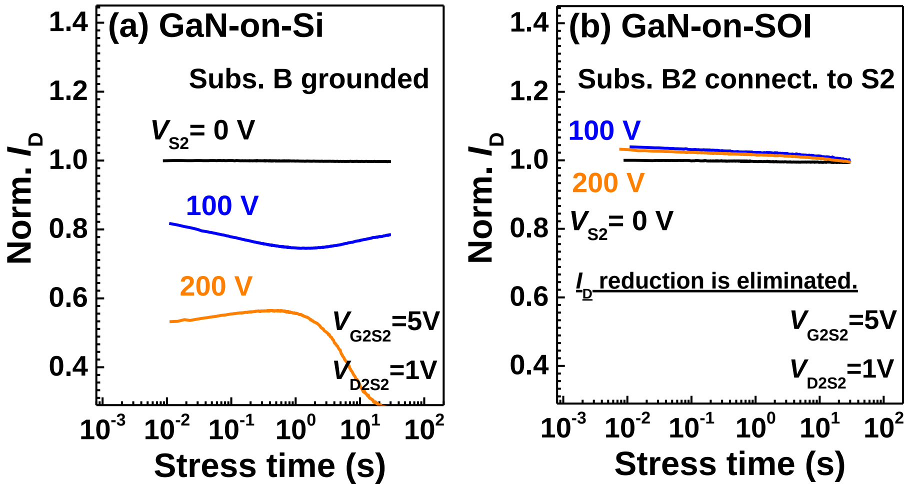
Buried oxide and oxide filled deep trench isolate the HS and LS devices from each other and from the silicon substrate.



ELECTRICAL MEASUREMENT OF GaN-on-SOI

BACKGATING EFFECT

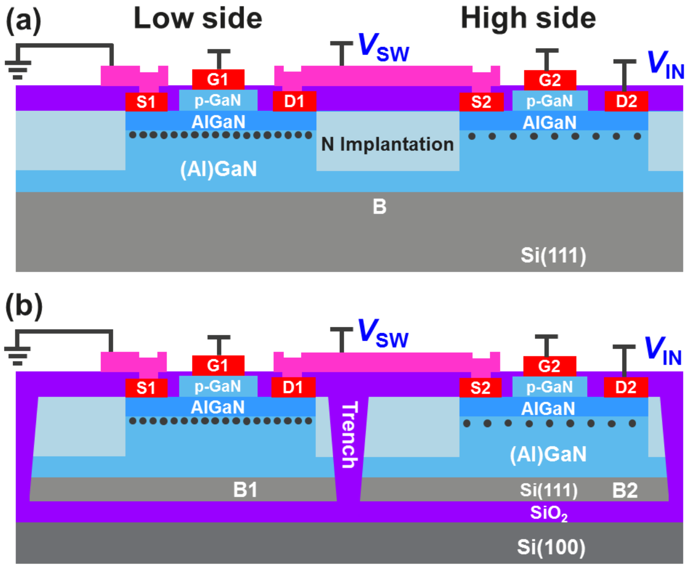


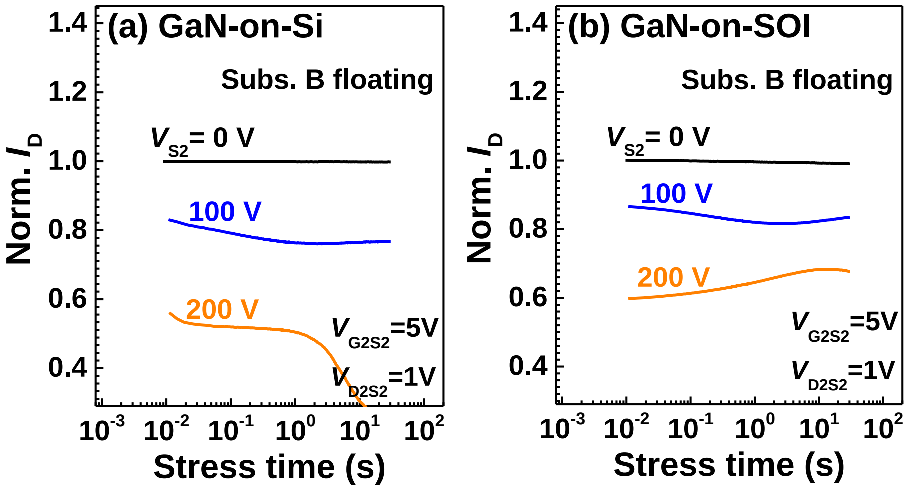


- The backgating effect can be fully **eliminated** by connecting the source terminals to their respective Si(111) device layer.

ELECTRICAL MEASUREMENT OF GaN-on-SOI

BACKGATING EFFECT

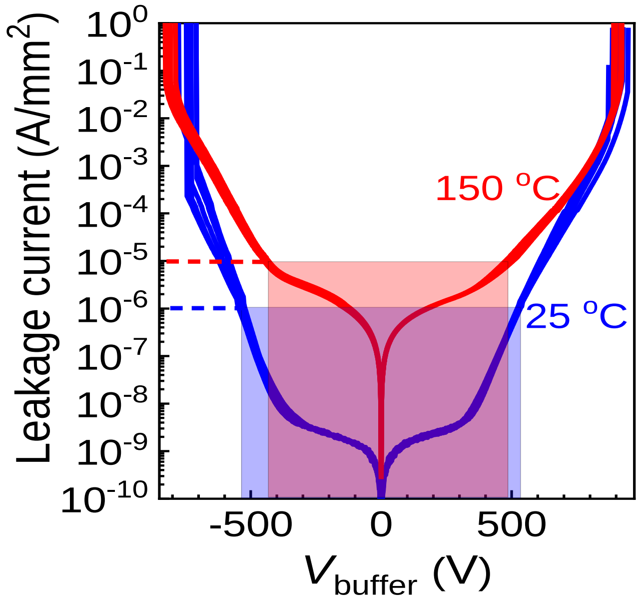




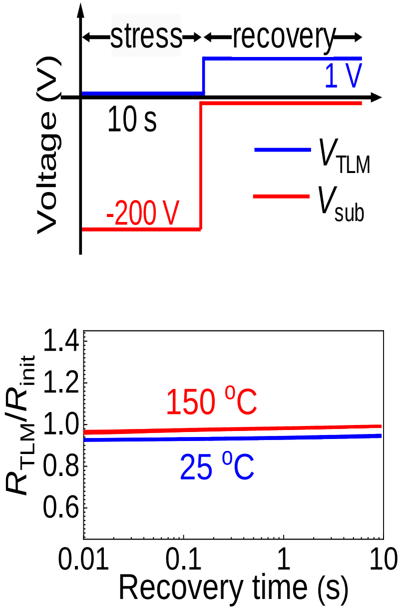
- The backgating effect **cannot** be removed by simply **floating** the Si(111) device layer;
- The substrate contact is **indispensable**.

ELECTRICAL CHARACTERISTICS P-GAN POWER HEMT AND ISOLATION

BUFFER CHARACTERISTICS



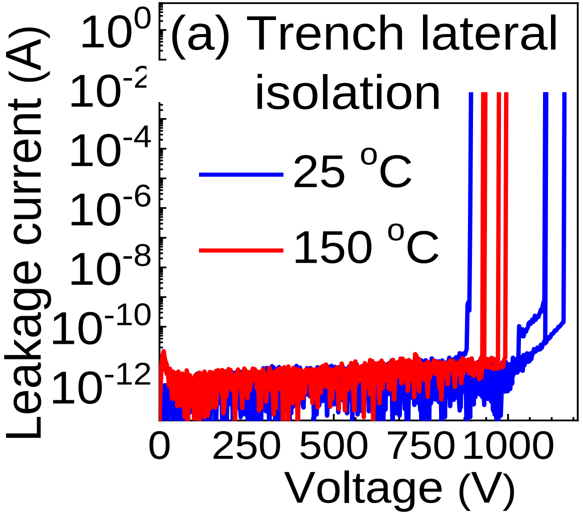
Buffer leakage in spec over temperature range and voltage range.

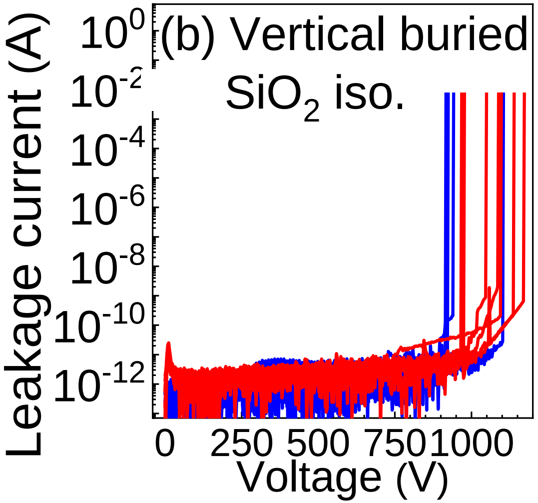


Stress and recovery measurements on the buffer using a 2DEG resistor shows that the buffer is low in dispersion over temperature range.(Trapping effects in buffer under control)

ISOLATION

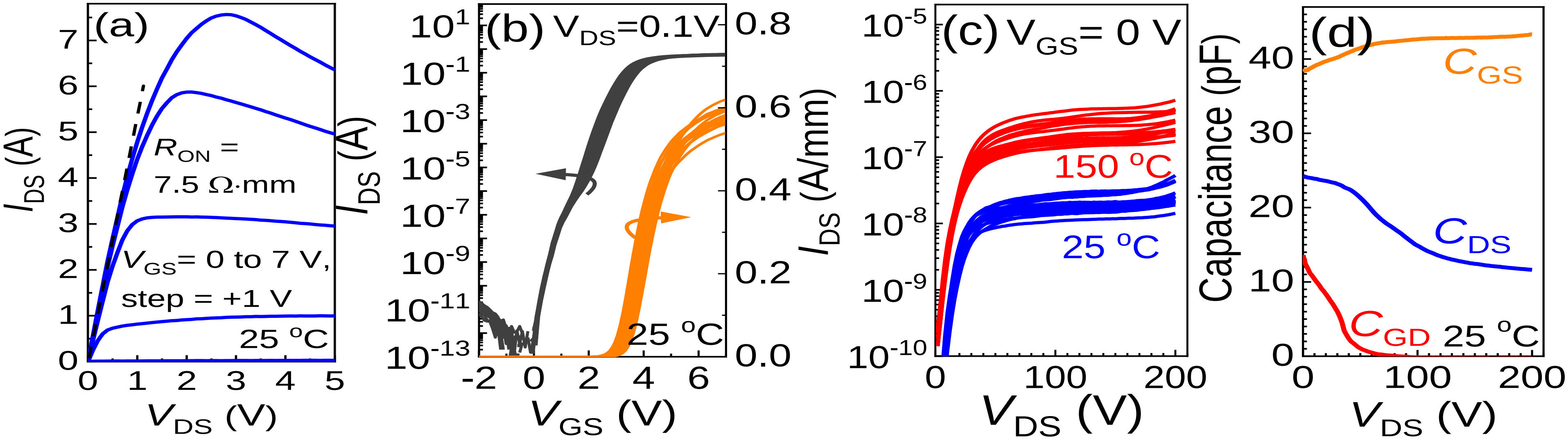
HIGH BREAKDOWN VOLTAGE FOR LATERAL AND VERTICAL ISOLATION OF HEMTs





P-GAN HEMT KEY CHARACTERISTICS

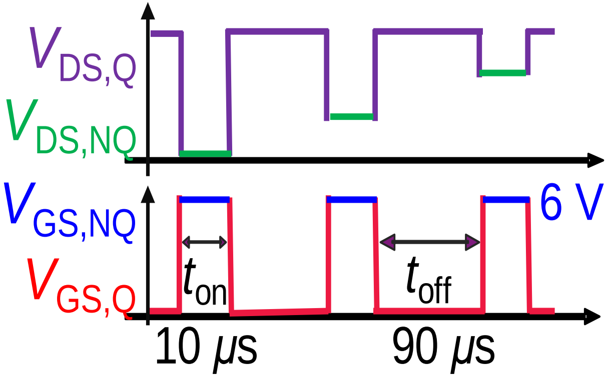
HEMT with W_{EF} = 40mm



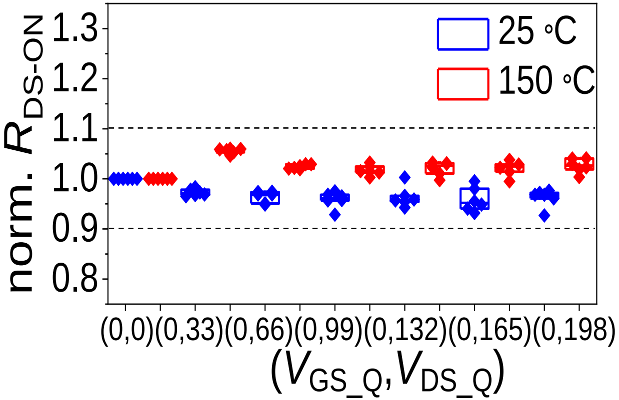
Power devices are modeled using the MVSG model, supported by the Compact Modeling Coalition

DEVICE DISPERSION

DYNAMIC R_{ON}



Pulse conditions for measurement of the dynamic R_{DS_ON}



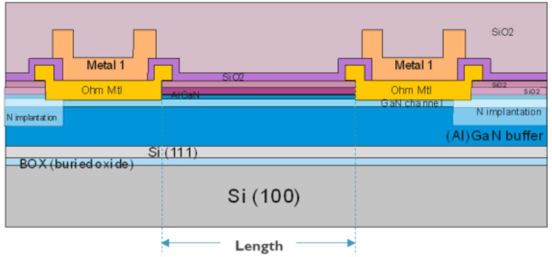
Normalized dynamic R_{DS_ON} as a function of the quiescent voltage. Very low dispersion is observed.

INTEGRATED PASSIVE COMPONENTS (FREE COMPONENTS)

INTEGRATED PASSIVE COMPONENTS THAT COME FREE WITH THE TECHNOLOGY

High-ohmic Resistor

Resistor using the 2-dimensional electron gas. 600 Ω/ □

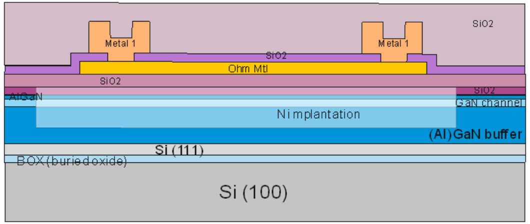


Spice model including :

- Linear and quadratic voltage linearity coefficients
- Linear and quadratic temperature coefficients

Low Ohmic resistor

Resistor using the metal layer of the ohmic contacts. 1.7 Ω/ □

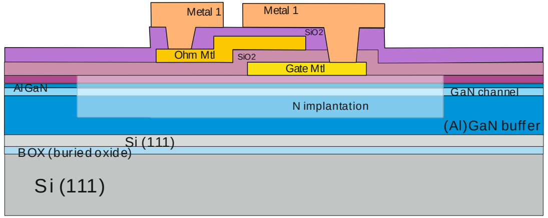


Spice model including :

- Linear voltage linearity coefficient
- Linear and quadratic temperature coefficients

MIM capacitor

Back-end capacitor using the metal layers for the ohmic contacts, gate metal and metal 1. 0.3 fF/μm^2



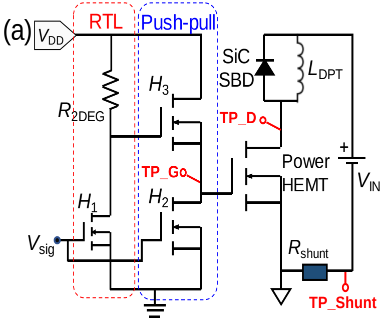
Layout recommendation :

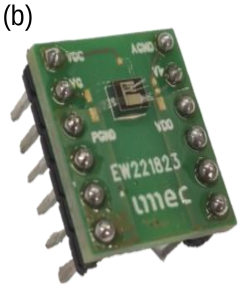
- Electrode in Ohmic metal has large series resistance
- Use stripe geometry capacitor unit cells for Rs reduction

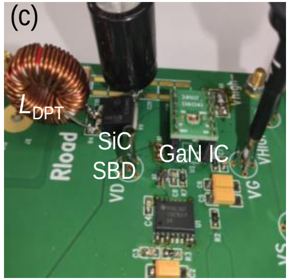
EXAMPLES : P-GAN HEMTS WITH INTEGRATED DRIVERS

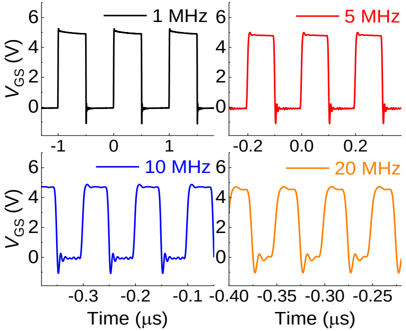
P-GAN HEMT WITH INTEGRATED DRIVER

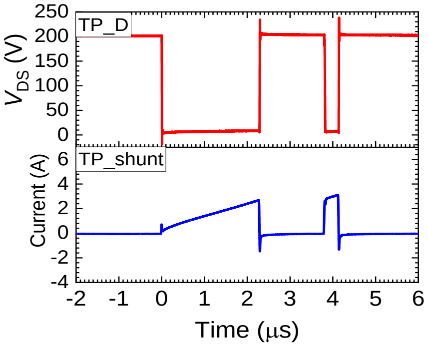
DEMONSTRATION





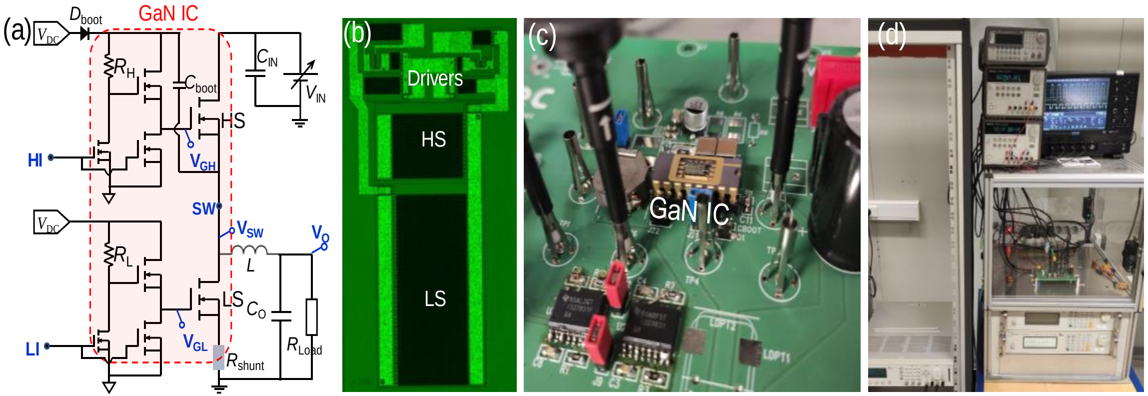


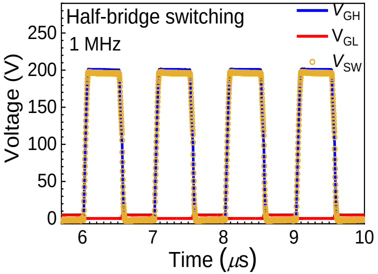


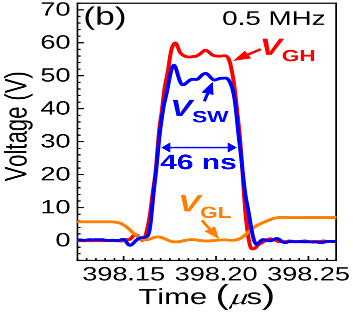


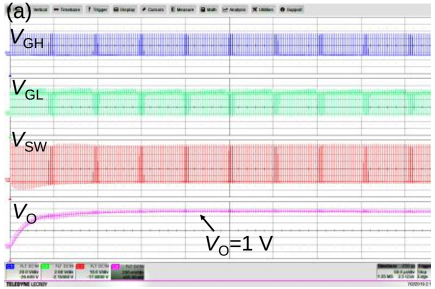
HALF-BRIDGE WITH INTEGRATED DRIVERS

DEMONSTRATION IN 48 TO 1 VOLT BUCK CONVERTER









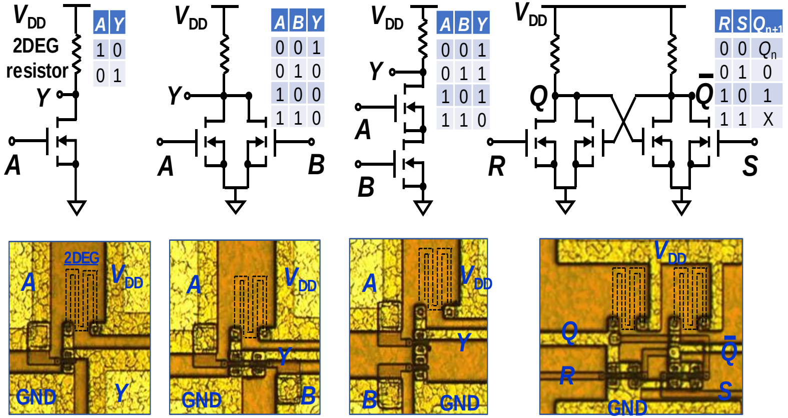
EXAMPLES : LOGIC GATES

LOGIC FUNCTIONS IN A GaN POWER TECHNOLOGY

RTL : RESISTOR – TRANSISTOR LOGIC

Using the 2DEG resistor and a low voltage GaN HEMT, basic logic functions can be designed in RTL (Resistor-Transistor Logic):

- The low voltage GaN HEMT is designed with small effective gate width (e.g. 6µm) and L_{GD}= 1.5µm.
- Threshold voltage is approximately the same as for the power device.



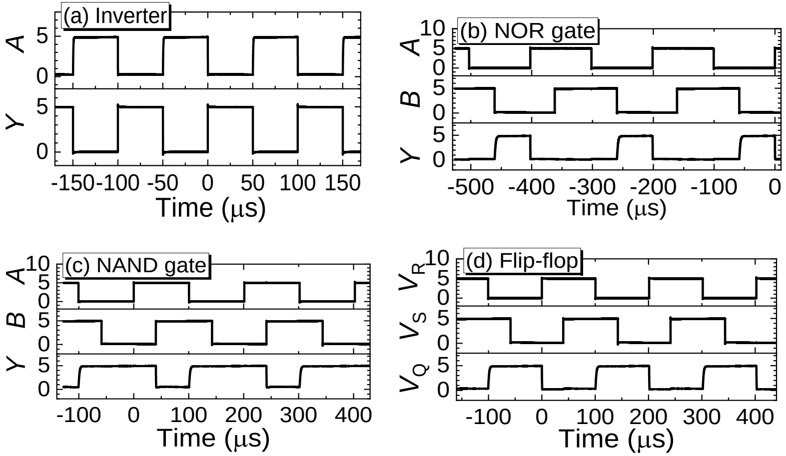
A	Y
1	0
0	1

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

R	S	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

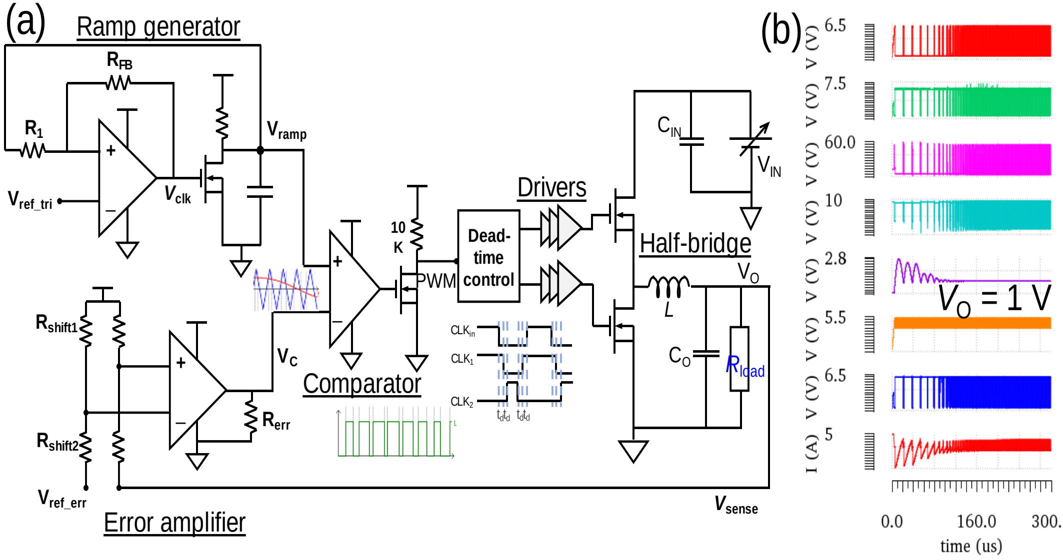
(a) Inverter **(b) NOR** **(c) NAND** **(d) Flip-flop**



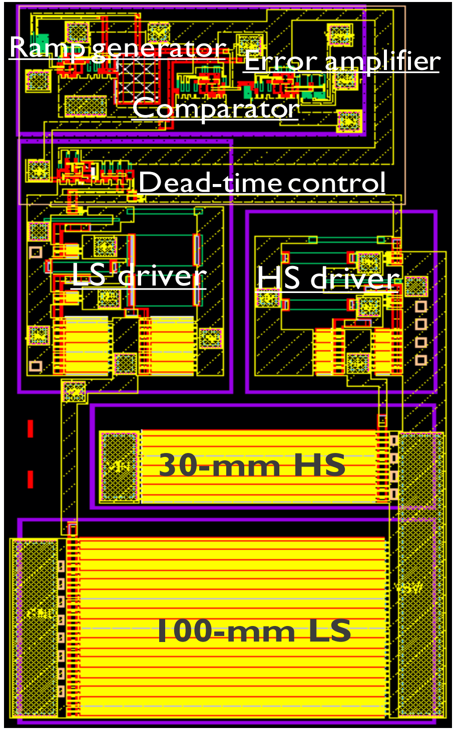
EXAMPLES : ANALOG FUNCTIONS / PROTECTION CIRCUITS / …

ANALOG BLOCK DESIGN USING TRANSISTORS/RESISTORS/CAPACITORS

Example 1 : 48 to 1 Volt (monolithic) buck converter



(Simulation result)



DIAGNOSTIC AND PROTECTION CIRCUITS

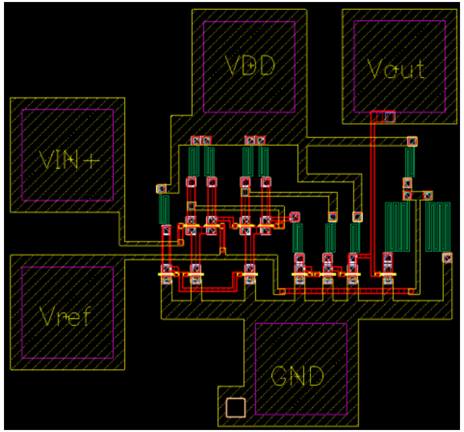
EXAMPLES

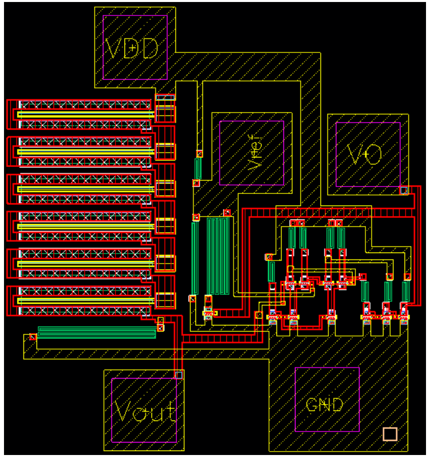
Undervoltage lock-out

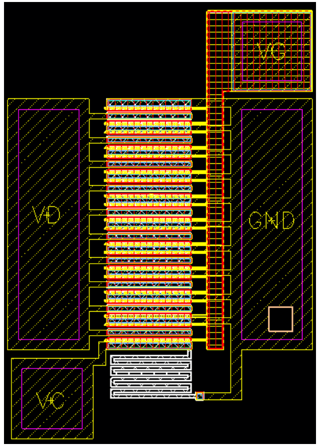
Over-Temperature protection

Over-current protection

All – GaN … Monolithically integrated !





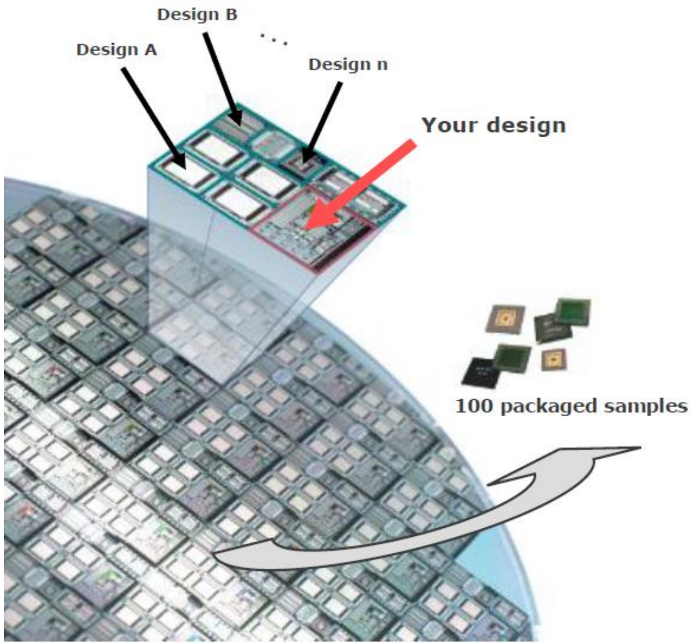


HOW TO GET ACCESS TO THIS GaN-IC TECHNOLOGY ?

GaN-IC PROTOTYPING AND VOLUME PRODUCTION

TECHNOLOGY ACCESS (PROTOTYPING)

- MULTI-PROJECT WAFER SERVICE (MPW)



**Reference to a MPW wafer, please verify the current commercial offer.*

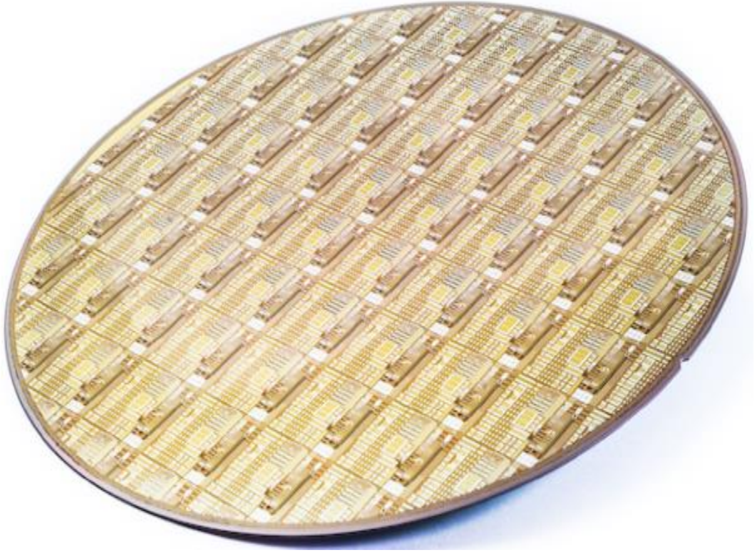
- Access to low cost prototyping runs through MPW service
- Mask and wafer fabrication costs are shared between customers
- Small NRE costs
- Extensive check on all submitted designs
- Limit on max number of wafers processed

Contact: ganmpw@imec-int.com

https://www.imec-int.com/en/innovation/build-your-gan-ics-with-imec-s-gan-on-soi-mpw-process
http://europractice-ic.com/mpw-prototyping/power-electronics/

TECHNOLOGY ACCESS (LOW VOLUME PRODUCTION)

- DEDICATED RUNS



- Dedicated mask runs which return approximately 12 x 200 mm/8 inch wafers. Prices on request
- For even larger production runs, we offer the possibility of engaging with external manufacturing partners

Contact: ganmpw@imec-int.com

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