ACTIVITY REPORT

2019-2020

EUROPRACTICE

EUROPRACTICE

THE ACCESS POINT FOR INDUSTRY AND ACADEMIA TO ELECTRONIC COMPONENTS AND SYSTEMS

EUROPRACTICE was launched by the European Commission in 1989 to help companies improve their competitive position in world markets by adopting ASIC, Multi-Chip Module or Microsystems solutions in their products. The program helps to reduce the perceived risks and costs associated with these technologies by offering potential users a range of services, including initial advice and ongoing support, reduced entry costs and a clear route to chip manufacture and product supply.

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by offering more than 600 European universities and research institutes affordable access to the latest IC (Integrated Circuits) design tools and technologies. This is reflected in the training provided by universities from which the best IC design engineers emerge, essential for the SMEs innovation in new IC products.

The ultimate goal of EUROPRACTICE is to enhance European industrial competitiveness in the global marketplace. The EUROPRACTICE services are open to industrial companies (especially SMEs), research institutes and academic users.

SERVICES OFFERED TO EUROPEAN SMEs AND ACADEMIC INSTITUTIONS:

The mission statement of EUROPRACTICE is to provide the European industry and academia with a platform to develop smart integrated systems, from advanced prototype design to volume production. The latter is achieved by providing affordable and easier access to a wide range of state-of-the-art industry-grade fabrication technologies and design tools complemented with training and support to the customer in all critical steps which are needed.

- Affordable access to industry-standard and state-of-the-art design (CAD) tools
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- Low-cost prototyping in various technologies (both ASIC and More than Moore) via MPW runs
- Access to advanced packaging and smart system integration
- Training courses in advanced design flows and on various technologies

IC SERVICES OFFERED TO THE GLOBAL INDUSTRY:

EUROPRACTICE also offers industry worldwide access to microelectronic and microsystem design services, MPW prototyping, small volume production, packaging, smart system integration and test operations. Note, this does not include access to design tools. Industry from all over the world has rapidly discovered the benefits of using the EUROPRACTICE-IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who do not always need the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise. All these services are provided by EUROPRACTICE-IC, a well-established service that has been in the market for 20 years.

THE EUROPRACTICE SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:

- imec (Belgium)
- UKRI-STFC Rutherford Appleton Laboratory (United Kingdom)
- Fraunhofer-Institut für Integrierte Schaltungen (Fraunhofer IIS) (Germany)
- CMP (France)
- Tyndall National Institute (Ireland)

FOREWORD

Dear customers, colleagues and friends,

Another year has passed, and another decade has arrived. The results of 2019 are summarized in the new EUROPRACTICE Activity Report 2019-2020, which is in your hands now. We hope you will enjoy reading about our achievements in the past year and looking forward to the new year.

2019 was a busy challenging year, since the services from two new partners CMP and Tyndall have been integrated into EUROPRACTICE, as a result of the new EU-funded (H2020) project, named the ***Next EUROPRACTICE eXtended Technologies and Services*** (NEXTS). The integration of those new technologies and services can be immediately seen from the high number of designs fabricated through our EUROPRACTICE service. We realized a total of ***884 design submissions*** in a wide range of technologies with 75% of the designs submitted by European universities, research institutes and companies. Although EUROPRACTICE focuses mainly on European customers, its service and technologies are also accessible outside Europe. More and more customers from Asia are using the EUROPRACTICE prototyping services resulting in a total volume of 128 designs in 2019.

EUROPRACTICE offers a good technology mix for its customers. The older technology nodes (ranging from 0.7µm to 0.11µm) are still very popular and represent approximately half of the total designs which have been fabricated. For the more advanced nodes, 65nm is the most popular technology node with 172 realized designs. In addition, the FDSOI technologies from STMicroelectronics and GLOBALFOUNDRIES are also very popular with more than 50 designs. The 22nm FDSOI technology from GLOBALFOUNDRIES has tripled its number of designs – going from 5 in 2018 to 15 in 2019. The popularity of Silicon Photonics has been confirmed in 2019. Finally, a first design has been fabricated in GaN-IC technology, which has been added very recently to the EUROPRACTICE technology portfolio.

In ***2019***, EUROPRACTICE increased its outreach activities in order to get even closer to its customers. EUROPRACTICE has been exhibiting at the microelectronics top conferences world-wide, such as ISSCC, ESSCIRC/ESSDERC and TRANSDUCERS, and has also organized dedicated User Meetings / National Seminars. In 2019, a total of 4 National Seminars took place in Munich (Germany), London (UK), Zurich (Switzerland) and Cork (Ireland). In addition, EUROPRACTICE rejuvenated its marketing and communication material – with as main result a brand-new website, new vibrant technology flyers, a promotional video and an active presence on LinkedIn. Finally, on the training front Tyndall organized a first EUROPRACTICE webinar on Advanced Photonics packaging.

In ***2020***, EUROPRACTICE will continue to deliver a high-quality service for its customers. New technologies will be accessible from our portfolio, such as a new 0.18µm technology from EM Microelectronic and a new MEMS technology from X-FAB. New class-room trainings and webinars will be developed and presented to a broad range of users, including traditional electronic sectors and non-traditional sectors (for instance, MedTech and Agri Food) and as such support the training of future generations of engineers that will be required for the growing digital economy in Europe. Moreover, an enhanced service offering towards smart system integration is expected in 2020. Ultimately, EUROPRACTICE will act as a true one-stop shop for technologies enabling fully integrated systems and providing direct routes for industrial up-scaling of those systems and consequently it will contribute to creating and sustaining new jobs in Europe, especially in the areas of design and fabrication of microelectronic components and systems.

We thank the European Commission (DG Connect) for their support. The EC funding ensures that we hold our commitment to continue the EUROPRACTICE service and to offer the European academic institutions and SMEs easy and affordable access to state-of-the-art design tools and to IC technologies.

Finally, we thank all of you, our customers from both academia and industry, our technology and design tool suppliers, for supporting our services and we wish you all a successful 2020. Looking forward to another fantastic year filled with challenges and success stories.

Romano Hoofman (EUROPRACTICE General Manager)
On behalf of the entire EUROPRACTICE team at imec, UKRI-STFC, FhG-IIS, CMP and Tyndall

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THE ACCESS POINT FOR ELECTRONIC COMPONENTS AND SYSTEMS

EUROPRACTICE (1995-present) and its forerunner EUROCHIP (1989-1995) have supported the European academic sector with CAD tools and IC prototyping for almost 30 years. Moreover, SMEs have been supported with IC prototyping and small volume services for over 15 years. The provided services are widely recognized as world leading.

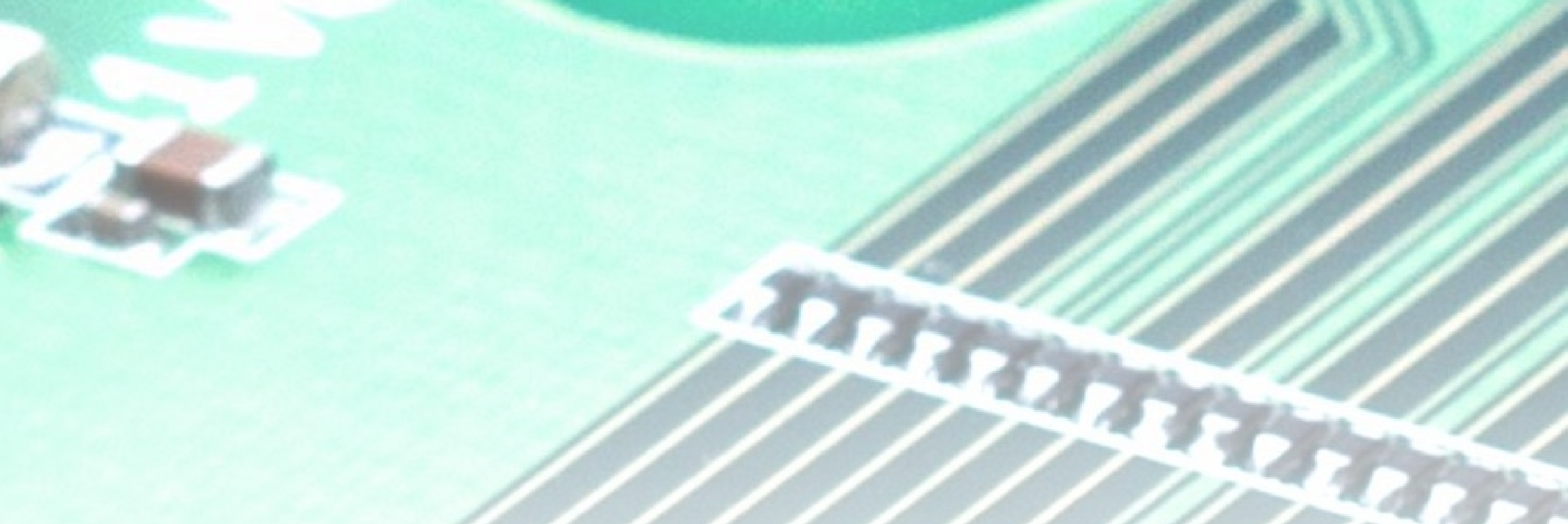
Currently, approximately 600 academic institutions from the EU member States and "extended" Europe are supported by this EUROPRACTICE service funded by the European Commission. Eligible institutions are currently able to access CAD services and MPW services at discounted prototyping prices.

The European Commission has financially supported the provided services that offer the European universities and research institutes appropriate access to CAD tools, advanced technologies, design kits, IP blocks and training to support their education, prototyping and small volume production.

In 2019, a new H2020 project has been launched, named the "Next EUROPRACTICE eXtended Technologies and Services" (NEXTS), in which two new partners CMP and Tyndall complement and extend the EUROPRACTICE offering. The project has been built upon the well-established, widely used and successful EUROPRACTICE service. The new extended services have a particular focus on SMEs and System Integration.

The mission statement of the EUROPRACTICE consortium is to provide the industry and academia (in particular those in Europe) with a platform to develop smart integrated systems, from advanced prototype design to volume production. The latter will be achieved by providing affordable and easier access to a wide range of state-of-the-art industry-grade fabrication technologies and design tools complemented with training and support to the customer in all critical steps which are needed.

Ultimately, EUROPRACTICE acts as a true one-stop shop for technologies enabling fully integrated systems and providing direct routes for industrial up-scaling of those systems and consequently it will contribute to creating and sustaining new jobs in Europe, especially in the areas of design and fabrication of microelectronic components and systems.



THE EUROPRACTICE BUSINESS MODEL

The EUROPRACTICE business model is based on a coordinated brokerage service for industry and academia looking for affordable and easier access to technologies in the domain of electronic smart systems – which builds on the many years' experience of its partners: imec, UKRI-STFC, Fraunhofer IIS, CMP and Tyndall.

EUROPRACTICE provides its customers technology access through a vast network of technology suppliers, ranging from design tool vendors and foundries to packaging, assembly & test houses – who all provide state-of-the-art industry-grade technologies.

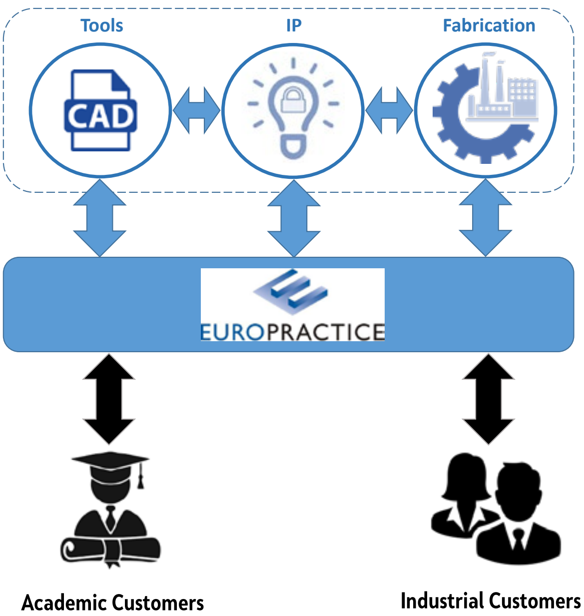


Fig. 1: Schematic representation of the entire NEXTS ecosystem, depicting a central role of the NEXTS service as prime interface between the technology suppliers (on top) and the customers (at the bottom).

The overall concept is that EUROPRACTICE acts as the prime interface between the users/customers and the technology providers (such as design tools and IP library vendors, foundries, assembly and test houses). Such a prime interface (or one-stop function) has advantages for both the supply and demand side of the value chain. The latter is schematically depicted in Figure 1, where the supply side is depicted on top, the demand side at the bottom and centrally EUROPRACTICE.

On the supply side, one can find centrally the current technology portfolio, where design tools are supplied by design tool vendors, technology IP by IP library vendors and fabrication services by various foundries. The technology portfolio is extended with emerging technologies typically offered by leading research institutes, and technologies which are brokered by other technology service providers (such as CMC in Canada for Silicon Photonics by AMF).

Although EUROPRACTICE represents a large user base, it is considered as one user to the suppliers. Design tool vendors, IP-vendors and foundries have only to deal with EUROPRACTICE, and have their products and technologies promoted and securely distributed all over Europe. Thanks to this, it has been possible to negotiate access and very favorable conditions for the EUROPRACTICE customers. This would not be possible when operating on a national level with only a very few users. Since the service is being offered on a pan-European level, the know-how and experience has only to be built up once.

AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated lower prices with the major design tool vendors world-wide and also with IP and programmable device vendors. Consequently, European academic institutions can purchase EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics etc.) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service also provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows our customers to participate in EC-funded projects, ranging from IP block and component design to complete system design.

Some mechanisms and terms and conditions have been negotiated which, subject to the approval of the specific design tool vendor to be obtained via UKRI-STFC, allow:

- a design originally undertaken for non-commercial purposes to be exploited commercially
- non-commercial licenses installed at an experienced academic institute to be used by a start-up company, e.g. an academic spin-out, under the guidance of the academic institute to produce a commercial demonstrator to prove the viability and marketability of a novel end product. The design cannot be then sold or assigned without a further appropriate payment being made directly to the design tool vendor.

These and other similar mechanisms will be introduced to help lower the barrier to effective innovation by academic institutes and start-ups.

ACCESS TO PROTOTYPING FOR ASICS, MEMS AND PHOTONICS

In general, it is challenging for academic institutes and small companies to obtain access to foundry fabrication lines since they often need a high level of technical support and require only a small-volume production for prototyping purposes.

Over the last decades, leading IC-foundries have recognized that EUROPRACTICE is the ideal partner to offer low-cost prototyping services to smaller users and academia as EUROPRACTICE is the entity that offers both access and technical support.

The current portfolio includes a wide range of technologies, such as ICs with nodes ranging from 0.7µm to 16nm, MEMS, Si-Photonics and SiN-Photonics. It also includes digital logic, RF, mixed-signal and high-voltage solutions. The service has been kept to a manageable size by endeavoring to obtain the maximum functionality from the minimum number of foundries or technologies.

Currently, seven of the nine ASIC foundries (namely, ams, EM Microelectronic, GLOBALFOUNDRIES, IHP, ON Semiconductor, STMicroelectronics and X-FAB) have manufacturing facilities in Europe and the Si-Photonics fabrication takes place in IHP, imec and CEA-Leti (where the last two are leading European RTOs).

The cost of producing a new ASIC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. EUROPRACTICE has reduced the prototyping cost, especially for ASIC prototyping, by two techniques: Multi-Project-Wafer (MPW) runs and Multi-Level Masks.

MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto one mask set and prototype run, known as Multi-Project-Wafer (MPW) runs, the high costs of a mask set is shared among the participating customers.

Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full prototyping wafer run. A limited number of tested or untested ASIC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time". In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the designs fabricated for educational purposes are much smaller than the minimum charged design size on regular MPW runs, the concept of **mini@sic** runs was introduced in 2003. This solution allows to further lower prototype fabrication costs compared to standard MPW runs. The mini@sic principle is based on the following methodology: Several times per year, a minimum area MPW block size is bought and resold in smaller and cheaper sub-blocks. This mini@sic MPW program has been extended over the years and currently includes selected technologies from GLOBALFOUNDRIES, IHP, ON Semiconductor, TSMC, UMC and X-FAB.

Since 2018, EUROPRACTICE-IC has also offered its customers a particularly small silicon area of one mm^2 to fabricate their designs in the TSMC 28nm HPC and HPC+ technology. This so-called **MICROBLOCK** can be placed on any of the 28nm Multi-Project-Wafer (MPW) runs that use the mini@sic methodology. However, in case of only one Microblock design submission, there is no commitment that the run will be launched.

TECHNOLOGY PORTFOLIO

For 2020, EUROPRACTICE will continue to extend and update its technology portfolio. Currently, customers can have access to prototype and production fabrication in the following technologies:

ams 0.35µm CMOS C35B4C3
ams 0.35µm CMOS C35OPTO
ams 0.35µm HV CMOS H35B4D3
ams 0.35µm SiGe-BiCMOS S35
BARC Diode for ams C35OPTO
WLSCP for ams C35B4C3

em microelectronic

EM Microelectronic 0.18µm EMALPC18 logic

GF SiGe 8HP
GF 130nm BCDlite
GF 130nm LP
GF 90WG Silicon Photonics
GF 55nm LPx-NVM/LPx-RF
GF 55nm Lpe
GF 45RFSOI
GF 40nm LP/LP-RF/RF-mmWave
GF 28nm SLP/SLP-RF
GF 22nm FDSOI

IHP SGB25V 0.25µm SiGe:C
IHP SG25H3 0.25µm SiGe:C
IHP SG25H5_EPIC (BiCMOS + Photonics)
IHP SG25 PIC (Photonics)
IHP SG13S 0.13µm SiGe:C
IHP SG13C 0.13µm SiGe:C
IHP SG13G2 0.13µm SiGe:C
IHP SG13G2Cu FEOL process SG13G2 together with Cu BEOL option
IHP SG13SCu FEOL process SG13S together with Cu BEOL option
IHP BEOL SG13

On Semi 0.7µm C07M-D
On Semi 0.7µm C07M-A
On Semi 0.7µm C07M-I2T100 100V
On Semi 0.5µm CMOS EEPROM C5F & C5N
On Semi 0.35µm C035U
On Semi 0.35µm C035-I3T80U 80V
On Semi 0.35µm C035-I3T50U (E) 50V
On Semi 0.35µm C035-I3T25U 3.3/25V
ONC18MS 0.18µm
ONC18MS-LL 0.18µm
ONC18HPA 0.18µm
ONC18-I4T 0.18µm 45/70V

ST 28nm CMOS28FDSOI
ST 55nm BiCMOS055
ST 65nm CMOS065
ST 130nm BiCMOS9MW
ST 130nm H9SOI-FEM
ST 130nm HCMOS9GP
ST 130nm HCMOS9A
ST 0.16µm BCD8sP
ST 0.16µm BCD8s-SOI

TSMC 0.18µm CMOS Log/MS/RF (G)
TSMC 0.18µm CMOS HV BCD Gen II
TSMC 0.13µm CMOS Log/MS/RF (G, LP)
TSMC 90nm CMOS Log/MS/RF (G ,LP)
TSMC 65nm CMOS Log/MS/RF (G, LP)
TSMC 40nm CMOS Log/MS/RF (G, LP)
TSMC 28nm CMOS Log HPL/HPC/HPC+
TSMC 28nm CMOS RF HPL/HPC/HPC+
TSMC 16nm CMOS Logic FinFET Compact

UMC L180 Logic GII, MM/RF
UMC L180 EFLASH Log GII
UMC CIS18 – CONV diode
UMC CIS18 – ULTRA diode
UMC L130 Log/MM/RF
UMC L110AE Log/MM/RF
UMC L65N Log/MM/RF (SP)
UMC L65N Log/MM/RF (LL)
UMC 40N Log/MM – LP
UMC 28N Log/MM – HPC

X-FAB XH035 0.35µm HV
X-FAB XH018 0.18µm HV NVM E-Flash
X-FAB XT018 0.18µm HV SOI
X-FAB XS018 0.18µm OPTO
X-FAB XP018 0.18 µm NVM
X-FAB XR013 0.13µm RF-CMOS
X-FAB XMB10 MEMS

AMF Si-Photonics

CEA-LETI Si-Photonics Si310-PHMP2M
CEA-LETI MAD200 130nm NVM
OPEN 3D post-process for 3D integration

imec GaN-IC on SOI
imec Si-Photonics Passives+
imec Si-Photonics ISiPP50G
imec SiN-Photonics BioPIX 300
imec SiN-Photonics BioPIX 150

MEMSCAP PolyMUMPS
MEMSCAP SOIMUMPS
MEMSCAP PiezoMUMPS

MULTI-LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi-Level Mask (MLM). With this technique the available mask area (20mm x 20mm field) is typically divided in four quadrants (4L/R : four layers per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is thus reduced by a factor of four. By adapting the lithographical procedure, it is possible to use one mask four times for the different layers by using the appropriate quadrants. Using this technique, the mask costs can be reduced by approximately 60%.

The advantages of using MLM single user runs are:

- lower mask costs
- an MLM run is organized for one customer
- it can be scheduled for any date since it does not depend on regular MPW runs
- a customer receives a few wafers, resulting in a few hundreds of prototypes

The MLM technique is preferred over MPW runs when the chip area becomes large and when the customer would like to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.

MLM runs are only available for technologies from GLOBALFOUNDRIES, IHP, ON Semiconductor, TSMC and X-FAB.

PACKAGING AND SYSTEM INTEGRATION

Standardly, EUROPRACTICE delivers unpackaged untested prototypes. However, EUROPRACTICE offers a low-cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of packages are available ranging from DILs to PGAs and QFNs.

Side by side with world class partners and our long-term agreements, EUROPRACTICE boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.

In addition, photonics packaging is offered which is serviced by Tyndall. The photonics ecosystem continues to gather momentum attracting new users (both from academia and from industry) and increasing the technical scope of the photonics offering via EUROPRACTICE. Finally, various wafer-level packaging technologies are offered through CEA-Leti and Fraunhofer IZM channels, ranging from 3D frontside micro-bumping to 3D backside TSV, RDL and bumping.

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FROM PROTOTYPES TO VOLUME PRODUCTION

After successful ASIC prototyping, the EUROPRACTICE partners (in particular CMP, Fraunhofer IIS and imec) can also provide the customer access to the full production and qualification stage (from low to mid-high volumes).

PROTOTYPE FABRICATION

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. EUROPRACTICE takes care of the production for the first prototypes of the customer and organizes the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program. The test can be performed on both wafer level and on packaged devices. The goal is to reduce the test time and to examine the ASIC for manufacturing problems using the ATPG (Automatic Test Pattern Generation) and functional patterns. EUROPRACTICE supports you during the development of single-site test solution as well as with a multi-site test solution when high-volume testing is required. Based on the test strategy, different solutions can be implemented.

DEBUG AND CHARACTERIZATION

Before going into production, a characterization test program checks if all the ASIC specifications meet the customer's expectations. Threshold values are defined for each tested parameter. The software tests all the IP blocks and the results are verified with the bench test results. A characterization at Low (LT), Room (RT) and High (HT) temperature is performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be strong against process variations, the product qualification can start. EUROPRACTICE can support you through the full qualification process using different kind of qualification flows, including Automotive, Consumer, Industrial, Medical, Space, Military, Jedec and ESCC standards.

In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

YIELD IMPROVEMENT

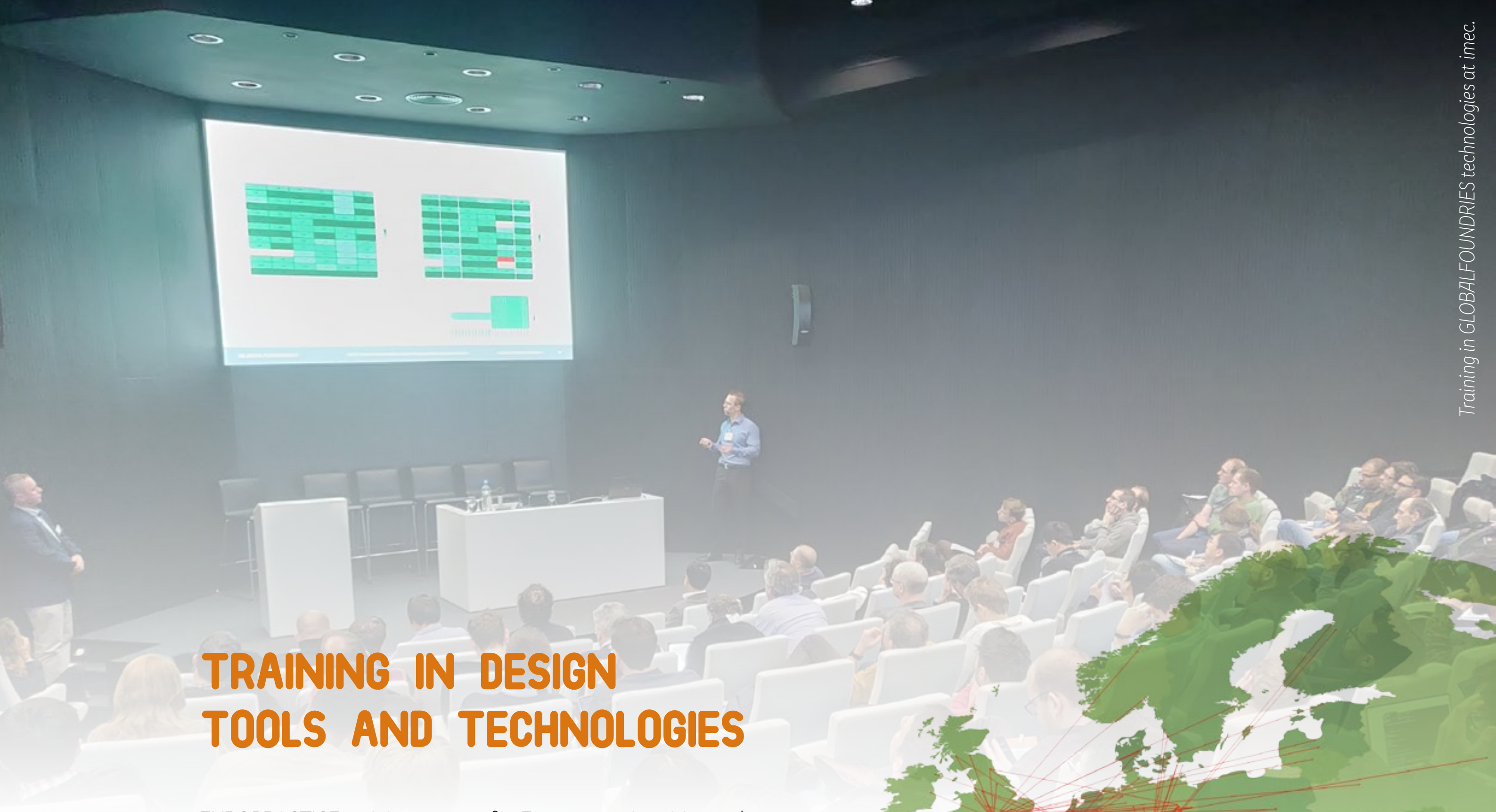
EUROPRACTICE can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the characterization and qualification of the device on corner lots, EUROPRACTICE can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers are analyzed to check for yield issues related to assembly or wafer production. EUROPRACTICE is using the well proven tool Examinator™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.

SUPPLY CHAIN MANAGEMENT

EUROPRACTICE is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.
Customer products are treated internally as projects and followed closely by the imec engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. EUROPRACTICE therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

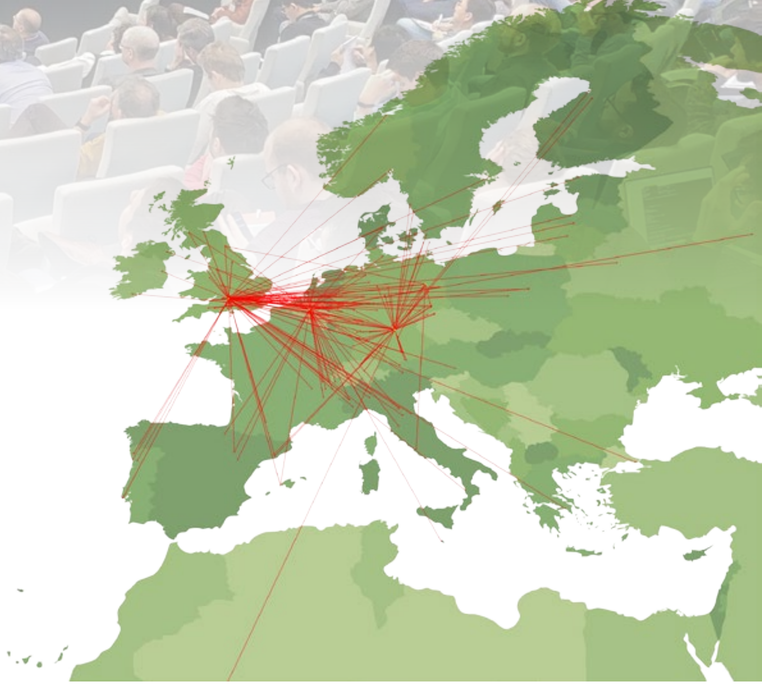
The most relevant companies involved in our semiconductor supply chain are listed below:

- **Foundry partners:** ams, EM Microelectronic, GLOBALFOUNDRIES, IHP, ON Semiconductor, STMicroelectronics, TSMC, UMC, X-FAB; AMF, CEA-LETI, imec and MEMSCAP.
- **Ceramic assembly partners:** Alter Technology (former Optocap), Kyocera, SERMA Microelectronics (former HCM).
- **Plastic assembly partners:** Amkor Technology, ASE, Greatek Electronics, Integra Technologies, Kyocera, StatsChipPac.
- **Wafer bumping partner:** ASE, FlipChip International, Pactech.
- **Si-Photonics packaging:** Alter Technology (former Optocap), PIXAPP (medium-volume/standard), Tyndall (low-volume/non-standard).
- **Test partners:** Aptasic, ASE, Bluetest, Delta, Microtest, RoodMicrotec.
- **Failure analysis:** Maser Engineering, RoodMicrotec.
- **Library partners:** Aragio, ARM, Cadence, eMemory, Faraday, INVECAS, Synopsys.



Training in GLOBALFOUNDRIES technologies at imec.

TRAINING IN DESIGN TOOLS AND TECHNOLOGIES



EUROPRACTICE training courses for European universities and Research Institutes are primarily aimed at academic staff and PhD students. Unlike training courses which address single topics or individual design tools, the EUROPRACTICE training courses address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow. Since the courses are based on the EUROPRACTICE EDA/CAD tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the EUROPRACTICE services/ infrastructure in their innovation, research and training.
Courses include a strong element of practical sessions where participants have an opportunity to extensively practice the concepts described in lectures and have access to experts who can answer questions about the concepts, design tools or technology process discussed on the course. Where it is known that a design flow is well supported by multiple vendors and/or processes, multiple course variants are offered that reflect the design tool / processes installed base.

New training courses will be added covering new design tools, new design flows, new nanoelectronic component technologies and smart system integration strategies. Courses will be offered at various "levels" ranging from introductory to advanced suitable for a wide range of attendees. Formal training courses will be augmented with a webinar series developed by EUROPRACTICE to ensure that training can be accessed easily by the widest possible audience.

During 2019 a total of 330 delegates (32 Lecturers, 163 Postgraduate students, 135 Researchers) attended 29 training courses organized by the EUROPRACTICE partners at 5 locations. The delegates came from 148 EUROPRACTICE Member Institutions in 25 countries.

Since EUROPRACTICE Training courses began in April 2014, a total of 1200 delegates from 290 Member Institutes in 37 countries have attended 104 training courses making 3310 days of practical training.

WEBINARS

A series of webinars on topics related to the rapidly maturing area of Advanced Packaging has been launched. The first webinar of this series was delivered in December 2019 and comprised two introductory talks. 92 delegates registered to join the live stream of webinar with a further 278 unique views accessing a recording of the webinar by the end of 2019

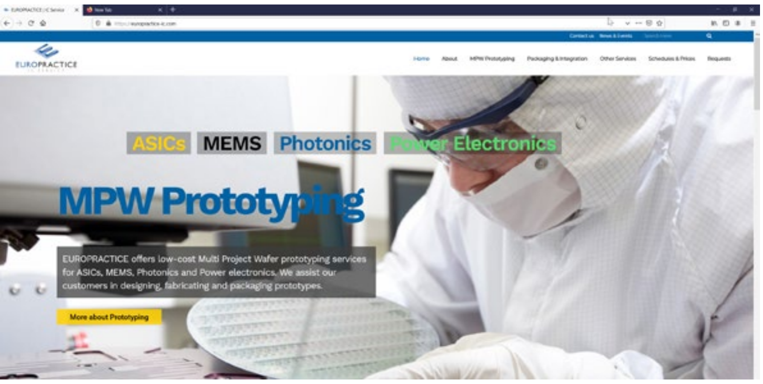
OUTREACH AND COMMUNICATION

In 2019, EUROPRACTICE has undertaken a major brand refresh to make the service more visible and provide customers with updated information more effectively. In order to do this, the EUROPRACTICE-IC website was relaunched, a EUROPRACTICE LinkedIn account has been created and exhibition materials have been redesigned.

WEBSITES

The current EUROPRACTICE service is operating two websites that present different parts of its offer.

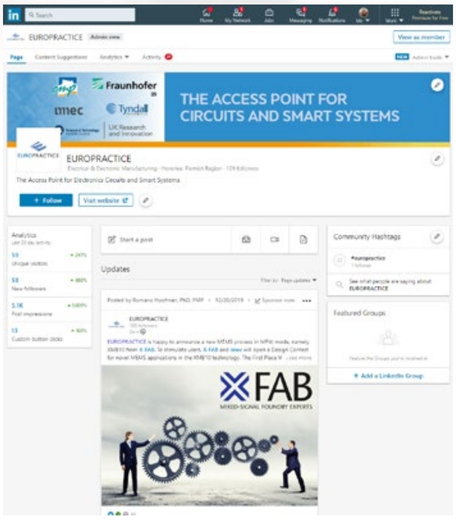
- https://www.europractice-ic.com : In June 2019, a new website was launched for the EUROPRACTICE-IC service, mainly dedicated to MPW prototyping and fabrication. Hosted by imec, it gives a clear overview of the EUROPRACTICE technology portfolio, packaging offer, system integration solutions, volume production and test services. Being constantly updated and including sections like News and Events, the new website makes it easier for customers to follow any changes regarding the EUROPRACTICE-IC service. On the website, customers can also register their design and find information on the MPW run schedules and current pricelists.



- www.europractice.stfc.ac.uk : This design tool website is hosted and maintained by UKRI-STFC. It is updated at least twice per week by UKRI-STFC and contains all the latest information about the design tools, training courses and related events.

SOCIAL MEDIA

To get in direct contact with the customers, EUROPRACTICE has created an account on LinkedIn. Although it has been opened very recently, the account has already more than 100 followers. The LinkedIn page presents information on EUROPRACTICE news and events in a less formal way. It also allows to receive immediate feedback form various stakeholders.



PROMOTIONAL VIDEO

Both the LinkedIn profile and the websites contain a new promotional video based on a series of short interviews with the partners, providers and customers. In the video, the partners introduce EUROPRACTICE, describe its offer and the scope of the services it provides. Moreover, the video gives an interesting opportunity to hear actual customers' testimonials about working with EUROPRACTICE.

New design of the EUROPRACTICE technology flyers.

EXHIBITIONS, CONFERENCES AND FAIRS

EUROPRACTICE is present at various scientific conferences, industrial trade shows and fairs in order to present its services to the existing customers and to attract the new ones. Typically, this is done by means of an exhibition booth, roll-ups, flyers and/or presentations.

Over the past year, all these exhibition materials were refreshed: Both the design and the content were redefined. The new uniformed style uses the traditional EUROPRACTICE colors to boost brand recognition. The new content focuses not only on the up-to-date description of the EUROPRACTICE offer, but also underlines the benefits of working with EUROPRACTICE and using services of a particular foundry.

In addition, two separate booklets have been produced and distributed during various events: One describing the Design Tools and Programmable Platforms, the other describing the training courses.

In 2020, EUROPRACTICE will be present at least at the following events:

MEMS 2020	Vancouver, Canada	18-22 January
ISSCC 2020	San Francisco, US	16-20 February
DATE 2020	Grenoble, France	9-13 March
DAC 2020	San Francisco, US	19-23 July
PRIME 2020	Erfurt, Germany	20-23 July
ESSDERC / ESSCIRC2020	Grenoble, France	14-18 September
IEEE SENSORS 2020	Rotterdam, the Netherlands	25-28 October
EFECS 2020	Berlin, Germany	24-26 November

EUROPRACTICE national seminar in London.

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NATIONAL SEMINARS

In 2019, EUROPRACTICE has continued organizing national or regional seminars, where academic and industrial customers can meet and exchange learnings with each other and other stakeholders. Typically, the program is one-day. The morning part consists of plenary sessions in which EUROPRACTICE presents its current offering and its projected roadmap together with the highlights of user projects (preferably focusing on collaboration between academia and local industry). The afternoon session is more interactive consisting of an open-market place where users can share their results with each other by means of posters and presentations.

Last year, four national seminars were organized, namely in Zürich (Switzerland), Munich (Germany), Cork (Ireland) and London (the UK).

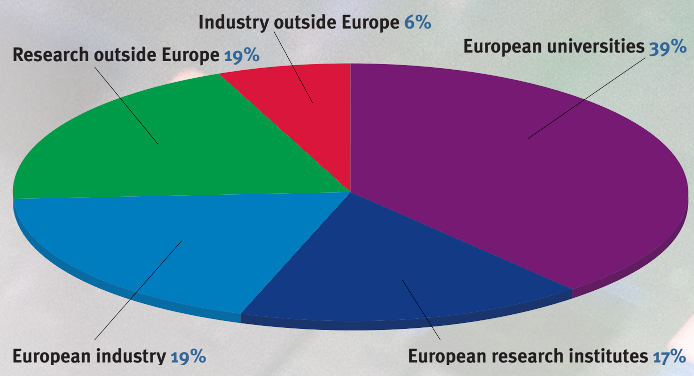
For 2020, at least 4 national seminars are planned in the Nordic region, Benelux, France and in the Balkan region.

EUROPRACTICE national seminar organized in cooperation with MIDAS Ireland in Cork.

RESULTS 2019

NUMBER OF PROTOTYPED CIRCUITS ON MPW RUNS

In 2019, a total of 884 submitted designs have been prototyped on EUROPRACTICE MPW runs. This number is much higher than for previous years, since it includes MPW prototypes in TSMC technologies and all prototypes from MPW runs organized by CMP. Therefore, any comparison with previous years will be difficult.



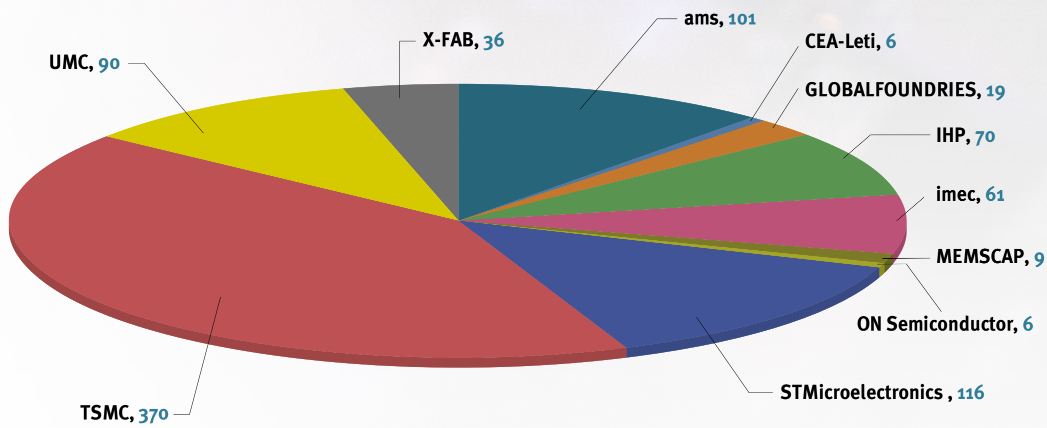
MPW designs in 2019

56% of the prototypes were designed by European universities and research institutes, while 19% of the designs are coming from European industry (mainly SMEs). The remaining 25% of the designs is coming from outside Europe, namely 19% from academic institutions and 6% from industry.

TECHNOLOGIES OF THE WORLD-LEADING FOUNDRIES

EUROPRACTICE provides access to the technologies of the world-leading foundries, such as ams, GLOBALFOUNDRIES, ON Semiconductors, STMicroelectronics, TSMC, UMC and X-FAB, complemented by specialty fabs at CEA-Leti, IHP, imec and MEMSCAP. Most of the submitted designs in 2019 were fabricated in TSMC, which is also the leading foundry for the global industry.

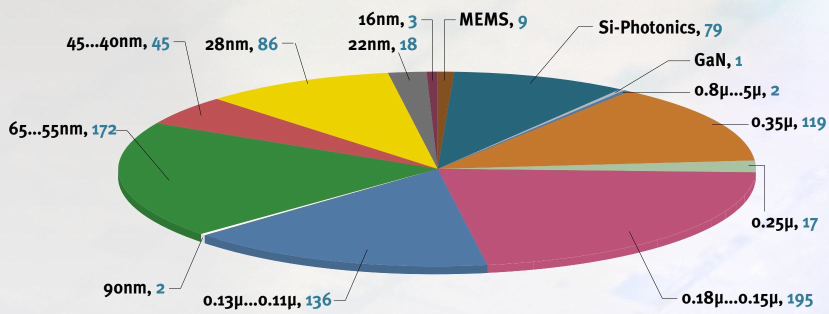
Notably, two of the European foundries, STMicroelectronics and ams, have the second and third largest number of designs realized. One of the other European foundries, X-FAB, has increased its number of fabricated designs again as compared to last year(s).



Number of fabricated designs in 2019 per foundry

A GOOD TECHNOLOGY AND GEOMETRY MIX

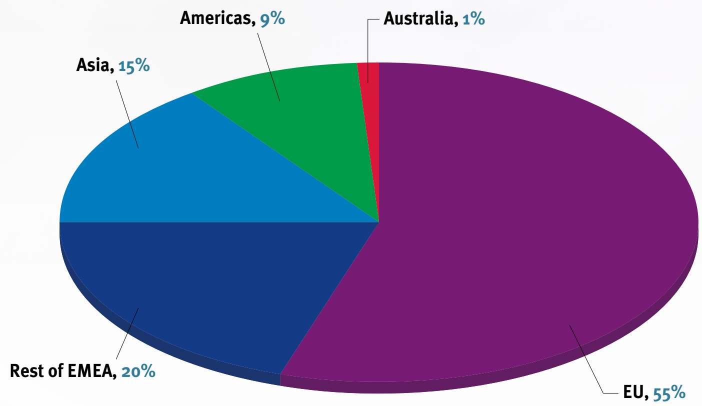
EUROPRACTICE offers a good technology mix for its customers. In 2019, advanced technologies, older technology nodes and More-than-Moore technologies have all been used in significant volume by the EUROPRACTICE customers. The older technology nodes (ranging from 0.11µm to 0.7µm) are still very popular and represent approximately half of the total designs which have been fabricated. For the more advanced nodes, 65nm and associated nodes (i.e. 55nm) are the most popular with 172 fabricated designs. In addition, the 28nm technology node has been used very frequently with an almost equal share in ST28FDSOI (42 designs) and TSMC28 (44 designs). 18 designs in total were fabricated in 22nm technologies. The 22nm FDSOI technology from GLOBALFOUNDRIES has tripled its number of designs – going from 5 last year to 15 this year. Moreover, the 16nm FinFET technology from TSMC has been added to the portfolio in 2019, representing 3 early prototypes. The popularity of Silicon Photonics and MEMS has been confirmed in 2019 by the high number of designs in the imec Si-Photonics technologies (namely 60 designs in total). Finally, a first design has been fabricated in the GaN-IC technology, which is also a newcomer to the EUROPRACTICE technology portfolio.



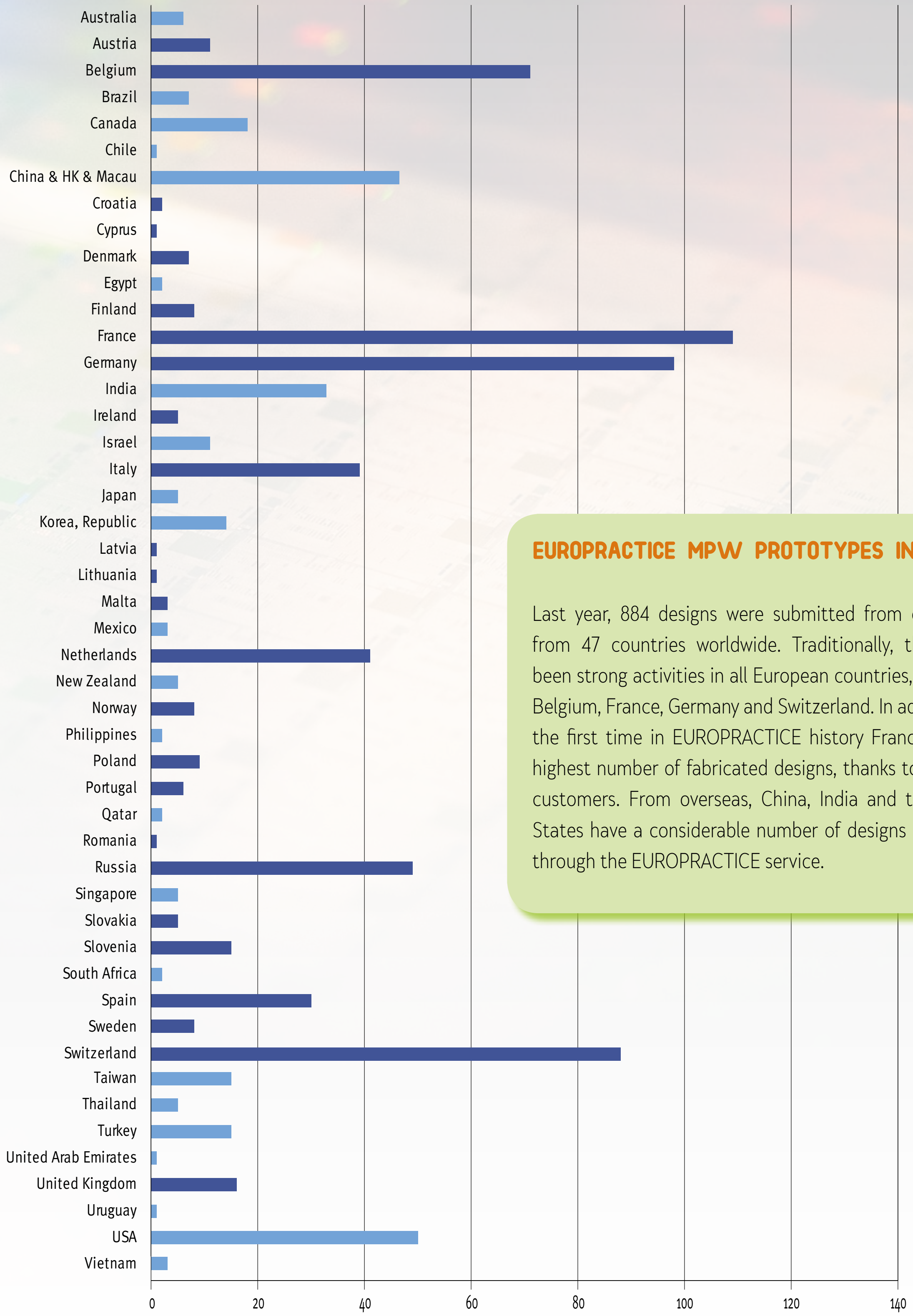
Number of fabricated designs in 2019 per technology (node)

GEOGRAPHICAL DISTRIBUTION

Although EUROPRACTICE focuses mainly on European customers, its service and technologies are also accessible outside Europe. 55% of the fabricated designs are coming from inside the European Union and another 20% from other countries in the EMEA (Europe, Middle East and Africa) zone. More and more customers from Asia are using the EUROPRACTICE prototyping services – representing a total volume of 128 designs in 2019. Finally, the remaining 10% of the designs fabricated are coming from the Americas and the Australian continent.



Geographical distribution of MPW designs in 2019



EUROPRACTICE MPW PROTOTYPES IN 2019

Last year, 884 designs were submitted from customers from 47 countries worldwide. Traditionally, there have been strong activities in all European countries, especially Belgium, France, Germany and Switzerland. In addition, for the first time in EUROPRACTICE history France has the highest number of fabricated designs, thanks to the CMP customers. From overseas, China, India and the United States have a considerable number of designs submitted through the EUROPRACTICE service.

VERITAS 2.2: A low-noise, source-follower and drain current read-out integrated circuit for the Wide Field Imager on the Athena X-ray satellite

Max Planck Institute for extraterrestrial Physics, Garching, Germany

Contact: Dr. Norbert Meidinger
E-mail: nom@mpe.mpg.de
Technology: ams 0.35µm HV CMOS C35B4C2
Die size: 7100µm x 4600µm
Design Tools: Cadence IC v6.1.5 and Mentor

Description

VERITAS 2.2 is an evolutionary step of the VERITAS read-out integrated circuit (ROIC) architecture designed for high-speed, low-noise DEPFET (Depleted Field Effect Transistor) source follower or drain read-out for the Wide Field Imager on the Athena X-ray satellite. Drain read-out, also known as current read-out, mitigates the RC time of the classical source follower read-out. This is particularly beneficial for large DEPFET detectors where the line capacitance is large, with the current measured at the drain of the DEPFET transistor providing an immediate signal proportional to the collected charge in the pixel. VERITAS 2.2 is designed to address the implementation challenges of drain read-out and deliver consistent performance at short processing time (2.5µs) with a system noise better than 3 e-.

The VERITAS 2.2 Application Specific Integrated Circuit (ASIC) is composed of 64 analog read-out channels to process in parallel the signals coming from 64 pnCCD outputs or 64 DEPFET transistors. The architecture in VERITAS 2 implements for the first time both source follower and current drain read-out modes of the DEPFET sensors. In contrast to the previous versions of VERITAS, and its predecessor ASTEROID, the VERITAS 2 analog signal processing is based on a fully differential architecture. This results in a larger dynamic range at the amplifier outputs, which in turn allows for higher gains and therefore better noise performance. The fully differential topology is intrinsically less sensitive to noise from the power supply and cross-talk. Fig. 1 shows the layout of the ASIC. The chip is 7.1mm x 4.6mm with a channel pitch of 75µm. Every channel consists of two detector input stages: one for source follower voltage read-out, one for drain current read-out; a signal amplifier; a dual slope integrator as filter and a sample and hold stage. The 64 analog outputs are multiplexed to a fully differential output buffer capable of a pixel rate of 40 Mpix/sec. The chip also includes a dedicated test and debugging network to enable an in-situ test and debugging capability.

The main advantage of the drain read-out is that all the nodes of the DEPFET are at a fixed potential. Therefore, the read-out speed of the system is not limited by the RC time constant given by the 1/gm of the device and the total input capacitance of the read-out electronics. This comprises the input capacitance of the preamplifier and the parasitic capacitance associated to the DEPFET source line. This time constant can be particularly high in case of large DEPFET arrays due to the relative low gm (~100µS) of the DEPFET on one side and the big line capacitance on the other side. In fact, in the case of the DEPFET matrices, all the sources of the DEPFETs in one column are connected to one single metal line and therefore the capacitance, depending on the sensor size, can be as high as 40pF.

Why EUROPRACTICE?

EUROPRACTICE offers affordable access to chip design technology including state-of-the-art software tooling and MPW production. We use the Cadence and Mentor tools provided by EUROPRACTICE for the chip design flow from design and analysis to verification. The EUROPRACTICE staff at Fraunhofer provides excellent technical support for the chip submission and all questions related to the technology. Max-Planck-Institute for extraterrestrial Physics has worked with EUROPRACTICE for many years and we are grateful for the good collaboration with Fraunhofer and UKRI-STFC at the Microelectronics Support Center.

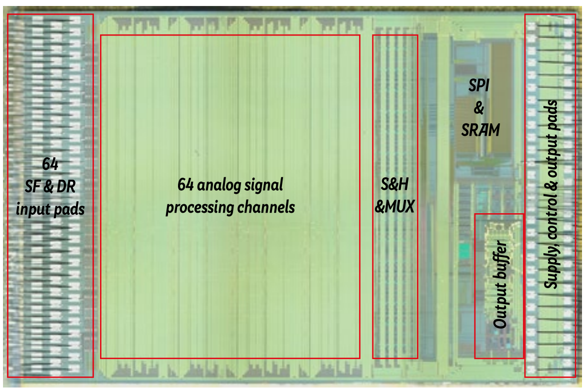


Fig.1: Microscope picture of VERITAS 2.2.

CMOS image sensor with two-tap pixel-wise coded exposure for compressive sensing

University of British Columbia, Vancouver, B.C., Canada

Contacts: Yi Luo, Shahriar Mirabbasi
E-mails: luoyikey@ece.ubc.ca, shahriar@ece.ubc.ca

Technology: ams 0.35µm CMOS Opto
Die size: 3925µm x 4025µm

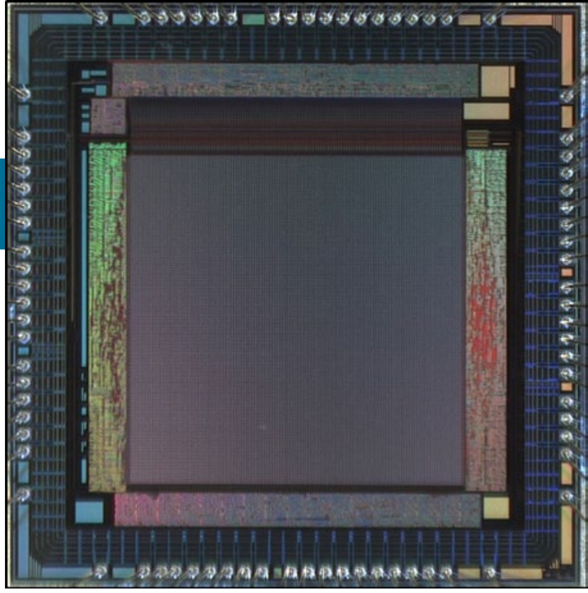


Fig.1: Picture of the fabricated die.

Introduction

Compressive sensing (CS) is one of widely applied theories in computational imaging paradigms. Currently, pixel-wise coded exposure is developed to demonstrate CS for types of applications such as high-speed imaging and high-dynamic range (HDR) imaging. Due to on-chip per-pixel exposure switching is not available on most image sensors, pixel-wise coded exposure is usually realized by discrete spatial-light modulators (SLMs) which make cameras suffer from bulky sizes and high-power consumption. In this project, the designed CMOS image sensor is intended to implement on-sensor pixel-wise coded exposure. With a conventional camera packaging, CS applications are naturally extended to sensor nodes in a single frame period. In comparison to the state-of-the-art, the proposed on-sensor CS solution provides improved light throughput and in lower power consumption.

Description

The proposed CMOS image sensor consists of variety of functional blocks. The row decoder block performs row-by-row scanning to provide reset, charge transfer, and read-out signals to the pixel array. The DRAM controller is a row scanner which sequentially selects a row of pixels to enable their exposure codes refreshment. During sensor read-out periods, the pixel array is read out using a correlated double-sampling (CDS) scheme realized by column-based CDS circuits. Before reaching to a column scanner to output the final image data, pixel output signals are digitized to corresponding digital format through an analog-to-digital convertor (ADC) placed in each column. The fabricated image sensor chip contains 192×192 pixels with a pixel pitch size of 17.2µm and a fill factor of 35.2%. The chip is powered by two separately regulated 3.3V power sources – one supplies for analog circuits and the other for all digital control modules.

In a dark environment, the pixel dark current is measured as 1.36 fA. The lowest achievable detection limit of a pixel is 10.8 nW/cm^2. By calculating the mean of the standard deviation of all pixel outputs, the extracted pixel and column fixed-pattern noise (FPN) are 0.19% and 0.26%, respectively. The prototype camera equipped with the proposed CMOS image sensor experimentally demonstrated single- frame pixel-wise coded exposure in both spatial and temporal domains. Operate at 10fps, the image sensor is exposed to scene for long period and improves SNR in recovered images. In each frame, as pixel readout is not required until coded exposure is accomplished, CS are naturally applied during the exposure period and the image sensor follows a conventional reset-exposure-readout operation flow.

Why EUROPRACTICE?

We appreciate the EUROPRACTICE services, which allow affordable access and reasonable prices to leading-edge IC technologies, frequent MPW-fabrication runs, CAD tools and packaging services. A research project such as this would simply not be possible without the services EUROPRACTICE provides.

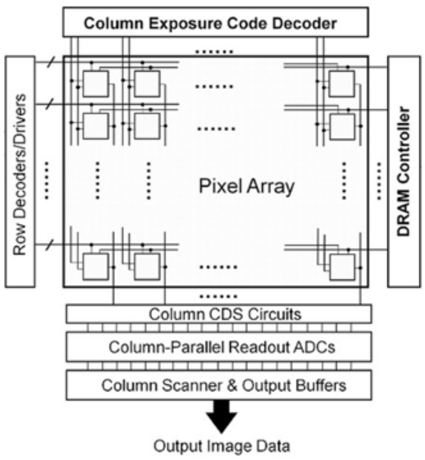


Fig.2: Architectural topology of the image sensor.

Transceiver ASIC in ams H35 process for 3D ultrasound computer tomography

KIT ASIC and Detector Laboratory, Karlsruhe Institute of Technology, Eggenstein-Leopoldshafen, Germany

Contact: Prof. Ivan Peric
E-mail: ivan.peric@kit.edu
Technology: ams 0.35µm HV CMOS H35B4D3 4M
Die size: 4mm x 4mm
Design tool: Cadence IC v6.1.6

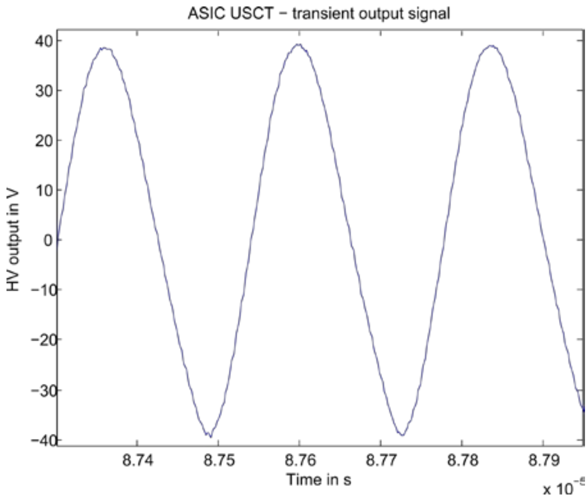


Fig.1: Output of the high-voltage amplifier, amplitude of 90V was achieved.

Description

3D Ultrasound Computer Tomography (USCT) is a novel method for early detection of breast cancer. The 3D USCT device contains about 2000 ultrasound transceivers placed in a half spherical reservoir filled with water. The transducers are grouped in groups with 18 devices, each group is driven and readout with two USCT9C ASICs that we developed in H35 ams process.

Every ASIC contains nine high-voltage analogue drivers and three low-noise receivers. The high-voltage driver has a gain of 40 and can generate output signals with amplitude of 120V. The bandwidth of the amplifier is about 5MHz. The receiver is implemented as a three-stage amplifier; every stage is a voltage amplifier with RC feedback that uses a single ended inverting amplifier as the active element. The feedback can be configured in the way to provide wideband (0.1 – 5MHz) and narrowband (around 3.5MHz) amplification. Frequencies and amplification can be varied. Simulated input referred noise is less than 10µV.

The measurement results are promising, the USCT9C ASIC fulfils the requirements for 3D USCT. The high-voltage amplifier was used to amplify a chirp signal. The output amplitude of 90V was achieved as shown in Figure 1. Receiver has been used to amplify signals with a gain of 3000. Figure 2 shows the photograph of the bonded USCT9C ASIC.

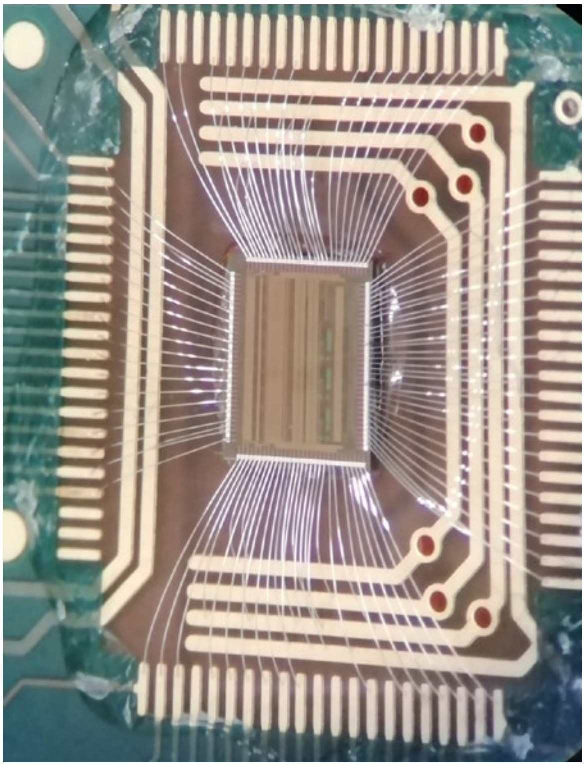


Fig.2: Photograph of the bonded USCT9C ASIC.

Why EUROPRACTICE?

We have been working with EUROPRACTICE since 2004. Although it is sometimes possible to make direct contact with foundries, a long-term development would not be possible without help of EUROPRACTICE. EUROPRACTICE organizes regular MPW runs, provides design support. EUROPRACTICE offers access to chip design software (for instance, Cadence) and standard cell libraries. EUROPRACTICE offers the possibility that several academic partners share the engineering run costs. EUROPRACTICE establishes the link between foundries and customers.

Arnold: eFPGA implemented in an open source RISC-V micro-controller

ETH Zürich, Switzerland
in collaboration with QuickLogic Corporation

Contacts: Davide Pasquale Schiavone, Frank K. Gürkaynak
E-mails: pschiavo@iis.ee.ethz.ch, kgf@ee.ethz.ch
Technology: GLOBALFOUNDRIES 22nm FD-SOI 22FDX
Die size: 3mm x 3mm
Design tool: Cadence IC v6.1.6

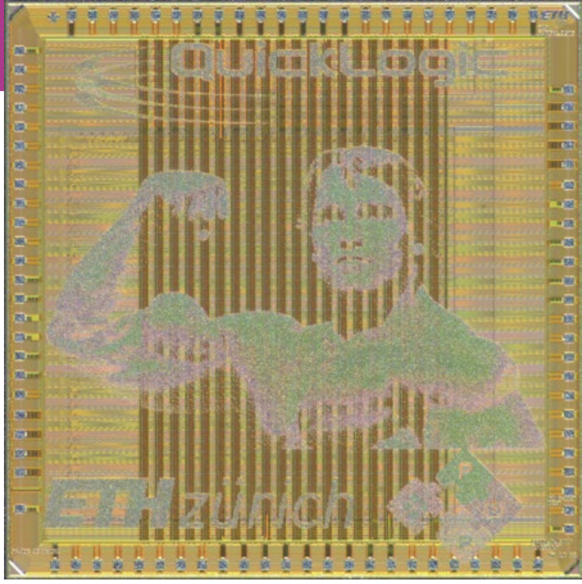


Fig.1: Micrograph of the Arnold Die. The logo is made by the fill pattern on the last level metal.

Description

Arnold is a RISC-V based 32-bit micro-controller based on the open source PULPissimo system part of the PULP project developed by ETH Zürich and University of Bologna. PULPissimo uses a 32-bit RISC-V core with custom extensions for DSP applications called RI5CY and has 512kByte on chip SRAM memory and a set of peripherals that can copy data to and from memory over a microDMA.

What makes Arnold special is that it also houses an embedded FPGA (eFPGA) by QuickLogic Corporation that is connected as an accelerator with direct access to the shared local memory, offering many interesting opportunities to accelerate operations on the microcontroller.

The eFPGA can be programmed through an APB bus interface by the RISC-V core. Communication between the processor and the eFPGA can go through a second APB bus when needed. But the real power of the system comes when the eFPGA connects to the Tightly Coupled Data Memory (TCDM) of PULPissimo using four configurable 32-bit ports, allowing the eFPGA to work on the same memory as the host processor directly (see Fig. 2).

The eFPGA has direct access to most of the I/O pins of Arnold over a configurable pin multiplexer. This allows the eFPGA to be used as a programmable peripheral in the system. Even more interesting is the operation mode that allows the eFPGA to be connected between the uDMA and peripherals, allowing it to be used as a programmable filter in incoming/outgoing data further enhancing the capabilities of the system.

Designed as a pure research chip (no commercial version is planned at the moment) with a close collaboration between QuickLogic Corporation and ETH Zürich, Arnold is a success story of open source hardware design. From the initial contact between QuickLogic representatives following a chance encounter at the GLOBALFOUNDRIES Technology Conference until the tape-out it took less than one year. This is in large part due to the permissive open source licensing scheme of the PULP platform (using the Solderpad license) and commitment by both partners.

The Chip has been tested and currently we are working on different demonstrator applications that highlights the various configurations of the eFPGA when working in concert with the PULPissimo system.

Why EUROPRACTICE?

ETH Zürich typically tapes out 10 to 20 ASICs per year, roughly half of those are for research projects, such as Arnold here. Our research concentrates on Energy Efficient Computing Architectures and to produce results that remain relevant, we need to have access to technologies with smaller feature sizes. EUROPRACTICE-IC service has been a very important partner for us to help us get access to GF22FDX. It is not only the access to the PDK but the support given throughout the submission process to ensure that we have ASICs that work properly.

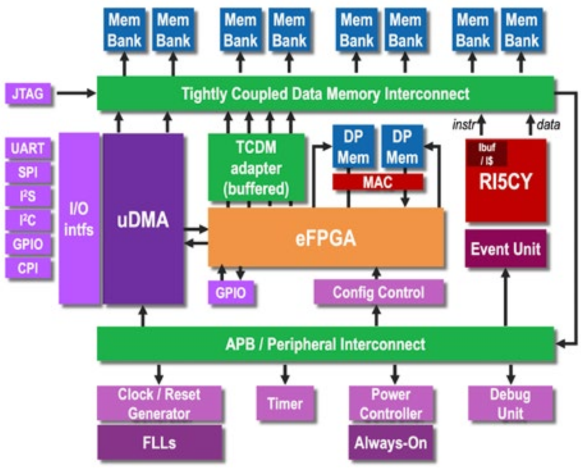


Fig.2: Block diagram of Arnold. In the actual implementation, the eFPGA shown in orange occupies most of the core area of the chip.

REFERENCE: A 4.3-GHz fractional-N PLL frequency synthesizer in GLOBALFOUNDRIES 22FDX

Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, München, Germany

Contact: Enno Böhme
E-mail: enno.boehme@emft.fraunhofer.de
Technology: GLOBALFOUNDRIES 22nm FD-SOI 22FDX
Design size: 1.27mm x 1.17mm
Design tool: Cadence

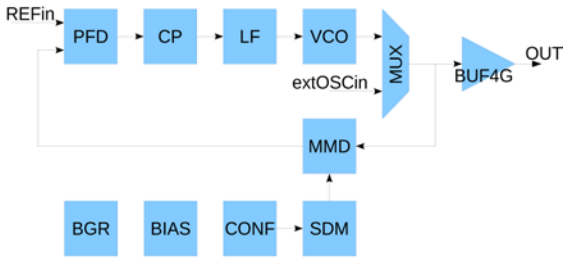


Fig.1: Block diagram of REFERENCE

Description

The REFERENCE (Rf Engineered substrates to FostER fEm performaNCE) project funded under ECSEL JU aimed to leverage a European leading-edge Radio Frequency (RF) ecosystem based on RF Silicon-On-Insulator (SOI) technology, which was perceived as the most promising to reach best trade-off for performance, cost and integration needs for RF Front End Modules (FEMs).

The project has developed innovative solutions from material, engineered substrates, process, design, metrology to system integration in order to address the challenging 4G+/5G requirements for RF FEMs.

The Fraunhofer EMFT focused on realizing mixed-signal building blocks for frequency synthesis IP, required by the specific transmitter and power amplifier for the future wireless avionics intra-communication (WAIC band from 4.2 to 4.4 GHz).

The focus of the IMS institute of the Universität der Bundeswehr München (UniBwM) was to develop the High-Level plan and RF requirements. Further, a voltage-controlled oscillator (VCO) block was designed using the specification to cover the WAIC spectrum.

After a successful first tapeout in 2018, this year Fraunhofer EMFT successfully integrated a complete fractional-N phased-locked loop (PLL) frequency synthesizer for 4.3 GHz in GLOBALFOUNDRIES' 22FDX (22nm) technology including the VCO from UniBwM. The objective was to also showcase the RF performance and integration possibilities in the 22FDX technology.

The PLL consists of a Voltage Controlled Oscillator (VCO), Phase Frequency Detector (PFD), charge-pump (CP), a 4 GHz multi-modulus frequency divider (MMD), third-order Sigma-Delta Modulator (SDM), RF output buffer and an external Low-pass Filter (LPF). As can be seen in the block diagram (Fig. 1), an RF multiplexer was also included to allow other frequency ranges and enabling testing and evaluation purposes.

The UBWM designed an 8.6 GHz VCO with a wide tuning range and a divide-by-2 prescaler to shift the signal in the desired frequency range. This architecture was chosen to achieve better phase noise performance at lower power consumption, minimize frequency pulling due to output buffer as well as reduce the area of the passive components of the VCO. They also designed the RF multiplexer.

All other blocks, including a bandgap reference und reference bias current generator, were designed by Fraunhofer EMFT.

The digital blocks, i.e. the MMD, the SDM and the configuration interface, were designed with the digital standard cell libraries from INVECAS using Cadence tools in the digital design flow.

The design is pad-limited and with pads and IO cells the size is 1270μm by 1170μm. As the top-level power routing and the fill structures hide most of the blocks, as the die photo shows (Fig. 2), the layout is shown without top-level power routing and filling (Fig. 3).

Papers giving measurement results for this tape-out are currently in preparation.

Why EUROPRACTICE?

EUROPRACTICE offers prototyping and testing for various technologies at affordable prices, including modern nanometer scale processes, such as GF22FDX, which was used in this project, as well as access to a wide portfolio of current EDA tools from various vendors for non-commercial use. They also provide excellent support for PDKs and tapeout procedures.

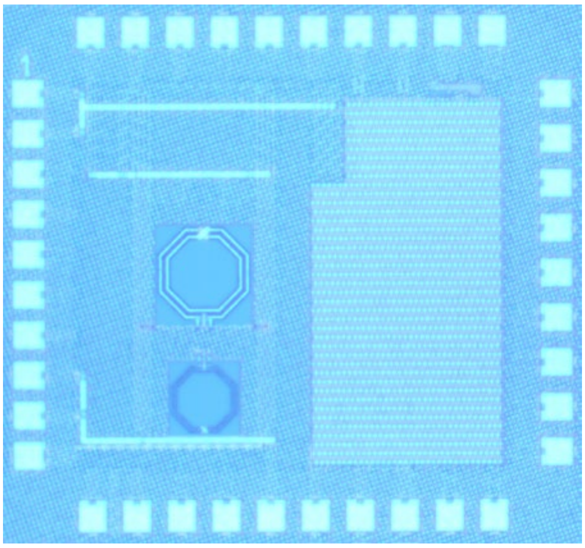


Fig.2: REFERENCE die photo

Without the help of EUROPRACTICE we would have been unable to achieve our results; those for the first silicon have already been published in several papers at IEEE conferences by UniBwM and Fraunhofer EMFT in 2019.

Acknowledgments

The project REFERENCE has received funding from the Electronic Component Systems for European Leadership Joint Undertaking under grant agreement No 692477. This Joint Undertaking receives support from the European Union's Horizon 2020 research and innovation program and France, Germany, Ireland, Portugal, Belgium.
The German funding is provided by BMBF under the funding number 16ESE0121 and 16ESE0123.

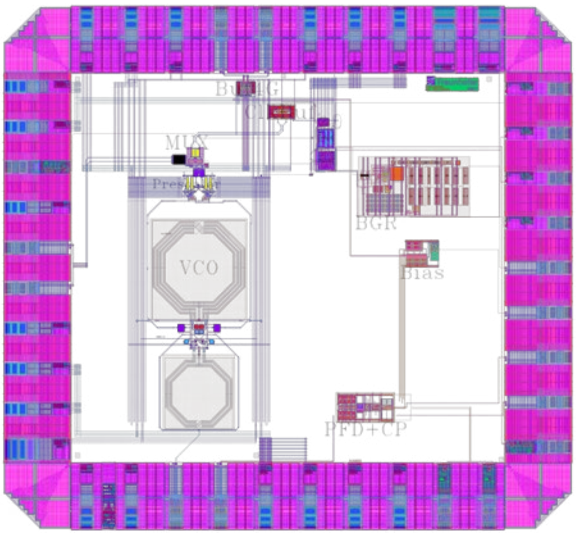


Fig.3: Layout of REFERENCE

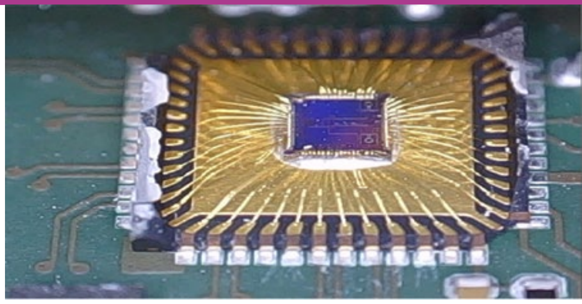


Fig.1: Packaged PASCAL on PCB.

PASCAL ASIC: A dual-channel multi-GNSS front-end ASIC

Department of Satellite Based Position Systems and Department of Integrated Circuits and Systems (ICS), Fraunhofer Institute for Integrated Circuits IIS, Nuremberg/Erlangen, Germany

Contacts: Alexander Rügamer, Dr. Frank Oehler
E-mails: alexander.ruegamer@iis.fraunhofer.de, frank.oehler@iis.fraunhofer.de
Technology: GLOBALFOUNDRIES 55nm LPe
Die size: 1800µm x 1900µm

Introduction

The modernized global navigation satellite systems (GNSS), such as GPS III, Galileo, GLONASS CMDA and BeiDou Phase 3, will considerably improve navigation performance with their mostly wideband signals on different frequency bands. Moreover, multi-band reception is mandatory in order to fulfil the more and more challenging requirements in accuracy, availability, robustness and integrity in both the mass-market and semi-professional GNSS receiver segments. Consequently, there is a strong interest in integrating configurable and wideband dual-band reception capabilities into low-power-optimized devices. In order to take advantage of the GNSS wideband signals, RF front ends have to provide a certain linearity and bandwidth taking into consideration a low increment in power consumption, group delay variation and higher sampling rates.

Description

PASCAL ASIC is a dual-channel RF front-end ASIC which enables simultaneous reception of two wideband frequencies in the GNSS L-band range. The integrated circuit includes two separate low-IF architectures. The front end was designed to achieve low power consumption and to reduce the front-end area of the whole receiver. One main benefit is the support of the full Galileo E1/E6 PRS reception with a very low number of external components. PASCAL does not require external IF filters and its two reception paths are independently configurable using an SPI interface. Moreover, PASCAL features a fully integrated loop filter.

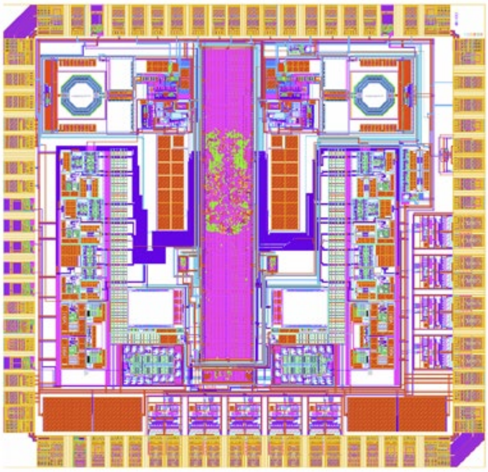


Fig.2: PASCAL layout snapshot.

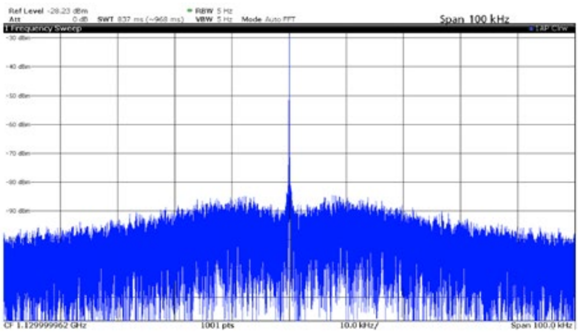
Each of the two channels require an external low-noise amplifier (LNA) and a preselection RF filter. The external LNA dominates the overall noise figure (NF); consequently, an overall receiver NF lower than 2 dB is feasible. The chip includes the analog-to-digital converters (ADCs) which are programmable from 1 to 4-bit resolution. The sampling frequency can be generated and configured internally or used from an external source. Multiple PASCAL chips can be combined in order to realize array-applications or more than two simultaneous reception bands.

Main benefits

PASCAL supports all L-Band GNSS signals and is a design for low-power consumption. Simultaneous and independent dual-band reception is possible together with configurable bandwidths and intermediate frequencies. Two Fractional-N Synthesizers with integrated VCOs support a wide range of LO frequencies. No external IF filters are required. PASCAL ASIC is prepared for Galileo E1/E6 PRS reception or other wideband signals like Galileo E5 AltBOC with more than 50 MHz bandwidth.

Why EUROPRACTICE?

EUROPRACTICE offers access to modern CMOS technologies. The participation on MPW runs is cost effective and allows realizing ASIC research projects with limited budget. Fraunhofer IIS has participated in many tapeouts via EUROPRACTICE. The huge variety of CMOS technologies and the frequent MPW runs are reasons to choose EUROPRACTICE services.

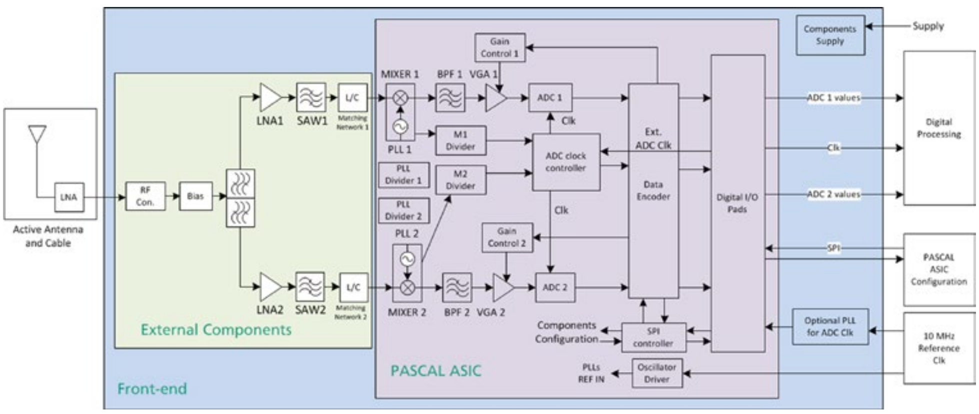


References

www.iis.fraunhofer.de/positioning

Fig. 3: Measurement of LO phase noise: Low Phase Noise -120.20 dBc/Hz @ 1 MHz for an internal 1230-MHz synthesizer LO signal.

Fig. 4: Block diagram.



IHP SG13G2-electronics for applications in quantum technologies

High-Frequency Electronics and Department of Physics, Paderborn University, Paderborn, Germany

Contacts: Alex Widhalm, Andreas Thiede, Artur Zrenner

E-mail: alex.widhalm@upb.de

Technology:
IHP 0.13µm SiGe BiCMOS SG13G2

Die size: 900µm x 720µm (mini@sic)

Introduction

Quantum technologies play an increasingly important role in today's world. Starting from sensing techniques and secure data transmission to simulations and quantum computers, all application areas are being discussed and researched today with great effort. In this context, quantum mechanical state control and state preparation play a central role. The state control can be performed utilizing coherent control. Until now, coherent control of single QDs (Quantum Dots) has been demonstrated by using purely optical ps laser fields. In our work, we apply a new coherent optoelectronic control protocol, where we are using a combination of optical ps laser fields and ps electrical fields (see Fig. 1). For this purpose, we have designed IHP SiGe BiCMOS-Technology based electronic chips, which deliver voltage transients in the ps-time domain and operate at cryogenic temperatures (liquid helium 4.2K).

Our protocol has the advantage that the population of the QD can be achieved with $\pi/2$ laser pulse pairs, which play the

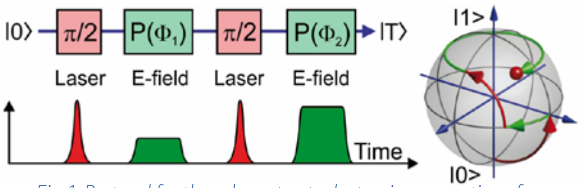


Fig. 1: Protocol for the coherent optoelectronic preparation of an arbitrary quantum state in an exciton qubit.

role of an invariant optical clock. Coherent state preparation for any target state |T> is completely controlled by phase manipulation via the electrical pulses $P(\Phi_1)$ and $P(\Phi_2)$. This seems advantageous in terms of the systems scalability.

Description

The system integration between the GaAs QD-photodiode chips and the SiGe electronic chips plays an important role. The SiGe BiCMOS chips were brought into close proximity to the QD-photodiode GaAs chip. The connection between the chips was performed by short distance wire bonding (see Fig. 2). In the first project phase, various chip design runs with SiGe-HBT as well as pure CMOS and BiCMOS were tested. It turned out that the current consumption of the HBT leads to a temperature increase and thus to a reduction of the coherence time of the QD. For these reasons, chips with CMOS technology were used for the coherent optoelectronic control experiments.

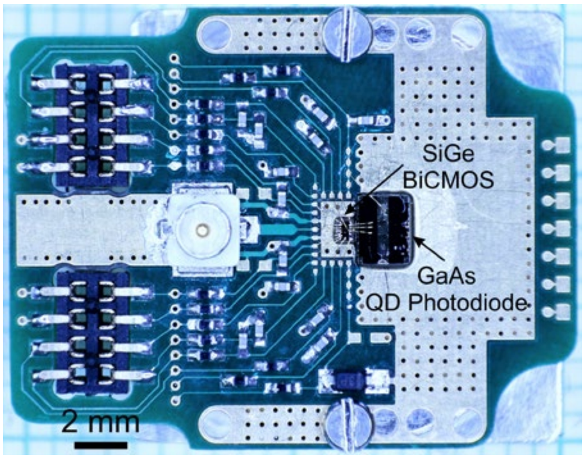


Fig. 2: Photograph of SiGe-chip connected to QD photodiode by wire bonding mounted on PCB with integrated electronic components.

Furthermore, the CMOS logic was used for pulse generation. Thereby various NOT gates, an inverter which is considered as delay-line, as well as NAND gate were used. A driver stage with cascaded MOSFETS is implemented at the end of the chip to significantly increase the current driver capability of the chip. The electronic chip generates an electric pulse with a voltage adjustable pulse width from 30 ps up to 3 ns.

In our Ramsey experiments (see Fig. 3), we have shown that the coherent phase of a single QD exciton can be controlled via the electric field manipulation up to values of within 100 ps. This is below the dephasing time of 300 ps of our QD exciton [1]. Our proposed protocol provides a scalable and universal approach for coherent state control.

Why EUROPRACTICE?

The department High-frequency Electronics of University Paderborn has been using EuroChip and EUROPRACTICE initiatives since its foundation in 1999. We have worked with OMMICs GaAs HEMT, STMicroelectronics CMOS and IHPs HBT technologies in numerous research projects. We appreciate the EUROPRACTICE services for providing access to leading edge IC technologies and CAD tools at reasonable prices. It is thus wonderfully suitable for academic institutions!

Acknowledgements

The German Research Foundation (DFG) is sincerely acknowledged for funding the project through the SFB TRR 142. Finally, we wish to thank IHP Frankfurt Oder for chip fabrication and the EUROPRACTICE initiative for providing access to this technology and the respective design tools.

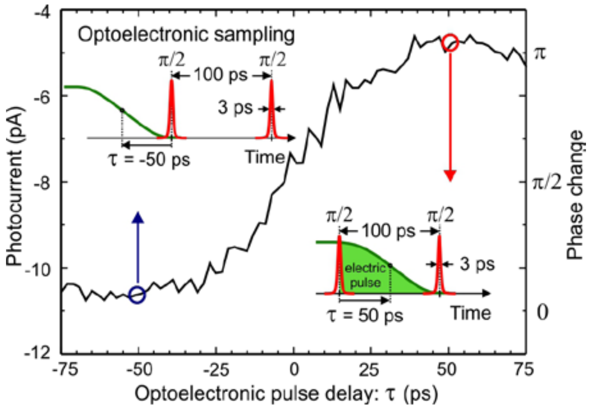


Fig. 3: Ramsey-based optoelectronic sampling of the applied electric pulse edge. A change of the optoelectronic pulse delay by 100 ps results in a π phase shift.

References

[1] Widhalm, A. et al. "Ultrafast electric phase control of a single exciton qubit" Appl. Phys. Lett. 112, 111105 (2018).

A W-band balanced power amplifier using broadside coupled strip-line coupler in SiGe Bi-CMOS 0.13-µm technology

School of Electrical and Data Engineering, Faculty of Engineering & IT, University of Technology Sydney, Sydney, New South Wales, Australia

Contact: Forest Xi Zhu
E-mail: xi.zhu@uts.edu.au
Technology: IHP 0.13µm SiGe BiCMOS SG13G2
Die size: 800µm x 800µm

Description

Load-variation insensitivity, for impedance matching between power amplifiers (PAs) and transmitting antennas, is a great design challenge for millimeter-wave wireless systems. To solve this issue, a balanced PA based on a compact quadrature coupler is presented to enhance the load-variation insensitivity and stability. The designed coupler utilizes a broadside-coupled strip line (BCSL) structure, which provides a truly broadband frequency response with minimized amplitude and phase imbalance. Using this coupler for a W-band balanced PA design, it achieves a high power-added efficiency (PAE) and a high saturated output power over a wide frequency bandwidth. The W-band balanced PA is implemented in a 0.13-µm SiGe Bi-CMOS process from IHP and achieves a measured saturation output power of 16.3 dBm and a peak PAE of 14.1% at 100 GHz (with 1.6-V power supply). The measured saturation power with 1-dB bandwidth is from 91 to 102 GHz. The measured results demonstrated the feasibility of compact quadrature coupler design and its application for PA design. The total chip area (with pads) is 0.64mm^2, where the size of the designed quadrature coupler area is only 0.04mm^2. This work has been published at IEEE Transactions on Circuits and Systems I: Regular Papers.

Why EUROPRACTICE?

The University of Technology Sydney has worked with EUROPRACTICE on IHP fabrication for a few years. We have benefitted from EUROPRACTICE'S excellent technical support for dummy fill and GDS submission. The EUROPRACTICE'S MPW service allows affordable access to state-of-the-art technology, such as the 0.13-µm SiGe Bi-CMOS technology used in this work.

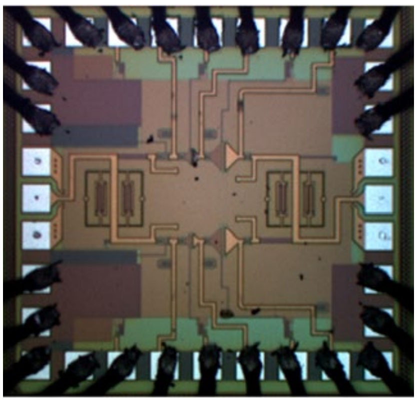


Fig.1: Micrograph of the fabricated chip.

Acknowledgement

The financial support of the Australian Research Council (ARC) Discovery Early Career Researcher Award (DECRA) under the grants DE160101032 is gratefully acknowledged.

Subharmonically pumped mixer for K-band mobile satellite communication systems

Tomsk State University of Control Systems and Radioelectronics (TUSUR), Tomsk, Russia

Contacts: Feodor Sheyerman, Andrey Kokolov, Alexey Pomazanov
E-mail: fish@tusur.ru
Technology: IHP 0.25µm SiGe:C SG25H3
Die size: 1.36mm x 1mm

Introduction

The development of radars and communication facilities based on transmit/receive modules (TRM) and active phased-array antennas (APAA) plays an important role in advanced microwave radioelectronic and telecommunication systems. In particular, the design of multi-channel TRMs and APAAs in the frequency range of 18..25 GHz (K-band) is a promising direction for various applications, such as fixed and mobile satellite communication systems and super-high resolution radars.

In order to achieve a high selectivity, the receiver front end (FE) is implemented using superheterodyne concept. When selecting a block diagram of the FE we should consider the possibility to provide required performances in a single-chip SiGe receiver; in addition, the chip area should be minimized. A promising approach to design FE is the use of active subharmonically pumped mixer (SM) based on the Gilbert cell [1] instead of passive mixer.

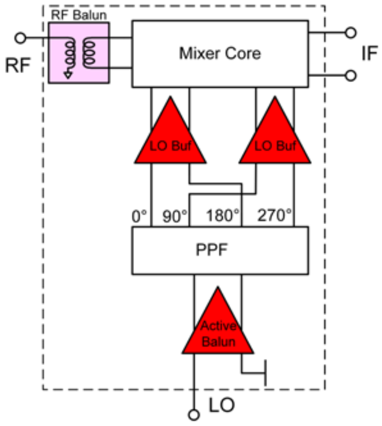


Fig.1: Block diagram of the mixer.

Description

The signal at the IF output of SM is produced as a result of mixing the input RF signal with the 2nd harmonic of the LO signal (8..10.5 GHz). The block diagram of the proposed mixer is presented in Fig. 1. The mixer consist of mixer core based on Gilbert cell, passive RF balun, active LO balun, polyphaser filter (PPF) and differential LO buffer amplifiers. The PPF is one of the important elements of SM, it is used to obtain quadrature components of the signal with the phase differences of 90° in the LO path. As the PPF is a passive device the LO buffer amplifiers compensate the losses in the LO path. The passive RF balun is used in the RF path, it is designed with the trade-off between the following performances: frequency bandwidth, insertion losses, layout area and amplitude-phase unbalance. A microscope photograph of the manufactured IC is shown in Fig. 2.

In 18..25 GHz RF frequency band SM provides conversion gain GC = -6..-9 dB at -10 dBm LO power, return losses at RF and IF ports better than -10 dB, RF-IF isolation of 30 dB, LO-RF isolation of 37 dB and LO-IF isolation of 35 dB. The 1-dB compression point for the input RF signal (IPRF_1dB) is -8 dBm. Die area of the SM is 1.36mm × 1mm including the pads. The advantages of the developed MMIC SM are small size, broadband performances and lower frequency band for LO signal.

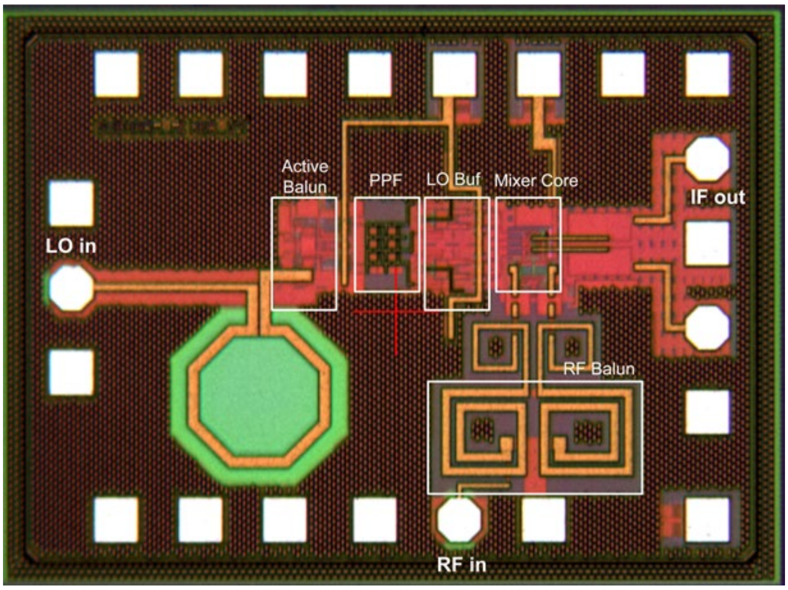


Fig.2: A microscope photograph of the IC bare die.

Why EUROPRACTICE?

The EUROPRACTICE service is almost the only opportunity for our university to gain access to state-of-the-art integrated circuit fabrication processes. This allows us to carry out scientific research at sophisticated level and affordable price. Thanks to this program, students, Ph.D. students and university staff get acquainted with modern CAD systems, design kits and technology processes and we have the opportunity to introduce our ideas into real products.

The EUROPRACTICE staff at the Fraunhofer Institute provides excellent support and help in our work.

Acknowledgements

This work was funded by Ministry of Science and Higher Education of the Russian Federation. Unique identifier is 8.3423.2017/4.6. Experimental results were obtained with help of "Impulse" centre under the project RFMEFI62119X0029.

References

[1] L. I. Babak, A. A. Kokolov, F. I. Sheyerman and A. V. Pomazanov, "Design of MMIC Subharmonic Mixer for K-band Receiver Based on 0.25 μm SiGe BiCMOS Technology," 2019 International Siberian Conference on Control and Communications (SIBCON), Tomsk, Russia, 2019, pp. 1-4.

STMicroelectronics 28FDSOI

PSCALE_C: A near/sub-threshold RISC-V micro-processor

Department of Electrical Engineering (ESAT), Microelectronics and Sensors (MICAS), KULeuven, Leuven, Belgium

Contacts: Roel Uytterhoeven, Wim Dehaene
E-mails: roel.uytterhoeven@esat.kuleuven.be, wim.dehaene@esat.kuleuven.be
Technology: ST 28nm FD-SOI CMOS
Die size: 1496µm x 1511µm

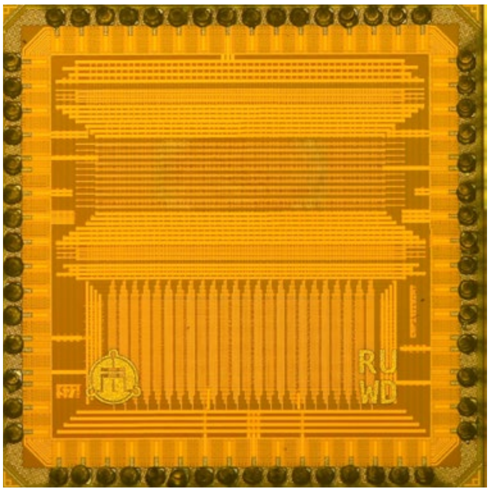


Fig.1: Photograph of the fabricated die.

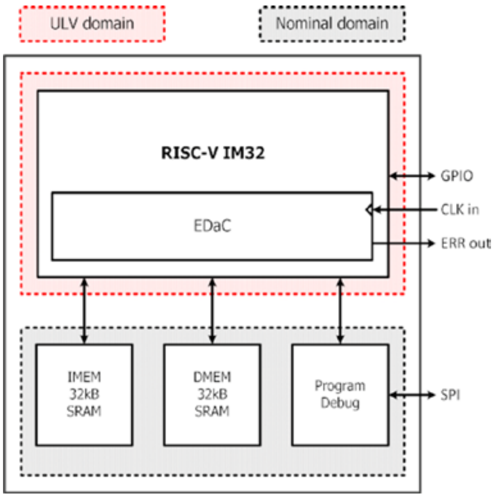


Fig.2: Circuit diagram.

Introduction

The PSCALE chip is a small RISC-V micro-processor using the RISC-V IM32 ISA. It targets a versatile range of energy constraint applications where low to medium processing speeds are desired, e.g. medical implants, IoT sensor nodes etc.

Description

To maximize energy efficiency, the RISC-V processor is implemented at near/sub-threshold supply voltage. This enables operation in the minimum energy point (MEP) of the device. FDSOI's unique body-biasing capabilities allow to tune the MEP towards any desired operation point. Further, the processor is equipped with a Timing-Error Detection and Correction (EDaC) technique to overcome the large design margins typically encountered at near/sub-threshold supply voltages. Thanks to the EDaC, the device is able to operate at first point of failure with minimal voltage margin.

Why EUROPRACTICE?

We appreciate the EUROPRACTICE services, which allow affordable access and reasonable prices to leading-edge IC technologies, frequent MPW-fabrication runs, CAD tools and packaging services. A research project such as this would simply not be possible without the services EUROPRACTICE provides.

VCOSDM: Body-input circuits with enhanced linearity

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/ Universidad de Sevilla), Spain

Contacts: Luis Camuñas-Mesa, Jose M. de la Rosa
E-mail: camunas.jrosa@imse-cnm.csic.es
Technology: ST 28nm FD-SOI CMOS
Die size: 1163µm x 1163µm

Introduction

The main objective of this research work is to exploit the use of enhanced body effect of ST 28nm FD-SOI CMOS technology to improve the performance of analog and mixed-signal circuits (integrated in the left part of the chip, see Fig. 1) in terms of linearity, compared to the use of bulk CMOS processes. The chip includes also a pulse generator circuit (right part) for building a tunable spiking neuron which can generate spikes with controllable shape. This will be used for implementing Spiking Neural Networks (SNNs) with STDP learning capabilities. Finally, the chip includes also a sample-and-hold circuit for characterization.

Description

As stated above, several circuits are integrated in this test chip and used as a proof of concept to test the benefits of the ST 28-nm FDSOI CMOS technology in terms of enhanced body effect to improve the linearity of some analog and mixed-signal circuits, such as Voltage-Controlled-Ring Oscillators (VCROs) and their application to design ΣΔ Analog-to-Digital Converters (ADCs). A simulated output spectrum of a 2nd-order VCO-based ΣΔM is depicted by showing the linearity improvement (see Fig. 2).

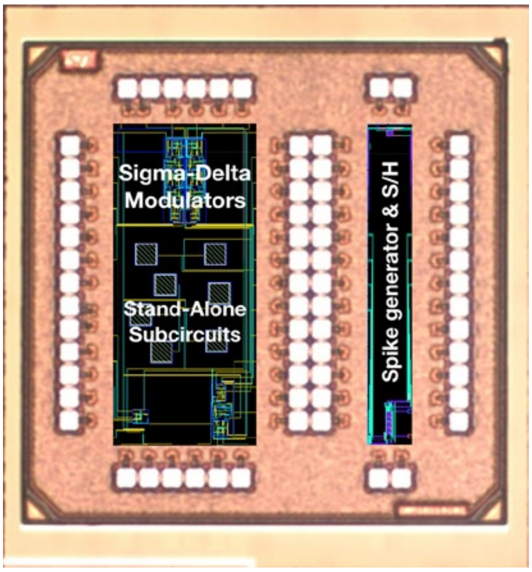


Fig.1: Photograph depicting the fabricated die overlaid with parts of the chip layout.

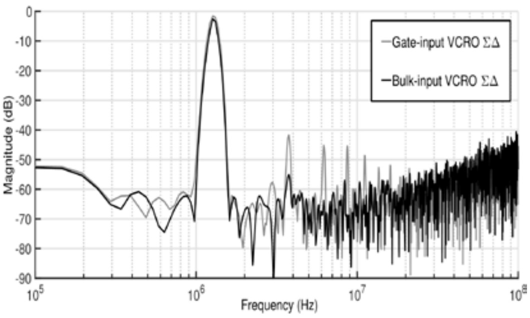


Fig.2: A simulated output spectrum of a 2nd-order VCO-based ΣΔM showing the linearity improvement.

References

[1] J. Ahmadi-Farsani and J.M. de la Rosa: "Bulk-Input VCO-based Sigma-Delta ADCs with Enhanced Linearity in 28-nm FD-SOI CMOS." Proc. of the 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, May 2019 (DOI: 10.1109/ISCAS.2019.8702810)

A 220GHz ultra-wideband FMCW radar

University of Michigan, Ann Arbor, MI, USA

Contact: Ehsan Afshari
E-mail: afshari@umich.edu
Technology: ST 55nm SiGe BiCMOS
Die size: 670µm x 770µm

Introduction

In this work, for the first time, a fully integrated imaging radar at THz/sub-THz frequencies is presented which demonstrate a fine lateral resolution without using any focal lenses/mirrors. We achieve a lateral resolution of 2mm for an object at 23cm distance as well as a range resolution of 2.7mm.

Description

To obtain the fine lateral resolution, we use near-field beam-forming algorithm based on the ISAR (Inverse Synthetic Aperture Radar) systems. The synthetized beam width is less than 0.5 degree. To achieve the decent range resolution, in a FMCW (Frequency-Modulated Continuous Wave) radar configuration, a state-of-the-art chirp bandwidth of 62.4GHz at a center frequency of 221.1GHz is generated and efficiently radiated. The level of integration and the bandwidth is the best among all published works.

Why EUROPRACTICE?

We appreciate the EUROPRACTICE services, which allow affordable access and reasonable prices to leading-edge IC technologies, frequent MPW-fabrication runs, CAD tools and packaging services. A research project such as this would simply not be possible without the services EUROPRACTICE provides.

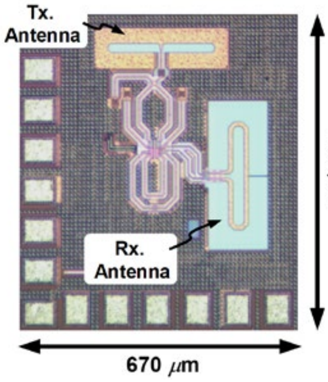


Fig.1: Layout of the imaging radar.

References

[1] A. Mostajeran, M. Naghavi, M. Emadi, S. Samala, B. Gingsburg, M Aseeri, and E. Afshari, "A High Resolution 220GHz Ultra-Wideband Fully Integrated FMCW ISAR Imaging System" IEEE Transactions on Microwave Theory and Techniques, Jan. 2019.

[2] A. Mostajeran, H. Aghasi, H. Naghavi, and E. Afshari, "Fully Integrated Solutions for High Resolution Terahertz Imaging," Proc. of IEEE Custom Integrated Circuits Con- ference (CICC), 2019 (Best invited paper award).

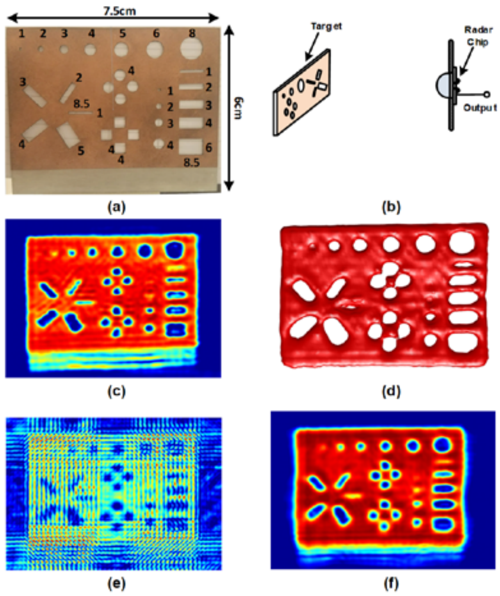


Fig.2: ISAR images:
(a) Stencil reflector as a benchmark for imaging.
(b) Plane wave imaging setup.
(c) Experimental results of ISAR image of the stencil at 15cm from the radar with a spatial sampling distance of 1mm.
(d) 3-D image of the scene from the reconstructed volume.
(e) Reconstructed ISAR image for a spatial sampling distance of 2mm to demonstrate the effect of the grating lobes.
(f) Experimental results of ISAR image of the stencil at a distance of 23cm.

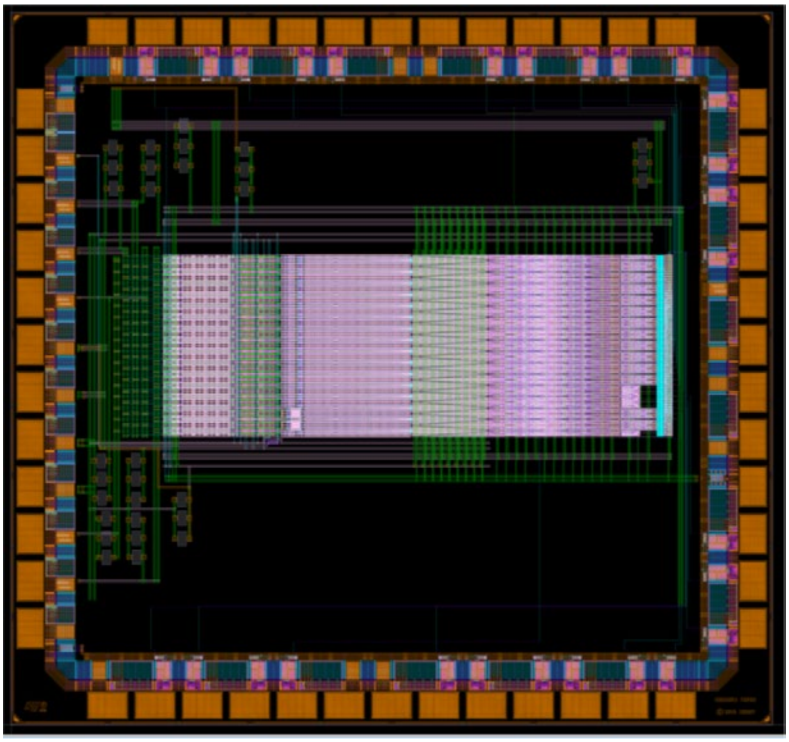


Fig.1: Layout of the IC.

Why EUROPRACTICE?

We appreciate the EUROPRACTICE services, which allow affordable access and reasonable prices to leading-edge IC technologies, frequent MPW-fabrication runs, CAD tools and packaging services. A research project such as this would simply not be possible without the services EUROPRACTICE provides.

MASSAR: A low-power 14-bits, 300KSps column ADC

XDIGIT, Grenoble, France

Contact: Daniel Dzahini
E-mail: dzahini@xdigit.fr
Technology: ST130nm HCMOS9A
Die size: 3300µm x 3600µm

Introduction

MASSAR is a new converter's architecture suitable for high-resolution-column analog-to-digital converter (ADC) for imaging applications. This design includes 32 columns featuring 14 bits of resolution. Each column needs only 24µm of pitch and dissipates 130µW while sampling at 300KHz.

Description

Some testing results are shown in Figure 2 about noise (less than 1.2LSB rms), and differential nonlinearity issues (-0.6 to 1.3LSB so no missing code), which are the most critical parameters for our imaging applications.

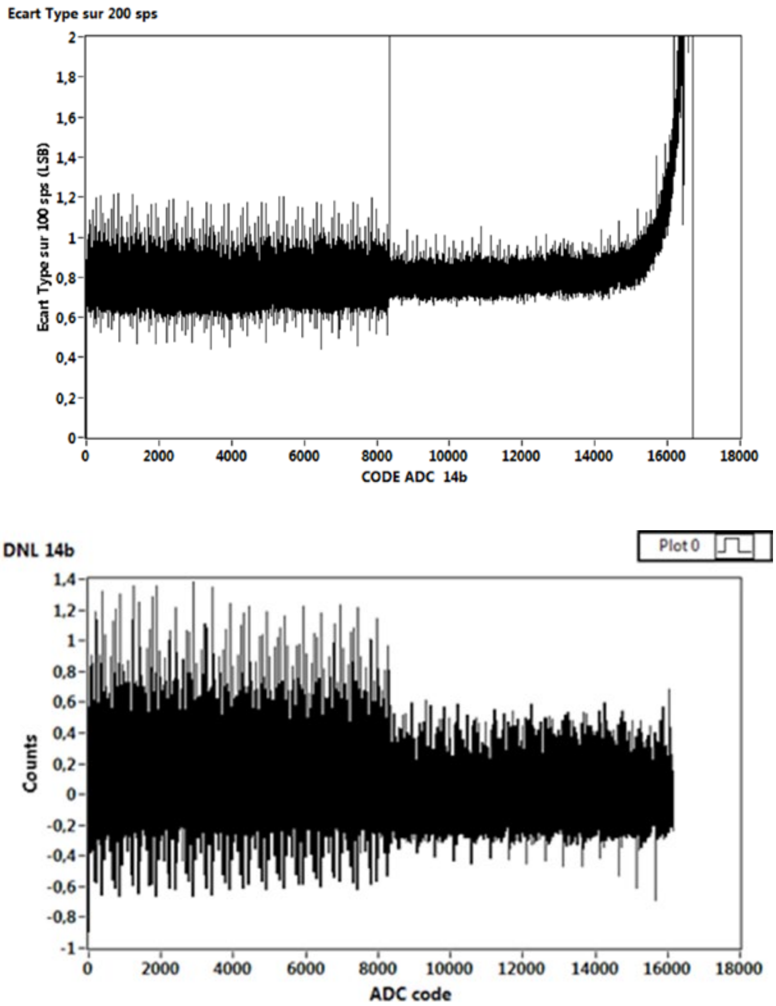


Fig.2: Standard deviation and Differential Nonlinearity (DNL).

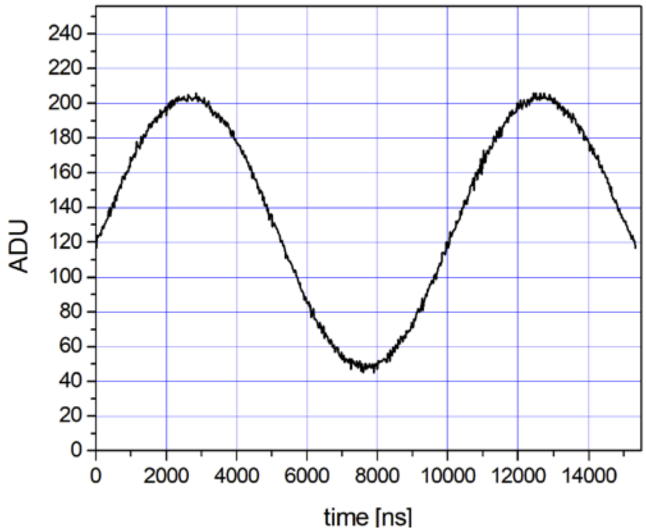


Fig.1: Digitized sine wave with 400mV amplitude, 450mV offset and 1 MHz frequency. Sampling rate was 40Msamples/s.

SAR ADC in TSMC 28nm CMOS technology

KIT ASIC and Detector Laboratory, Karlsruhe Institute of Technology, Eggenstein-Leopoldshafen, Germany

Contact: Prof. Ivan Peric
E-mail: ivan.peric@kit.edu

Technology: TSMC 28nm CMOS HPC RF
Die size: 1mm x 1mm (Microblock)

Description

Small gate size technologies are excellent choice for low-power and high-speed analogue designs. We have designed and submitted a test chip in 28nm high-performance RF CMOS technology of TSMC within a Microblock MPW run. One possible application would be the read-out of superconducting sensors or qubits.
The submitted successive-approximation-register (SAR) analog-to-digital converter (ADC) was designed by M. Tech. Mridula Prathapan. It is based on an 8-bit capacitive rail to rail DAC and a switched differential comparator. The sample and hold circuit uses a bootstrapped switch.

A synthesized digital part controls the DAC does 8-bit to 10-bit conversion of the ADC output and serializes the data words. The digital and analogue parts are designed to run with 1GHz clock, the sampling rate of 100Msamples/s with the output bit rate of 1Gbit/s. Standard cell library provided by EUROPRACTICE has been used. LVDS receiver and driver have been designed in our group. The chip contains several other test structures, such as SEU-tolerant memory cells.
First measurement results are promising. ADC works as expected. Figure 1 shows digitized sine wave with 400mV peak to peak amplitude, 450mV offset and 1 MHz frequency. Sampling rate was 40Msamples/s. Figure 2 shows the photomicrograph of the chip.

Why EUROPRACTICE?

For a small lab would be impossible to do designs in a process such as 28nm TSMC high-performance CMOS without help of EUROPRACTICE. We have submitted our design within a Microblock MPW run (die size 1mm x 1mm). The cost was only 9600 euros. EUROPRACTICE provides unique opportunity to develop circuits in modern processes for affordable price. EUROPRACTICE also provided the standard cell library and tapeout support. EUROPRACTICE provides regular MPW runs, design support, possibility of small productions. EUROPRACTICE offers access to chip design software.

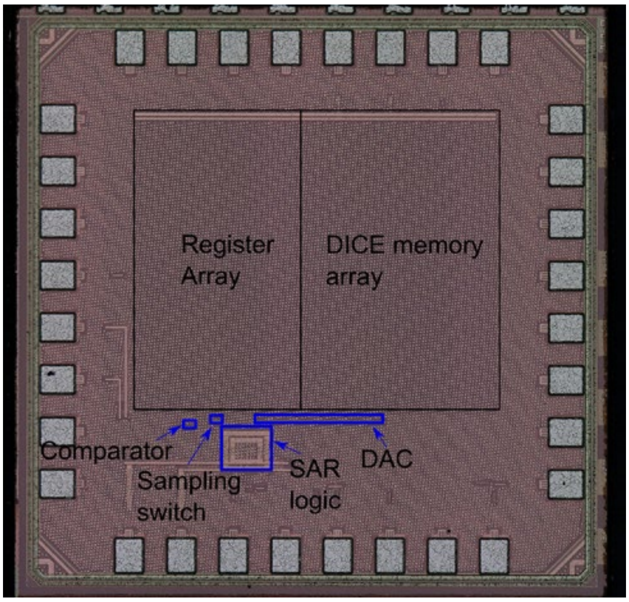


Fig.2: Photomicrograph of the chip.

Co-design of electronics and photonics components for Silicon Photonics receiver

University of Southampton, UK
in collaboration with Peking University, China

Contacts: Dr Ke Li, Dr David Thomson, Prof. Fan Zhang, Prof. Graham Reed
E-mail: kl@ecs.soton.ac.uk

Technology:
TSMC 28nm CMOS HPC RF + imec Si-Photonics ISiPP50G
Die size: TSMC 28nm: 1mm x 1mm (Microblock)

Description

The interest in developing silicon photonic interconnects to meet the growing demands of data processing speed and bandwidth has increased over the last decade. While there have been significant research efforts in developing standalone silicon Photodetectors (PD) or Transimpedance Amplifier (TIA), work on integrating these two components is limited, which is necessary for the practical implementation of silicon optical interconnects.

So far, work on silicon photonics-electronics integration is mostly limited to the physical coupling approach between photonic and electronic devices such as wire- or flip-chip bonding. In this work, we presented an alternative design approach where PD and TIA are co-designed synergistically to generate fully differential signals, which are essential for complex modulation formats under a direct detection scheme.

As shown in the Figure 1, we proposed a fully differential optical receiver, in which the CMOS TIA is co-designed with a balanced photodetector. Without using any DSP or equalization technique, measurement results show that the integrated receiver can operate at more than 50Gb/s under a 1V power supply (for the TIA) and the overall power efficiency can be optimized to 1.0pJ/bit.

This silicon photonics receiver is cooperatively designed and packaged by the researchers from Peking University (China) and the University of Southampton (UK). The silicon photonic photodetector is fabricated via the imec silicon photonics ISiPP50G platform. The CMOS TIA is fabricated via the EUROPRACTICE Microblock MPW program by using the TSMC 28nm HPC process.

Why EUROPRACTICE?

The University of Southampton has worked with EUROPRACTICE for TSMC fabrication for many years. We have benefitted from EUROPRACTICE's excellent technical support for CMOS chip submission. EUROPRACTICE has given us affordable access to frequent multi-project wafer fabrication runs.

Acknowledgements

This work was supported by UK's EPSRC through the Silicon Photonics for Future Systems (SPFS) Programme (EP/L00044X/1), National Natural Science Foundation of China (No. 61535002), and National Key R&D Program of China (No. 2018YFB1801204). D. J. Thomson acknowledges funding from the Royal Society for his University Research Fellowship.

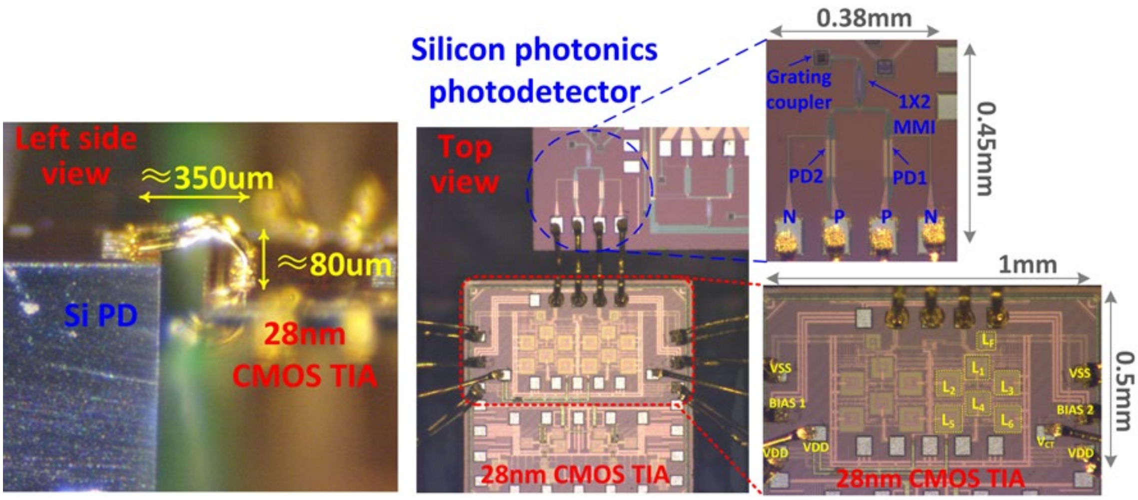


Fig.1: Microscope view of the packaged silicon photonics photodetector and CMOS TIA.

Ring oscillator-based time-to-digital converter

Electrical Engineering (ESAT) TC, KU Leuven, Campus Geel, Belgium

Contacts: Bjorn Van Bockel, Jeffrey Prinzie, Paul Leroux
E-mail: bjorn.vanbockel@kuleuven.be
Technology: TSMC 65nm CMOS LP MS/RF
Die size: 1920µm x 1920µm (mini@sic)
Design tool: Cadence IC v6.1.6

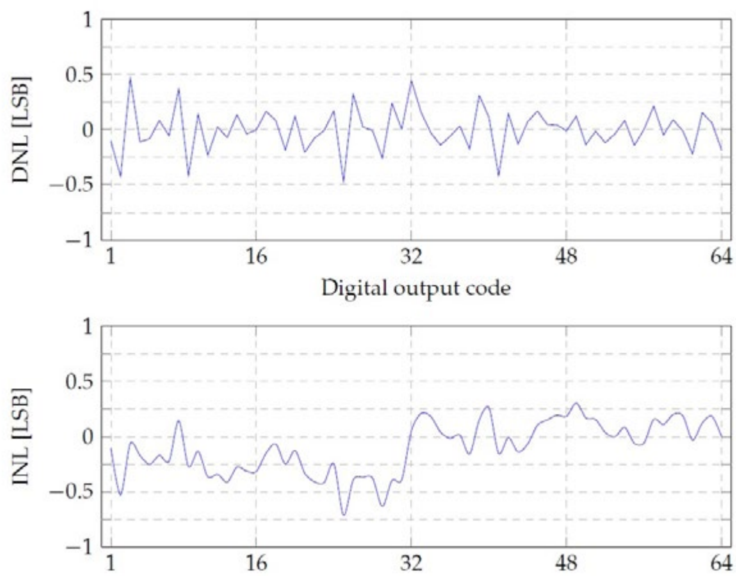


Fig.1: INL and DNL Measurement.

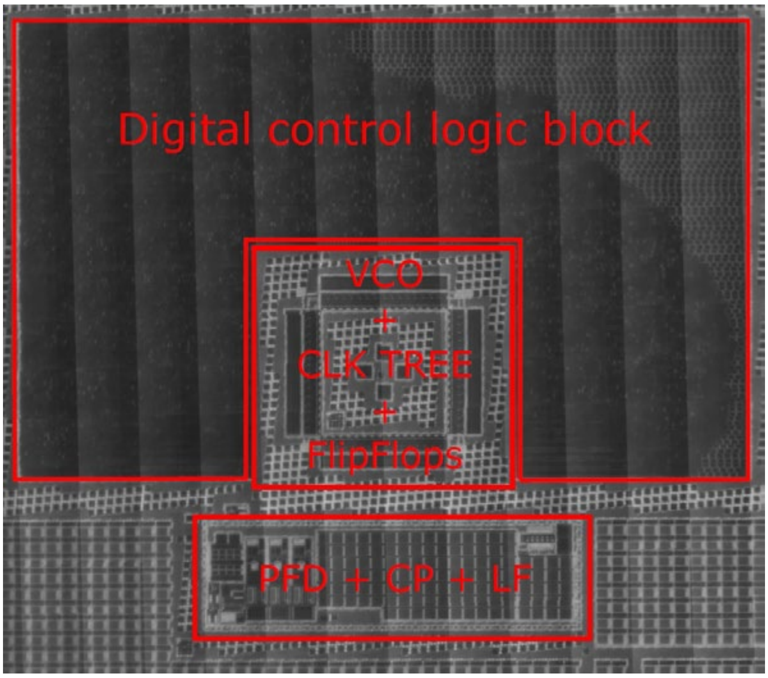


Fig.2: Photomicrograph of the RINGTDC.

Description

Time-to-digital converters (TDCs) can be compared to analog-to-digital converters (ADCs) as they digitize analog time differences instead of analog voltage differences. Several applications require precise time measurements. For example, time-of-flight (TOF) measurements or particle tracking in high energy physics, where the precision of distance measurements is related to the resolution of the TDC.

The design presented is based on a second-order phase-locked loop (PLL) with a ring oscillator as voltage-controlled oscillator (VCO). The VCO, which consists of 64 delay cells, is based on pseudo differential delay cells. The PLL is locked to a reference clock of 125 MHz with a multiplication factor of 8. The VCO thus runs at a stable frequency of 1 GHz, which leads to a period of 1 ns for the fine detection range. Therefore, once the PLL is locked the average static delay of the delay cells is 15.6 ps. The PLL feedback loop is used to ensure that the TDC is robust against process, voltage and temperature (PVT) variations, and additionally to variations due to ionizing radiation.

The TDC prototype was manufactured in 65nm CMOS technology. The static INL and DNL were measured by performing a code density test, using a random hit generator, which runs completely uncorrelated to the reference clock of the TDC. The measured DNL and INL are shown in Figure 1 and are bound between -0.42/+0.47 LSB and -0.71/+0.30 LSB, respectively.

Why EUROPRACTICE?

EUROPRACTICE offers researchers the possibility of designing ASICs in different technologies for an affordable price. Also, the support in the many different PDK's is excellent. Registration and submission of a design is very convenient.

ZEBRA: A compact and low-power bridge-to-digital converter

MCCI, Tyndall National Institute, Lee Maltings Complex Dyke Parade, Cork, Ireland

Contacts: Dr Ivan O' Connell, Annamaria Fordymacka
E-mail: ivan.oconnell@mcci.ie

Technology: TSMC 65nm CMOS LP MS/RF
Die size: 2mm x 2mm (mini@sic)

Description

Temperature sensors are required in a vast number of applications such as food monitoring or MEMS compensation. Resistive sensors achieve good efficiency but typically occupy more area than their MOS and BJTs counterparts. Traditionally, the temperature sensor read-out circuitry would consist of a Wheatstone bridge followed by an instrumentation amplifier that would require high input impedance and low input-referred noise. While the design of such an amplifier is challenging, the design of the subsequent analog-to-digital converter (ADC) is equally if not more demanding, to ensure that these blocks do not limit the resultant achievable resolution and accuracy. There have been many attempts to remove the requirement for the input instrumentation amplifiers from temperature-to-digital converters, but the majority of these are based on either sigma-delta or VCO based ADC, which trade area for power.

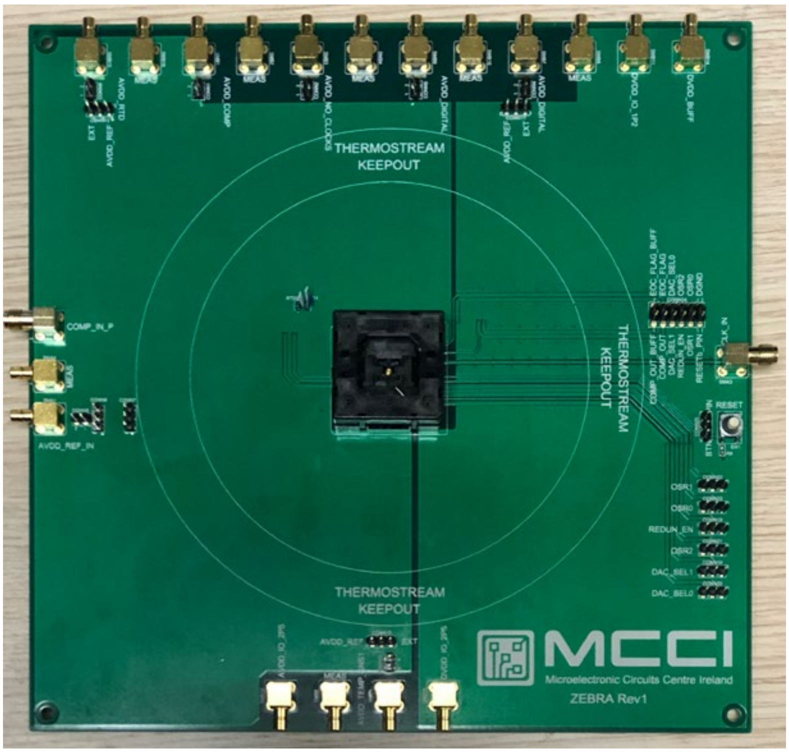


Fig.1: PCB ZEBRA

Our design employs a 12-bit Successive Approximation Register (SAR) ADC that is a popular low-power and mid-resolution solution and due to its highly digital architecture, scales well with technology. To achieve higher-sensitivity, the sensor was built with silicided p-poly and non-silicided n-poly resistors. The bridge-to-digital converter occupies only 0.01mm^2 taking a benefit of 65nm technology.

Why EUROPRACTICE?

EUROPRACTICE has given us PDK and foundry access to state-of-the-art semiconductor processes of TSMC and other manufacturers. We got good technical support from EUROPRACTICE engineers. All technical questions were timely addressed and when necessary their resolution was escalated to foundry technical team. We have also benefitted from EUROPRACTICE's support for dummy/density fill, chip submission and chip packaging processes. Finally, EUROPRACTICE has given us affordable access to frequent multi-project wafer fabrication runs and also to mini@sic shuttles.

Analog and high-voltage blocks for an implantable device

Biomedical Electronics Research Group, Department of Information and Communications Technologies, Pompeu Fabra University, Barcelona, Spain

Contact: Albert Comerma
E-mail: albert.comerma@upf.edu
Technology:
TSMC 0.18µm CMOS HV BCD Gen II
Die size: 2500µm x 2500µm (mini@sic)

Description

This microdevice comprises several analog and high-voltage building blocks for future prototypes. The design is in the framework of the eAXON research project aimed to obtain wireless implantable devices powered by epidermically applied high-frequency currents. The designed blocks floorplan uses a narrow design with a height of the blocks below 300µm. The submitted design includes a high-voltage bandgap reference that provides 1.2V with an input voltage between 3.6V and 24V as showed during tests. The reference is then connected to a low drop-out regulator to provide the 1.8V of the core supply (see Fig. 1). It has also been tested in the full operation range. At the input of the circuit, a rectifier bridge permits to use either AC (with double peak to peak voltage) or DC voltage independently of the polarity. The Schottky diodes rectifier has also been tested. Lastly, a binary weighted DAC using a current reference derived from the voltage one and a 4 MHz RC oscillator is also included. All of them have been successfully tested on 20 packaged devices and working as expected. The only element showing more variation than expected is the RC oscillator with a typical frequency of around 3.2 MHz instead of the 4 MHz it was designed for.

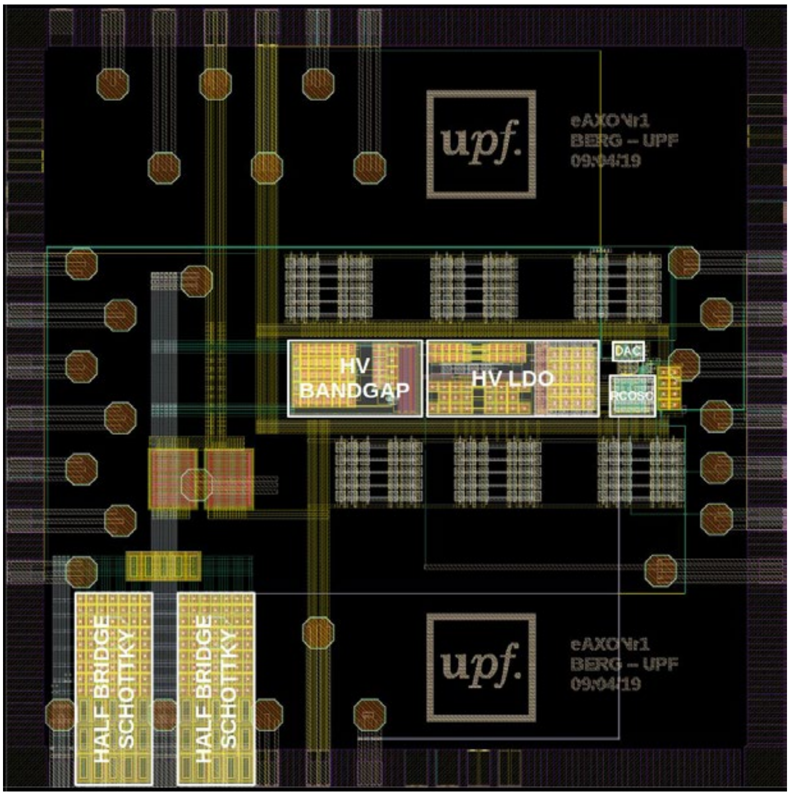


Fig.1: Layout of the designed device.

Why EUROPRACTICE?

For small volume ASIC production EUROPRACTICE offers an excellent solution both in the frequency of MPW runs (mini@sic program) as in price and tools needed for the design. The software tools provided by the different main vendors through EUROPRACTICE with low price licensing permit to choose and get started with the one that best fit our needs and technology including frequent training available. This makes an ideal choice for the submission and packaging of prototypes with relevant innovations. The excellent support is also an added benefit of submitting through EUROPRACTICE.

Acknowledgement

This project has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (Grant agreement No. 724244).

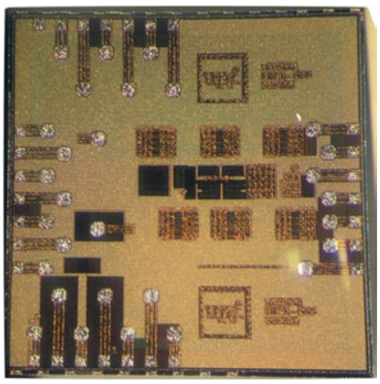


Fig.2: Photograph of the fabricated chip.

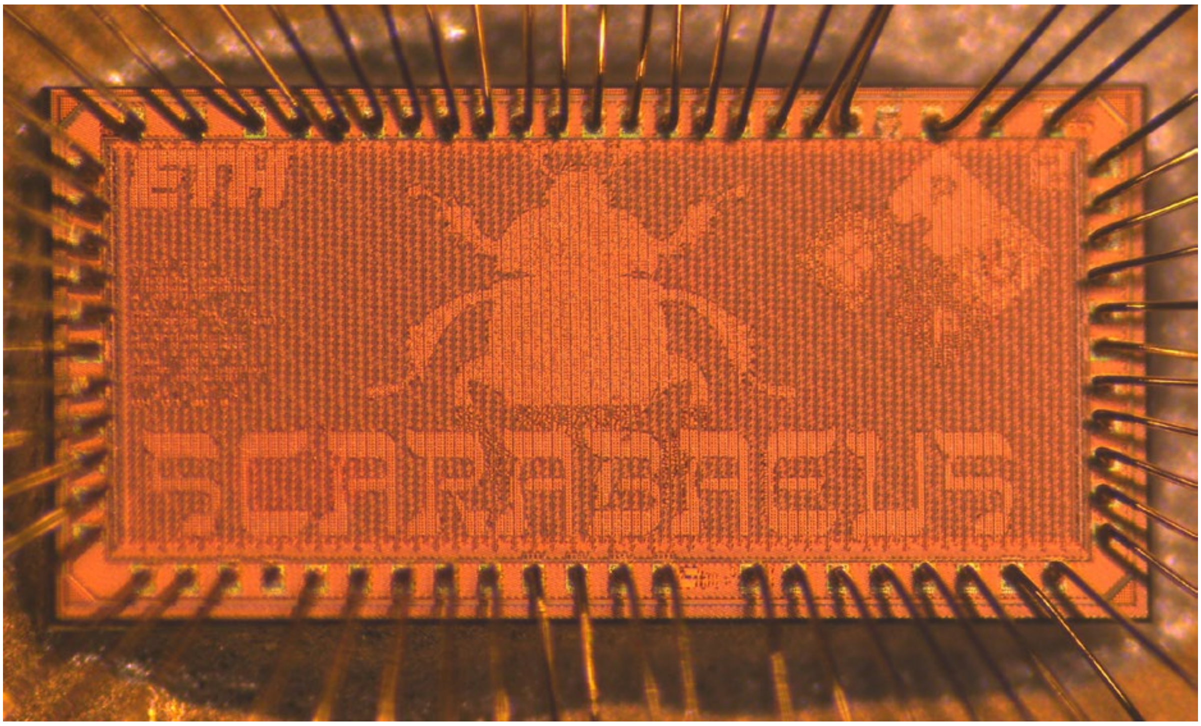


Fig.1: Micrograph of the Scarabaeus Die.

Scarabaeus: 64-bit RISC-V processor and HyperRAM interface as part of student projects

ETH Zürich, Switzerland

Contacts: Fabian Schuiki, Florian Zaruba
E-mails: fschuiki@iis.ee.ethz.ch, zarubaf@ee.ethz.ch
Technology: UMC 65nm Logic/Mixed-Mode/RF – LL
Die size: 2626µm x 1252µm
Design tools: Mentor Questasim simulator, Synopsys Design Compiler, Cadence Innovus, Synopsys Tetramax and Mentor Calibre

Description

Scarabaeus was designed by five students Thomas Benz, Thomas Kramer, Gian Marti, Stephan Keck, Armin Berger working on two separate semester theses in the Electrical Engineering department of ETH Zürich. Supervised by experienced designers, the students have 14 weeks time to design the ASIC from start to finish. They are aided by a lecture series that provides step-by-step tutorials for ASIC design running in parallel to their semester thesis. In Scarabaeus, the work of the two student groups complemented each other and resulted in one ASIC.

One of the theses concentrated on designing an efficient HyperRAM interface that allows a small pincount interface to memory blocks manufactured by Cypressm, with a throughput of 327 MB/s when operating using long bursts. This can be seen occupying the bottom part of the chip, with the required controller neatly fitting in the space between I/O pads. In the die micrograph the area where the controller is located can be seen just below the last 'A' of the logo, where the distance between the bond pads is slightly larger when compared to the others.

The second thesis concentrated on implementing a complete 64-bit microcontroller that uses the above mentioned HyperRAM interface and several additional peripherals. The system is based around the 64-bit RISC-V core Ariane that was developed within the Digital Circuits and Systems Group led by Prof. Luca Benini as part of the popular PULP project. The thesis added an efficient direct memory access (DMA) module that could be used to copy tensors between memory locations with programmable element size, shape and density in up to 4 dimensions. This gives the DMA enough flexibility to copy data from common machine learning applications between a large external memory (possibly over the HyperRAM interface) and local memory in chip independently from the processor that could then concentrate on running applications rather

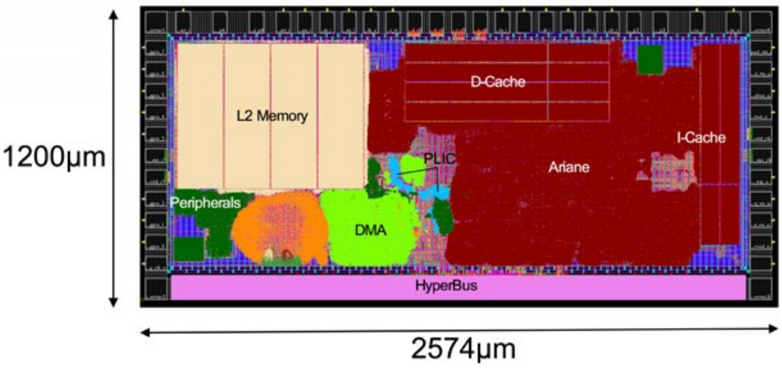


Fig.2: Floorplan of the die showing various components within the chip. Most area is occupied by the RV64 Ariane core.

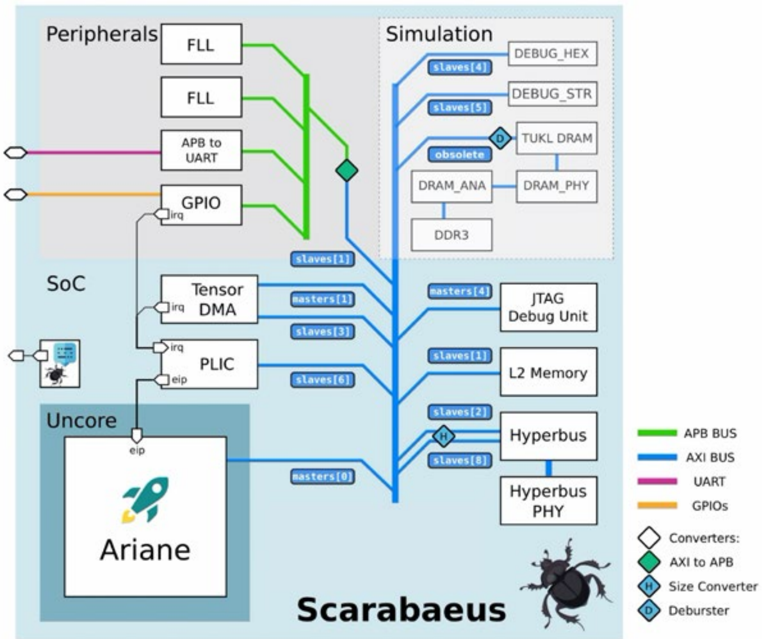


Fig.3: Bock diagram of Scarabaeus, showing different components and simulation environment.

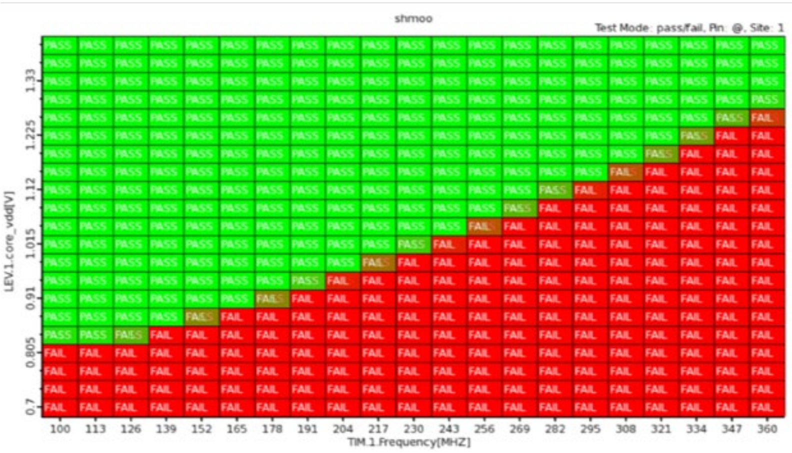


Fig.4: Shmoo plot from measurements showing operating frequency vs supply voltage at room temperature.

than data transfers. In addition, an open source platform-level interrupt controller (PLIC) compatible with the RISC-V standard has been designed.

The chip arrived back from manufacturing in early 2019; as part of a follow-up lecture on ASIC testing, the students were able to test their own chip on an industrial Advantest V93000 tester and have shown that it was functional at 330MHz (room temperature, at nominal voltage).

The Scarabaeus project resulted in several additional blocks that became part of the open source PULP platform and allowed students to gain first-hand experience in the design and test of a fairly involved 65nm ASIC.

Tool flow for Scarabaeus

For our UMC65 IC Design flow we rely mainly on tools we have obtained from EUROPRACTICE RAL service. RTL simulation is performed using Mentor Questasim simulator, logic synthesis with Synopsys Design Compiler, back-end design with Cadence Innovus, DFT insertion with Synopsys Tetramax and Mentor Calibre tools are used for DRC and LVS. The students usually design their chips in a semester thesis that runs in parallel with a VLSI design class that includes practical tutorials in the same technology. For the installation of the tools, management of the licenses and the development of the design flows, and the MPW submission, the Microelectronics Design Center of ETH Zurich with its four permanent employees provides support.

Why EUROPRACTICE?

ETH Zürich has established a strong and very successful curriculum in its undergraduate program that allows students to develop their own ASICs. Scarabaeus is part of this program. Such projects would not have been possible without the strong partnership we have with EUROPRACTICE-IC Service. Setting up such a curriculum and taping out several chips every year requires a close working relationship with an MPW provider, and we have been very happy with our interaction with EUROPRACTICE-IC service over the years.

Multi-band RF transceiver for reliable communication in industrial environments

Chair of Integrated Analog Circuits and RF Systems, RWTH Aachen University, Aachen, Germany

Contacts: Markus Scholl, Tobias Saalfeld, Johannes Bastl, Christopher Nardi, Christoph Beyerstedt, Fabian Speicher, Jonas Meyer, Ralf Wunderlich, Stefan Heinen
E-mail: ias@rwth-aachen.de
Technology: UMC 130nm RF CMOS
Die size: 3.3mm x 3.3mm (mini@sic)

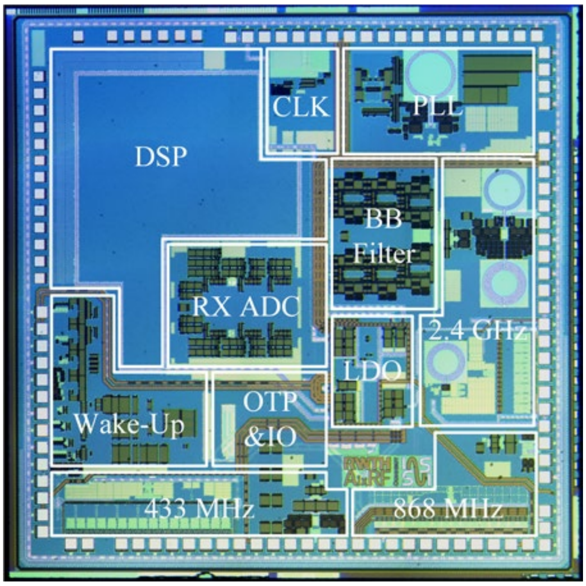


Fig.1: Photograph of the fabricated die.

Description

To verify new concepts in silicon and ensure optimum performance this RF Transceiver has been fabricated as four blocks of the mini@sic program. The targeted application of this transceiver is a highly reliable wireless communication in industrial environments. Particularly, the very low latency as well as the interference-immune multi-band design qualifies the transceiver for safety and time critical control loops. In usage scenarios demanding a long battery life of wireless appliances, like wireless sensor networks, the fully integrated wakeup receiver enables minimum power consumption of the network nodes during their idle times.

The multi-band multi-standard wireless transceiver is designed for the unlicensed 433MHz, 868MHz and 2.4GHz bands. It comprises a single frequency synthesizing PLL for RX and TX paths for all three bands. Similarly, the RX baseband processing core is shared among the three bands. The transceiver supports various modulation schemes and data-rates (10kbit/s to 2Mbit/s) and, thus, is applicable for multiple standards. The integrated dual-mode wakeup receiver working at 868MHz and 2.4GHz enables an ultra-low power standby operation for energy savings. Due to the high re-configurability the performance of the analog circuitry can be thoroughly evaluated while it also allows support for diverse applications. Altogether, the fabricated transceiver SoC is an innovative reconfigurable research platform enabling development of future applications, for which no commercial communication solutions are expected to be available within the next years.

Why EUROPRACTICE?

EUROPRACTICE's mini@sic program is a great opportunity for universities to do affordable prototyping in state-of-the-art nanoscale CMOS technologies. The access to key software IC design tools, the great technical assistance and customer friendly attitude of its staff members is an invaluable benefit to our tapeouts and thereby enhances the success of our research significantly.

Acknowledgements

We would like to express our gratitude to the HiSilicon Sponsorship Program for covering the tapeout expenses and to EUROPRACTICE and imec for their excellent support during this tapeout and throughout the last years.

PRINCSA - The Programmable Read-out with Improved Noise-performance Charge Sensitive Amplifier for microstrip sensors read-out

AGH University of Science and Technology, Department of Measurement and Electronics, Kraków, Poland

Contacts: Weronika Zubrzycka, Krzysztof Kasinski
E-mail: zubrzycka@agh.edu.pl
Technology: UMC 180nm Mixed-Mode/RF
Die size: 1565µm x 1565µm (mini@sic)
Design tool: Cadence v5.1.41-USR5

Description

The Programmable Read-out with Improved Noise-performance Charge Sensitive Amplifier (PRINCSA) is a prototype ASIC dedicated for radiation imaging using silicon microstrip sensors (Fig. 1). The IC shown in Fig. 2 was designed to meet the tight requirements of the tracking detectors for High-Energy Experiments: low noise, charge processing speed (expected, near megahertz interaction rates), parameters uniformity in many channels, linearity up to 12 pF signal, and good resolution of time and amplitude measurements [1]. The main goal of this project was optimization of the overall system noise expressed as Equivalent Noise Charge, ENC lower than 1000 e- rms. The power supply interference is one of the factors that may compromise the charge measurement capabilities. This chip comprises of 3 single-ended and 3 differential channels, each of them including a charge sensitive amplifier (CSA), a fast shaping amplifier for time measurements and a slow shaping amplifier for amplitude measurements. Single-ended and differential channels with identical input stages (and additionally CSA replica in the differential ones [2]) and similar filter architectures are placed on a same bulk to compare the noise performance and possibility to improve the Power Supply Rejection Ratio (PSRR) using differential charge processing. In the single-ended channels the CSA feedback is a novel combination [3] of a fast reset with a double-polarity Krummenacher circuit for leakage current compensation for both polarities of charge pulse and leakage current [4] without compromising the large value of the CSA feedback resistance. The ASIC is equipped with the calibration circuit operating in the double-polarity or in the single-polarity mode. The nominal supply of the design is 1.8V, and the biasing potentials and currents are generated by internal global DACs. For the Signal to Noise Ratio

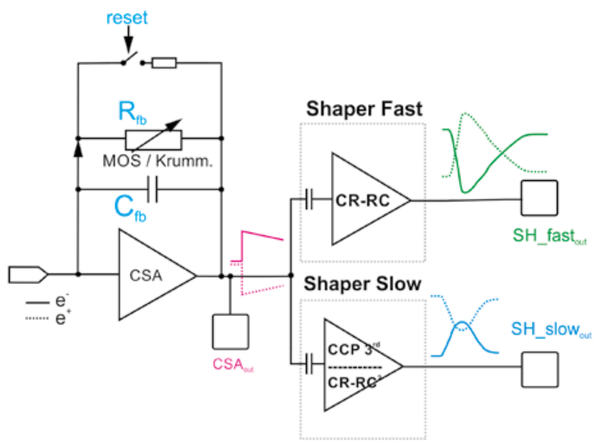


Fig.1: Simplified schematic of the implemented circuits.

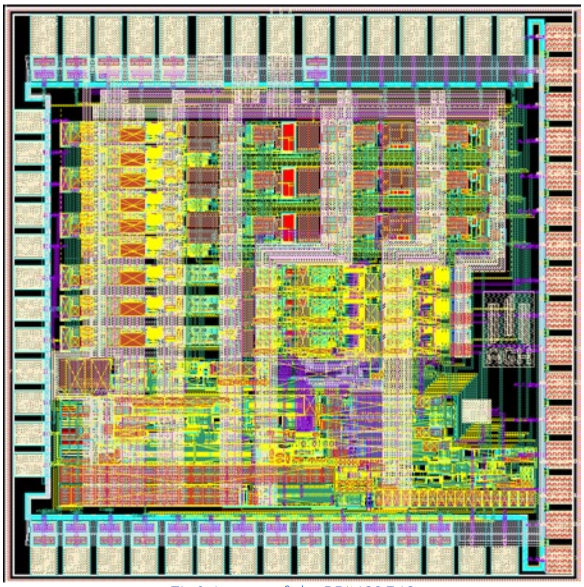


Fig.2: Layout of the PRINCSA IC.

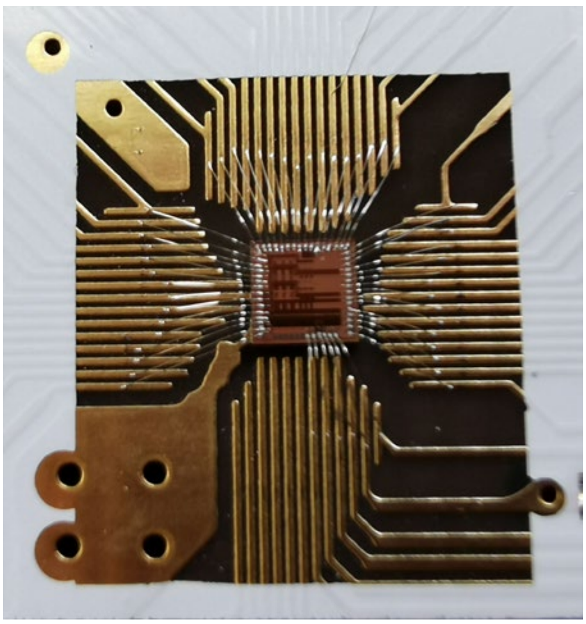


Fig.3: The DUT (Device Under Test) on the test board.

(SNR) improvement without the need for external components (e.g. bulky external capacitors), the internal R-C (MOS) filtering of the crucial biasing potential of the CSA input transistor is added in every channel. The design is configurable to enable tuning of the read-out chain depending on variable conditions (dominating noise source, sensor capacitance) by implementation of switchable filters architecture (CR-RC^2 and complex conjugate poles 3rd order) and peaking time (90, 180 and 250 ns).

Performance

The design was measured (Fig. 3) and characterized. Results show good agreement with simulated values, and the charge processing characteristics are linear up to 11 fC of input charge of both polarities (for slow shaping amplifier). The benefits of using the differential front-end when using noise power supply are visible in measurements.

Why EUROPRACTICE?

Our department has used EUROPRACTICE service for many years. It is affordable and easily available for the prototyping purposes for teaching and research, especially for Ph.D. students. The mini@sic program is an excellent and cost-effective choice to test several new ideas and circuitries. We also appreciate the well-qualified technical support team, which is very important for the successful tape-out process.

Acknowledgment

This work was funded by the Ministry of Science and Higher Education Poland, from the scientific budget in years 2016-2019 – a research project in the programme "Diamentowy Grant".

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A high-temperature low-power delta-sigma ADC

Integrated Circuits Design Center, Institute of Physics, Nanotechnology and Telecommunications, Peter the Great St. Petersburg Polytechnic University, Saint Petersburg, Russia

Contacts: Prof. Dr. Alexander S. Korotkov, Dr. Dmitry V. Morozov, Dr. Mikhail M. Pilipko, Dr. Mikhail S. Yenuchenko

E-mail: korotkov@spbstu.ru

Technology: X-FAB XT018 0.18μm SOI CMOS

Die size: 3000μm x 900μm

Design tools: Cadence Virtuoso, Calibre Mentor Graphics, Cadence Encounter

Description

Development of high-temperature electronic devices is an important problem. Currently, analog-to-digital converters (ADCs) based on delta-sigma modulators are widely used. Such ADCs have low power consumption with a sufficient number of output bits. The high-temperature low-power delta-sigma ADC consists of two parts. The first one is a switched-capacitor low-pass filter and a delta-sigma modulator. The second part is a digital filter for decimation of the modulator output (see Fig. 1). The ADC is designed for 10 MHz clock frequency and a passband of 100 kHz. The X-FAB SOI CMOS technology is employed. The ADC provides 11-bit effective resolution and consumes 37 mW from 5 V power supply. The 5th order low-pass filter has a balanced structure. The 2nd order delta-sigma modulator utilizes a 2-bit quantizer. The digital filter decimates the output code of the modulator by 48 times.

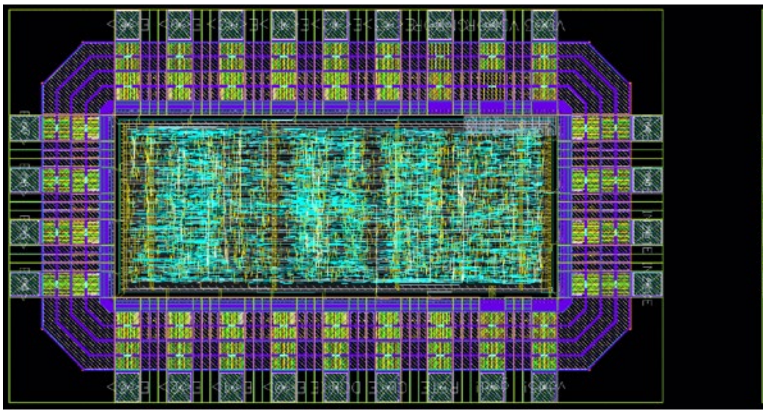

Fig.1: (a) Layout of one of the two parts of the designed ADC: a switched-capacitor low-pass filter and a delta-sigma modulator.

Results

The ADC provides SNDR of no worse than 70 dB with the input frequency of 100 kHz and a differential amplitude of 500 mV at the temperature up to 175 °C.

Design software

The following software has been used for the chip design: Cadence Virtuoso, Calibre Mentor Graphics, Cadence Encounter.

Why EUROPRACTICE?

Our University has been using EUROPRACTICE initiatives since 2005. The EUROPRACTICE service offers affordable prototyping for research. EUROPRACTICE offers very frequent access to fabrication in different kind of technologies. Also, EUROPRACTICE staff offers excellent technical support regarding technology PDK and general guidance regarding the design of the devices. The EUROPRACTICE service is always open to questions and suggestions related to delivery and billing.

Acknowledgement

This work was financially supported by the Ministry of Science and Higher Education of Russian Federation under Grant 8.1704.2017.

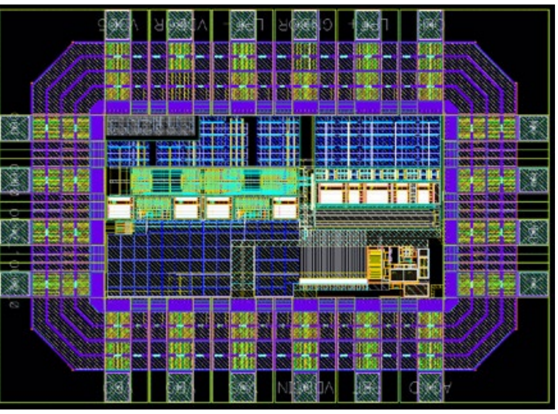

Fig.1: (b) Layout of one of the two parts of the designed ADC: a digital filter for decimation of the modulator output.

LED Driver

BKIC, School of Electronics and Telecommunications (SET), Hanoi University of Science and Technology (HUST), Hanoi, Vietnam

Contact: PhD. Loan Thanh Pham-Nguyen
E-mail: loan.phamnguyenthanh@hust.edu.vn
Technology: X-FAB XT018 0.18µm SOI CMOS MET3/4/MID/THK
Die size: 1520µm x 3040µm (mini@sic)

Description

Power management block is an essential part within every electrical device. Therefore, the raised demands for a DC-DC converter keep on increasing. Rather than just improving the efficiency while eliminating unwanted losses, reducing the size of the circuit is also another pattern to develop power circuits. As a result, implanting those circuit in integrated level sounds the most appealing. The tiny size of Power management ICs can lead to a significant increase in the power density and they are more likely to be implemented in smart applications or biomedical implants.

The DC-DC converter designed in this work aims to a LED Driver application specified for LEDs in Vietnam with high-input voltage and high-output current. More precisely, it receives an input voltage of 120V while its output voltage can be adjusted within the range from 0-30V according to the external duty cycles of control clocks applied to the circuit. An optimized DC-DC Dual-Inductor Hybrid Converter based Dickson topology [1, 2] was taken into consideration to satisfy such high voltage requirement. After that, the X-FAB HV SOI XT018 technology in EUROPRACTICE mini@sic program was chosen to design and fabricate this circuit. The design consists of a total of six power switches, four gate drivers with level shifters and bootstraps for four high-side switches. Buffer blocks are matched with sizing of corresponding switches to provide necessary driving capability. Seal-ring and pads with ESD protection are also implemented. Due to the limited area of the mini@sic die size, the capacitors and inductors could not be designed on-chip and thus they were fabricated as off-chip components instead. The layout and microscope picture of the designed LED Driver are depicted in Figure 1 and Figure 2.

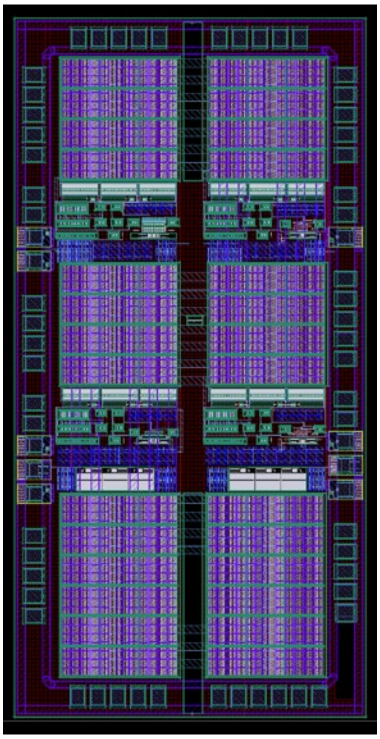

Fig.1: Layout picture of the designed LED Driver in technology X-FAB HV SOI XT018

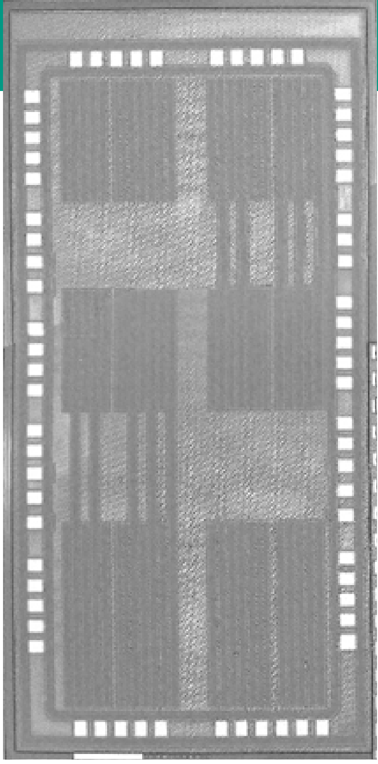

Fig.2: Microscope picture of the designed LED Driver in technology X-FAB HV SOI XT018

Why EUROPRACTICE?

EUROPRACTICE provides a wide range of technologies for our requirements. As an academic research group in Vietnam, we found that the offered prices for both fabrication and packaging are also affordable. This led us to a greater change to process our research, implement practical product and verify our design. In addition, the staff provides very helpful support whenever being asked.

References

[1] L. Pham-Nguyen, V. Nguyen, D. Nguyen, H. Han, K. Nguyen and H. Le, “A 14-W 94%-Efficient Hybrid DC-DC Converter with Advanced Bootstrap Gate Drivers for Smart Home LED Applications,” 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 4744-4749.

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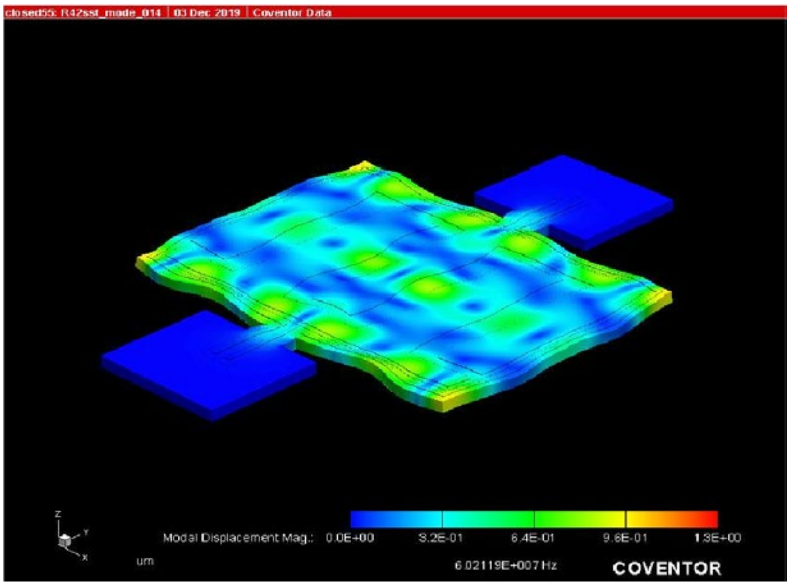

Fig. 1: Simulation results for the 5th mode lateral resonance obtained using Coventorware.

Piezoelectric MEMS lateral bulk acoustic wave resonators

Department of Microelectronics and Nanoelectronics, University of Malta, Malta

Contact: Mounira Bengashier
E-mail: mounira.bengashier.15@um.edu.mt

Technology: PiezoMUMPs Technology
Die size: 11.15mm x 11.15mm

Description

A number of resonators were designed using the PiezoMUMPs technology, and submitted to EUROPRACTICE for fabrication. These resonators were of different sizes and having various drive electrode geometries in order to evaluate their effect on the resonant frequency and quality factor. This work is part of a Ph.D. research study on the design of piezoelectric MEMS lateral bulk acoustic wave resonators with particular reference to the thermal effect on the resonant frequency. This study compares the results obtained from both analytical models as well as finite element simulations while including temperature effects. A comparative study has been carried out on resonators exhibiting a resonant frequency of around 19.5 MHz using the PiezoMUMPs MPW process, which consists of a 0.5μm AlN layer over an SOI structure having a thickness of 10μm. Both the analytical and the finite element models indicate a frequency variation of 300 kHz over a temperature range of 273-573 K. Based on these results, a number of PiezoMUMPs resonator prototypes, including a thermal heating element, have been designed in order to explore the feasibility of fine tuning the resonant frequency using the thermal effect. The possibility of fine tuning can be applied to high precision timing circuits such as frequency counters.

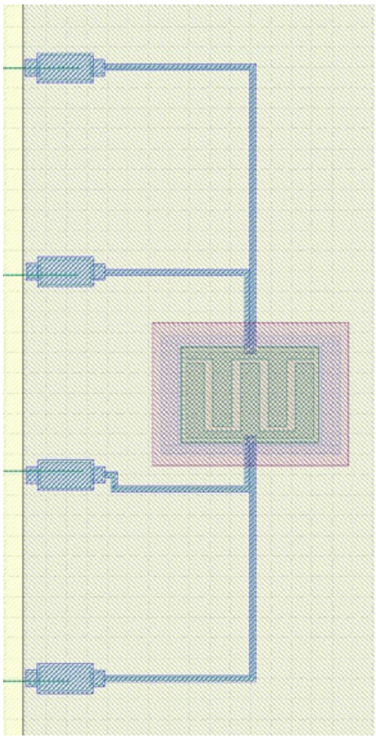

Fig.2: Layout of the designed resonator.

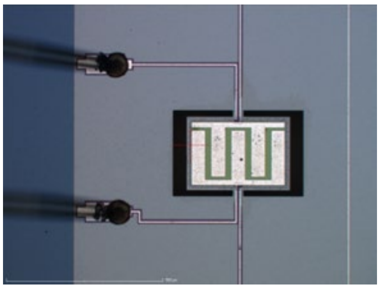

Fig.3: Microphotograph of the resonator.

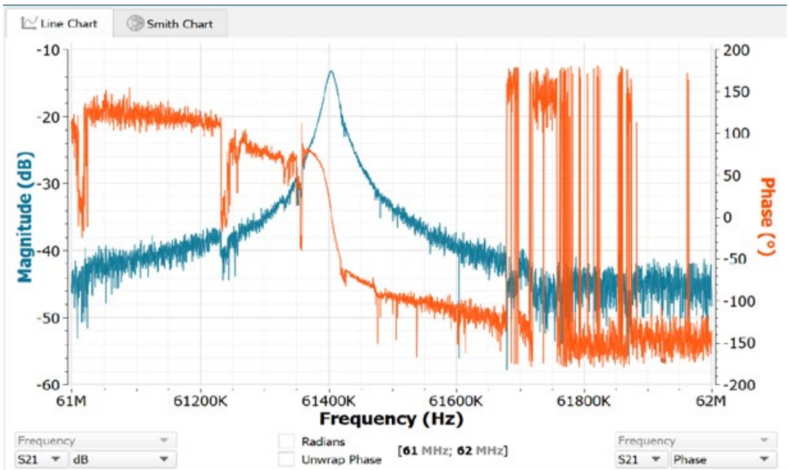

Fig.4: Measured S21 scattering parameter data showing a resonant frequency of 61.348 MHz.

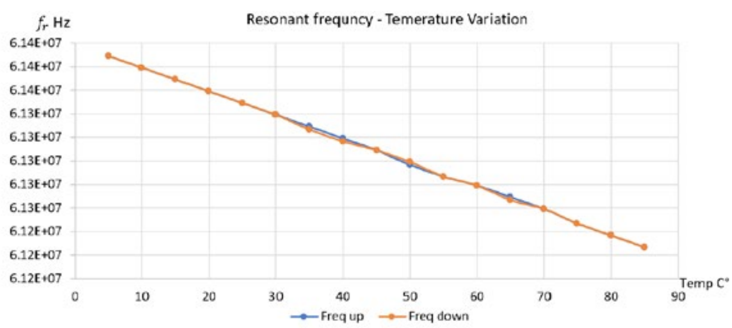

Fig.5: Variation of the measured resonant frequency with temperatures.

The attached figures and measured data belong to one resonator (250µm by 350µm), designed with interdigitated electrodes and a thermal heating element. The fifth mode resonant frequency was found to be 61.348 MHz during the measurement and characterisation performed using a vector network analyser. This is close to the simulated value of 62.212 MHz. A quality factor of Q_f = 2,928 was estimated and the motional impedance values were found to be R_m= 442.2 Ω, L_m = 3360 H and C_m= 22.6 mF.

Why EUROPRACTICE?

The EUROPRACTICE service offers affordable simple procedures to access the technology to produce IC prototypes for research purposes, and this service is always open to provide support and answer questions regarding technical issues encountered by the users.

Acknowledgement

We would like to acknowledge the Ministry of High Education in Libya for supporting the Ph.D. research work of Mounira Bengashier, which is currently being carried out at the Department of Microelectronics and Nanoelectronics at the University of Malta.

Microring resonator-based architectures for flexible-grid networks (FlexNet)

Dipartimento di Elettronica e Telecomunicazioni (DET), Politecnico di Torino, Turin, Italy
PhotoNext Interdepartmental Center, Politecnico di Torino, Turin, Italy

Contacts: P. Bardella, A. Bianco, R. Gaudino, G. Giannuzzi, M. Gioannini
E-mail: paolo.bardella@polito.it
Technology: imec Si-Photonics ISiPP50G
Die size: 2.5mm x 2.5mm

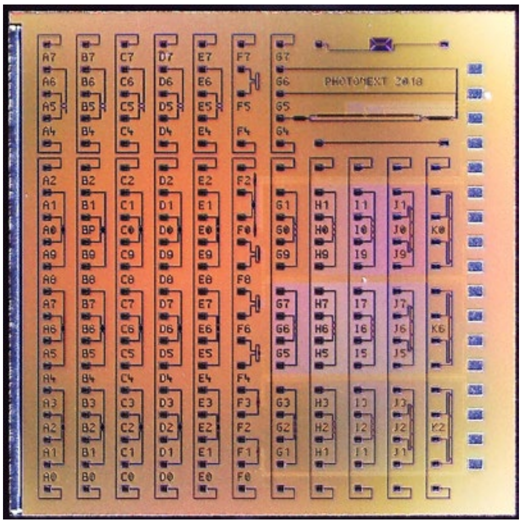

Fig.1: (a) Optical microscope image of the fabricated chip.

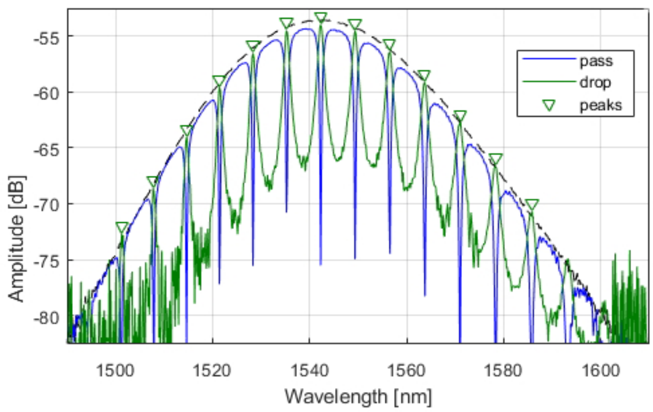

Fig.1: (b) measured response of exemplary add-drop ring resonator.

Description

The ever-growing amounts of traffic pushed by data-center interconnections and hungry-bandwidth applications in the access networks is requiring always greater capacity in telecom operators' networks. In this context, the elastic optical networks (EON) represent a feasible solution to provide flexible-grid switching capabilities thanks to the use of silicon photonics based architectures. The final goal of these EON is to achieve highly tunable and bandwidth-variable switching elements often by cascading micro ring resonators (MRRs). The latter are commonly referred as building blocks in larger architectures.

Based on the flexible-grid switching architectures for EON, the chip shown in Figure 1 is the first silicon photonics design fully developed in Politecnico of Torino within the FlexNet project. This project aims at the study of MRRs based optical circuits, from the theoretical analysis to the design and the practical characterization in laboratory.

The simplest MRRs blocks of the chip allow to evaluate their characteristic optical properties, comparing them with the design ones.

Additional blocks are based on cascaded MRRs, whose bandwidths have been designed to satisfy the requirement of the flexible grid application. In particular, the designed architecture was optimized for signals with spectrum slices of 12.5 GHz and a nominal central frequency granularity of 6.25 GHz. This characteristic enables elastic optical networks to support optical connections with almost arbitrary bandwidths.

A future development of this activity is the design and realization of a flexible network consisting of an input port, a through port and multiple drop ports, with different bandwidth, thermally tuned at different peak wavelengths to match incoming optical signals.

In the realized design, we exploited the flexibility of the imec active platform to insert additional components, such as photodiodes, Mach-Zender interferometers and thermally tuned resonators, which allowed us to gain further knowledge on the design of these building blocks and are also used for educational purposes in the framework of Politecnico's teaching activities.

Why EUROPRACTICE?

The EUROPRACTICE consortium provides accessible access to foundry services to research institutions that could otherwise not easily support regular fabrication costs. Politecnico di Torino is part of EUROPRACTICE membership and the services of the imec center are offered by EUROPRACTICE in the field of research in silicon photonics.

The available component library of imec ISiPP50G and its consolidated process design kit (PDK) represent an up-to-date technology for silicon photonics devices, helping the researchers to simplify and to improve the prototyping of active and passive devices by ensuring final top-quality. Being this the first silicon photonics chip developed at Politecnico, we really appreciated EUROPRACTICE and imec continuous technical support at every step of the chip design process. Finally, EUROPRACTICE training courses provided an additional opportunity of interaction with imec which significantly speeded up the development of the chip.

Acknowledgements

The FlexNet project was made possible by the EUROPRACTICE and its "Stimulation Action for VERY FIRST USERS in Si-Photonics" which is part of the EUROPRACTICE 2016 project funded by the European Commission. Hence, the Authors would like to thank EUROPRACTICE for the grant they received for the prototype fabrication of the chip.

The chip was designed with the IPKISS Design Framework by Luceda Photonics; the Authors thank Dr. Pierre Whal and his colleagues for the continuous technical support.

The testing part of the FlexNet project was supported by the PhotoNEXT Interdipartimental Center of Politecnico di Torino, thanks to the new probing station for silicon photonics equipped with Physik Instrumente Fiber Alignment System F-712.HA2.

A 4-channel true time delay optical beamforming network for mmWave applications

Photonics Research Group / IDLab,
Department of Information Technology (INTEC),
Ghent University – imec, Belgium

Contacts: Laurens Bogaert, Johan Bauwelinck, Gunther Roelkens
E-mail: Laurens.bogaert@ugent.be
Technology: Tyndall packaging + imec Si-Photonics Passives
Die Size: 6mm x 3mm (Full wafer to allow for post-processing)

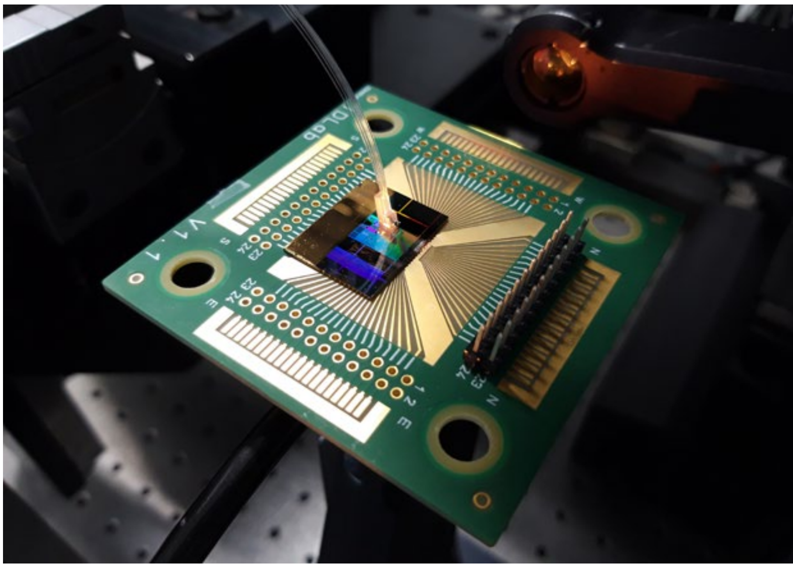

Fig.1: Packaged optical beamforming network

Description

Next-generation wireless networks will require increasingly faster data links. One of the key enablers is the shift towards higher frequency bands, e.g. the mmWave range. These parts of the spectrum offer large portions of contiguous bandwidth and are significantly less congested than traditional communication bands. Another key enabler is beamforming, which benefits from the scaling of antenna dimensions resulting from the migration to mmWave frequencies to allow for antenna arrays in a small form factor. Beamforming helps to overcome the increased path losses experienced at high frequencies. Additionally, it reduces the interference to other users allowing for spatial multiplexing of communication channels resulting in an increase of the system capacity.

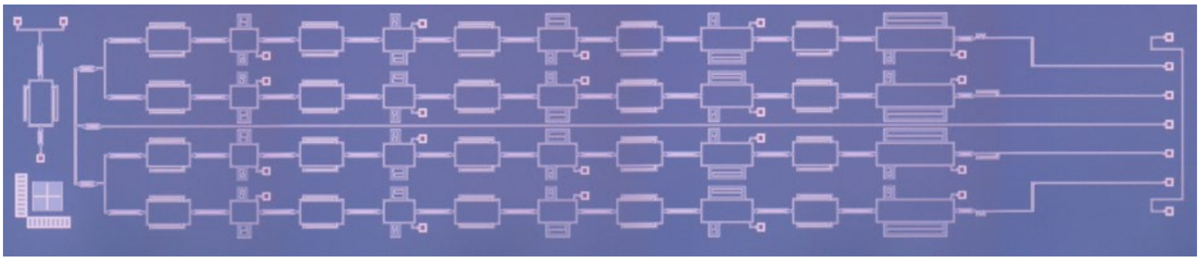

Fig.2: 4-Channel true time delay optical beamforming network before post-processing

This work demonstrates the implementation of a true time delay optical beamforming network (OBFN) for a 4-element antenna array. The design is based on switchable optical delay lines and offers a 5-bit tunability of the delay for each antenna element with a resolution of 1.6 ps.

Highlights

- Four channel true time delay OBFN
- 5-bit tunable delay cells with 1.6 ps resolution (thermal tuning)
- Packaged device: pin header for biasing of heaters and fiber array for optical I/O

Why EUROPRACTICE?

For the fabrication of our photonic devices we use EUROPRACTICE as it offers affordable MPW services. Furthermore, we relied on the packaging services provided by Tyndall National Institute to add a fiber array to the assembly resulting in a connectorized device that can easily be used in link experiments.

Acknowledgements

This work was funded by the Ghent University special Research Fund (BOF14/GOA/034). We would also like to thank M. Muneeb for his help with the post-processing of the passive silicon photonics wafer.

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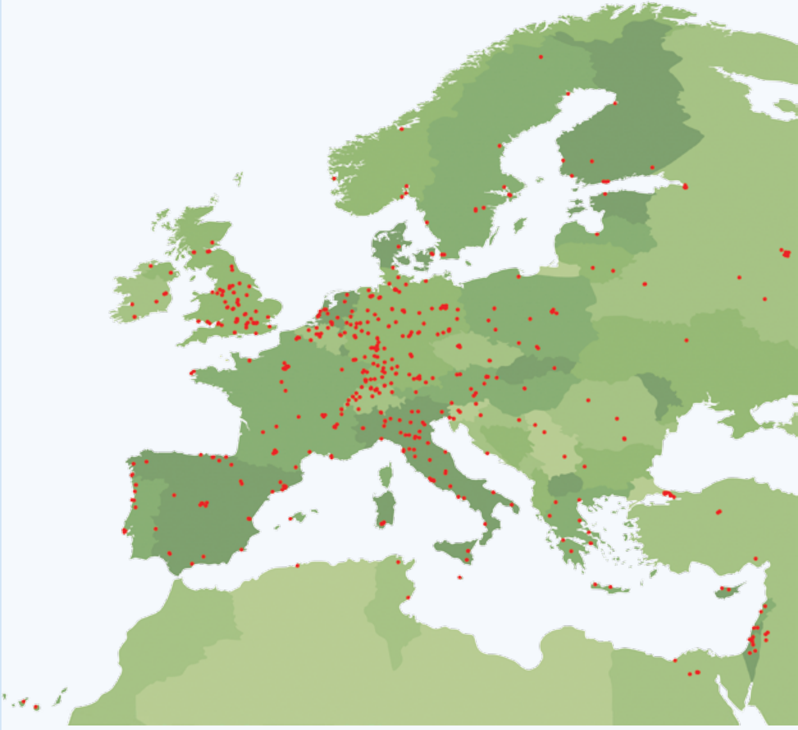

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A37550	National and Kapodistrian University of Athens
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A35300	University College Cork
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A13330	Technion - Israel Institute of Technology
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A13920	Bar-Ilan University
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A00740	Università degli Studi di Perugia
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R20670	Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari
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R21190	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali del Gran Sasso
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R22200	Radio Analog Micro Electronics srl
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R22410	Instituto Nazionale di Fisica Nucleare Sezione di Catania

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A47650	American University of Beirut

Lithuania

A47980	Vilniaus Universitetas

Malta

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R21460	SINTEF Stiftelsen for industriell og teknisk forskning

Palestine

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Poland

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A40120	Politechnika Warszawska
A40130	Politechnika Lódzka - Mikroelektroniki I Technik Informatycznych (DMCS)
A40140	Akademia Górniczo-Hutnicza im. Stanislawa Staszica
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A40160	Politechnika Wroclawska
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R40030	Siec Badawcza Lukasiewicz - Instytut Technologii Elektronowej
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Portugal

A12310	Universidade Nova de Lisboa
A12550	Universidade do Minho
A13710	Instituto Superior de Engenharia de Lisboa
A35540	Universidade do Porto
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R14120	Instituto de Telecomunicações - Lisboa
R21710	Laboratório de Instrumentação e Física Experimental de Partículas
R21750	International Iberian Nanotechnology Laboratory
R21890	Instituto de Telecomunicações - Aveiro
R22170	Instituto de Sistemas Robótica (ISR-UC)

Romania

A15520	Universitatea Politehnica din Bucuresti
A15560	Universitatea Tehnică "Gheorghe Asachi" din Iaăi
A16070	Universitatea Transilvania Brasov
R49010	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Nuclear Hadrons
R49060	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Particle Physics

Russia

A40240	Vladimir State Technical University named after Alexander and Nikolay Stoletovs
A47330	St. Petersburg State Polytechnical University
A47520	National Research University of Electronic Technology (MIET)
A47790	St. Petersburg State University of Aerospace Instrumentation
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A60060	Mordovian State University named after N.P.Ogarev
A60080	Novosibirsk State Technical University
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A60160	Bauman Moscow State Technical University - Kaluga
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A60200	Rzhanov Institute of Semiconductors Physics
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Slovakia

A40050	Slovenská technická univerzita v Bratislave
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Slovenia

A40280	Univerza v Ljubljani
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South Africa

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A35891	Universidad de Cantabria
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R21700	MAX IV Laboratory
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R22050	Institutet för Rymdfysik
R22140	European Spallation Source ESS AB

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A13090	Università della Svizzera Italiana
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The Netherlands

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A12010	Vrije Universiteit Amsterdam
A12650	Radboud Universiteit Nijmegen
A14510	Rijksuniversiteit Groningen
A15420	Erasmus Universitair Medisch Centrum Rotterdam
A15960	Universiteit van Amsterdam
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R20370	TNO-FEL
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R20520	Stichting Nederlandse Wetenschappelijk Onderzoek Instituten / Stichting ASTRON, Netherlands Institute for Radio Astronomy
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Uzbekistan

A16380	Urganch State University
A16390	Andizhan State University

CONTACT INFORMATION

For **general information or enquiries** about EUROPRACTICE, please contact the project coordination team at imec.

imec

Romano Hoofman (general)
Tel: +32 (0) 16 283865

Paul Malisse (operational)
Tel: +32 (0) 16 281272
E-mail: mpc@imec.be

Wendy Fannes (legal)
Tel: +32 (0) 16 281571
E-mail: epsec@imec.be

For enquiries about EUROPRACTICE **academic membership, design tools or training courses**, please contact the Micro-electronics Support Centre, UKRI-STFC Rutherford Appleton Laboratory, on:

UKRI Science and Technology Facilities Council

Mark Willoughby (design tools)
Tel: +44 (0) 1235 445327
E-Mail: MicroelectronicsCentre@stfc.ac.uk

Clive Holmes (training courses)
Tel: +44 (0) 1235 445327
E-Mail: MicroelectronicsCentre@stfc.ac.uk

Richard Bishop (academic membership)
Tel: +44 (0) 1235 445327
E-Mail: MicroelectronicsCentre@stfc.ac.uk

For enquiries about EUROPRACTICE **smart system integration**, please contact Smart Systems Integration service center:

Tyndall National Institute

Ramsey Selim (general)
Tel: +353 21 234 6613
E-mail: europractice.gateway@tyndall.ie

For more specific enquiries concerning **technology access, MPW schedules, and related customer support**, please contact one of the following EUROPRACTICE support centers.

imec

ON Semiconductor:
Greta Milczanowska
Tel: +32 (0) 16 281274
E-mail: Greta.Milczanowska@imec.be

TSMC Technologies
Tobias Vanderhenst
Tel: +32 (0)16 287889
E-mail: eptsmc@imec.be

UMC Technologies
Erwin Deumens
Tel: +32 (0)16 281930
E-mail: epumc@imec.be

X-FAB & MEMS Technologies
Pieter Claes
Tel: +32 (0)16 288770
E-mail: epxfab@imec.be

Si-Photonics Technologies
Mateo Aranda Moran
Tel: +32 (0)16 283045
E-mail: epsiphot@imec.be

SiN-Photonics Technologies
Adil Masood
Tel: +32 (0)16 288054
E-mail: sinmpw@imec-int.com

Fraunhofer IIS

ams Technologies
Wolfgang Marxer
Tel: +49 (0)9131 776-4423
E-mail: virtual-asic@iis.fraunhofer.de

GLOBALFOUNDRIES Technologies
Vikas Vijaya Kumar
Tel: +49 (0)9131 776-4418
E-mail: virtual-asic@iis.fraunhofer.de

IHP Technologies
Elvira Liandres
Tel: +49 (0)9131 776-4464
E-mail: virtual-asic@iis.fraunhofer.de

X-FAB Technologies
Stefan Rudischhauser
Tel: +49 (0)9131 776-4422
E-mail: virtual-asic@iis.fraunhofer.de

GaN-IC Technology
Maritza Tangarife Ortiz
Tel: +32 (0)16 281372
E-mail: ganmpw@imec-int.com

cmp

ams Technologies
Kholdoun Torki
Tel: +33-476 574615
E-mail: kholdoun.torki@mycmp.fr

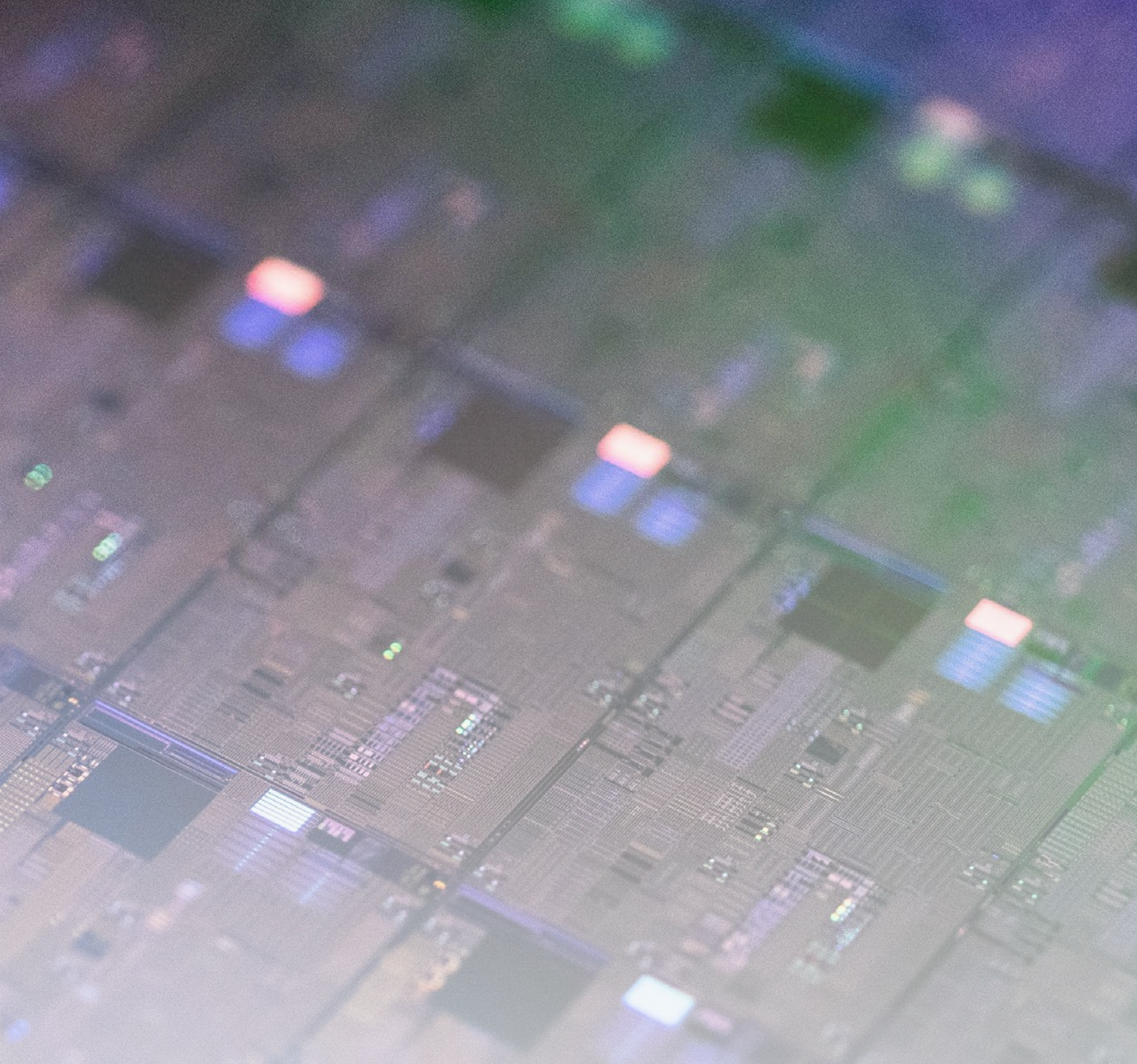
EM Microelectronic Technologies
Lyubomir Kerachev
Tel: +33-476 574834
E-mail: lyubomir.kerachev@mycmp.fr

ON Semiconductor Technologies
Kholdoun Torki
Tel: +33-476 574615
E-mail: kholdoun.torki@mycmp.fr

STMicroelectronics Technologies
Jean-Francois Paillotin
Tel: +33-476 574797
E-mail: jean-francois.paillotin@mycmp.fr

MEMS Technologies
Kholdoun Torki
Tel: +33-476 574615
E-mail: kholdoun.torki@mycmp.fr

Si-Photonics Technologies
Lyubomir Kerachev
Tel: +33-476 574834
E-mail: lyubomir.kerachev@mycmp.fr



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imec
General EUROPRACTICE-IC office & IC Manufacturing Center
p.a. P. Malisse
Kapeldreef 75
B3001 Leuven, Belgium
Tel: +32 16 281 272
E-mail: mpc@imec.be
http://www.europractice-ic.com

UKRI-STFC
Microelectronics Support Centre – EUROPRACTICE EDA tools and training office
p.a. Dr. J.A. McLean
Rutherford Appleton Laboratory
Didcot, Oxfordshire, OX11 0QX, United Kingdom
Tel: +44 (0)1235 44 5327
E-mail: MicroelectronicsCentre@stfc.ac.uk
http://www.europractice.stfc.ac.uk

Fraunhofer IIS
IC Manufacturing Center
p.a. T. Drischel
Am Wolfsmantel 33
D91058 Erlangen, Germany
Tel: +49 9131 776 4463
E-mail: virtual-asic@iis.fraunhofer.de
https://www.iis.fraunhofer.de/en/ff/sse/icd/leist/found.html

CMP
IC Manufacturing service center
p.a. K. Torki
46, Avenue Félix Viallet
F-38031 Grenoble, France
Tel: +33 476 574 617
E-mail: cmp@mycmp.fr
https://mycmp.fr/

Tyndall National Institute
Smart Systems Integration service center
p.a. M. Mora
Maltings Complex Dyke Parade,
Cork, T12 R5CP, Ireland
Tel: +353 21 234 6097
E-mail: europractice.gateway@tyndall.ie
https://www.tyndall.ie/packaging

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