IMEC Free Mini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuit: SUBCIRCUITS FOR BLUETOOTH LOW-ENERGY RECEIVER

Adviser Professor(s)
Prof. Wilhelmus Van Noije

Students involved (names and aimed degrees)
1 - Fellipe Sola - Master Student
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3 - Daniele Santana - Master Student
4 - Thiago Alves Amaral - Master Student
5- Hugo Hernandez - Professor at UFMG

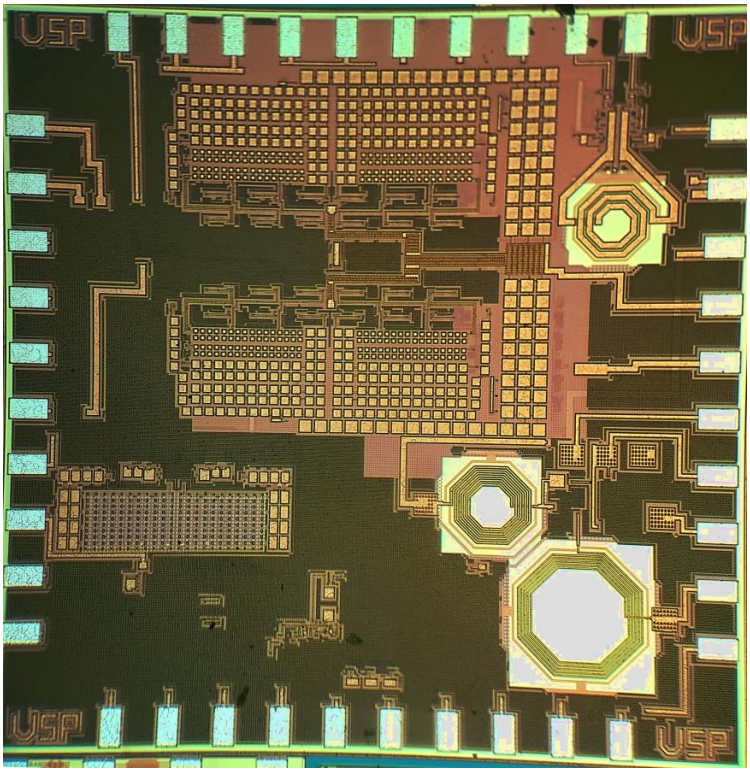
Institution (University/Faculty):
Polytechnic School of the University of São Paulo - Electrical Engineering

Type of Circuit Design: ( ) Digital; (X) mixed signal; (X) analog; (X) RF

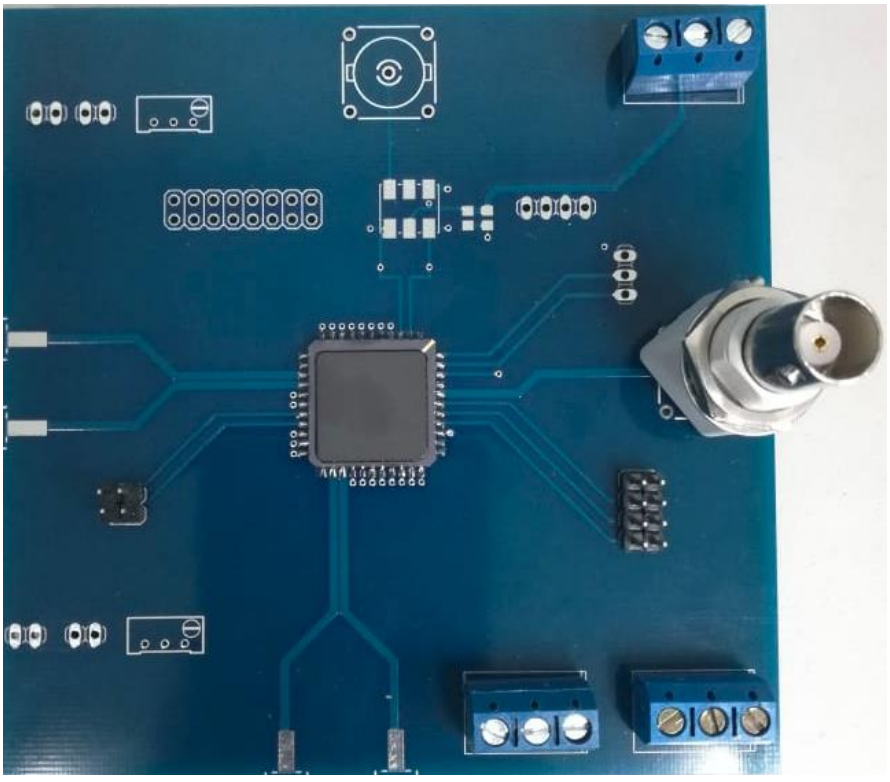
Date of the circuit tape-out of the run: 23/09/2018
Date of receiving the chips at your institution: 10/01/2019

Short description of the circuit: (function, proposed innovation, number of transistors, passive components, screenshot of the chip layout, etc.)

Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc.



(a)



(b)

Figure 1. (a) Microphotograph of the manufactured chip; (b) PCB developed to test the circuits on the chip.

A. A 0.5V Switched Capacitor Digital Low Dropout Regulator

This work presents the design of an 0.5V digital LDO in 180nm CMOS technology for Dynamic Voltage Scaling applications. The proposed digital LDO is based on the topology name of SCR-LDO .
The basic schematic diagram of the designed SCR-DLDO is shown in Figure 2. The circuit is composed of a dynamic comparator, a D flip-flop in bi-stable configuration, a switched capacitor resistor, and a two-phase non-overlapping clock generator. An external 0.5V stable voltage is used as reference. The output (Vout) and the reference voltage (Vref) are compared by the dynamic comparator. In the event that Vout is less than Vref, the pulsed signal will be generated on the comparator output which will switch the flip-flop state, if Vout is more than Vref the D flip-flop is not pulsed and as a consequence, the output capacitor (Co) is not switched. The lip-flop output is connected to the two-phase non-overlapping clock (φa and φb) which turn-on/off switches (PMOS transistors) of the switched capacitor resistor. The SCR-DLDO was designed to operate with a typical clock frequency of 200MHz.
The output ripple (ΔVout) in the SCR-DLDO can be reduced by a factor M by time-interleaving M unit SCR cells. A M=4 factor was chosen in this work and the schematic diagram is presented in Figure 3. ΔVout nominally increases linearly with Vdrop. Therefore, the amount of charge transfer capacitance (Co) can be scaled by a similar factor to the Vdrop (Vout - Vin) increase, without reducing the load current handling capability.
A Binary Ripple Control (BRC) circuit was used to divide the capacitance and the switched capacitance resistance of each of the 4 interleaved phases into 5 binary-weighted banks. These are enabled by EN[4:0] signal which can be controlled by an external battery state-of-charge monitoring circuit. A redundant LSB bank is always on. The schematic of the BRC circuit is shown in Figure 4 which in composed in total by 32 SCR unit cells. The Co value selected in this work was around 154pF implemented as a MIM capacitor M6-M5 available in the 180nm technology.
Figure 4 shows the simulation result of the output voltage response to the Vref step with maximum current load (1.5mA) and minimum load (200uA) operating at 200MHz clock frequency and input voltage of 0.6V. A typical settling time of around 100ns was obtained for both load current cases. Off-chip capacitance was not included.

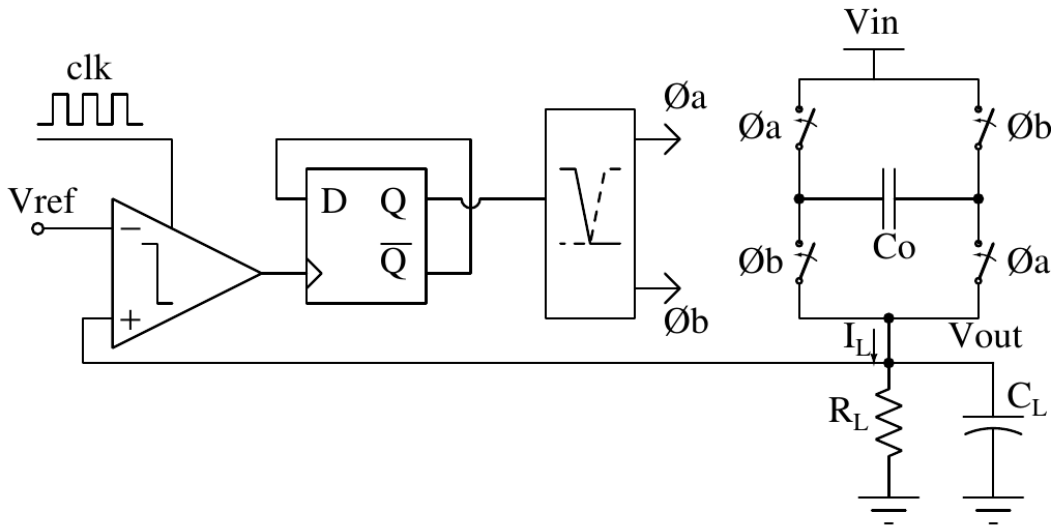


Figure 2. Schematic diagram of the designed SCR-DLDO

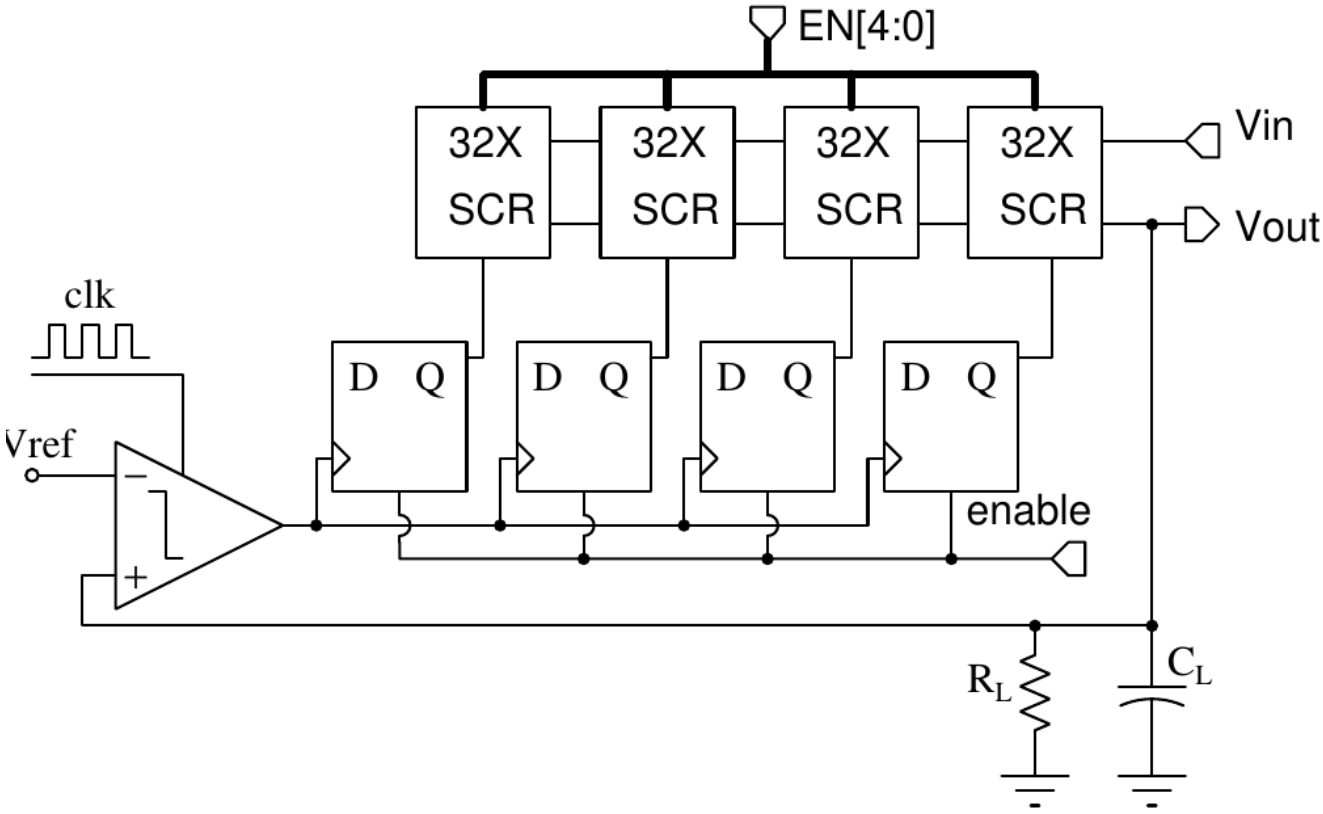


Figure 3. Schematic diagram of the designed SCR-DLDO with Binary Ripple Control

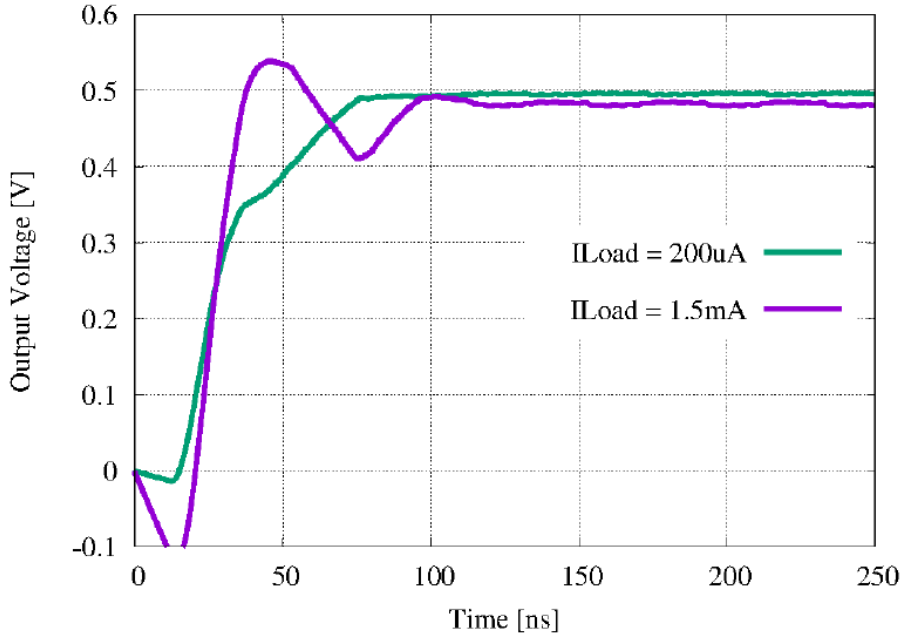


Figure 4. simulation result of the output voltage response to the Vref step

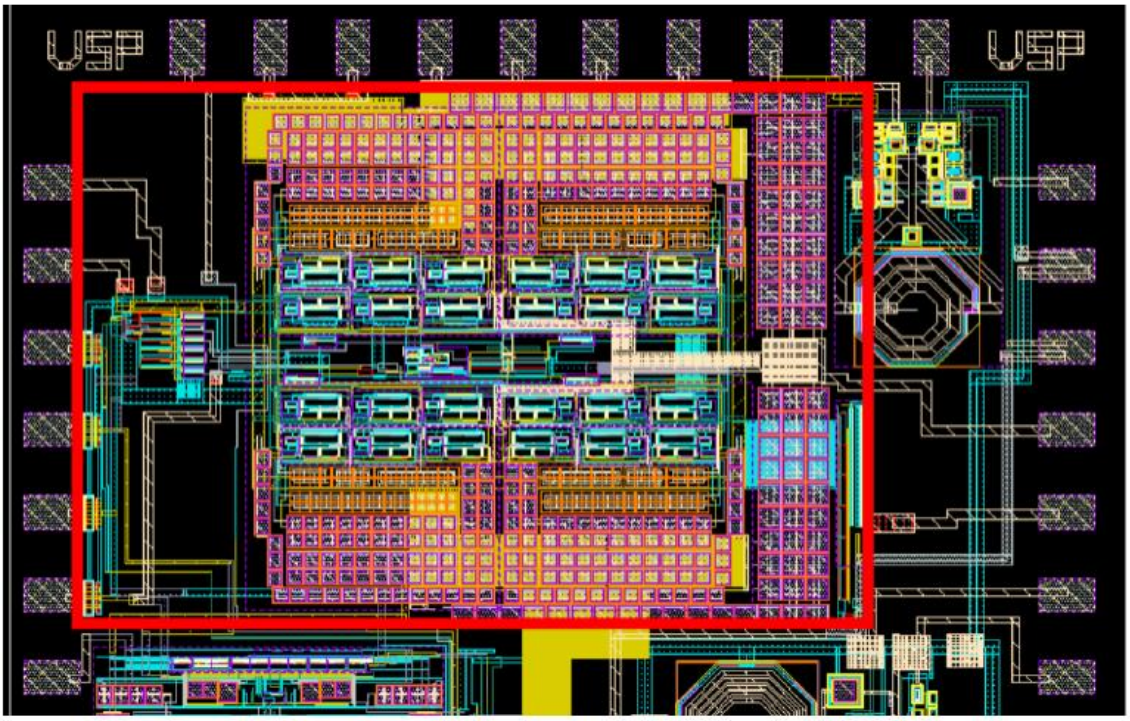


Figure 5. Layout of the 0.5V Digital LDO.

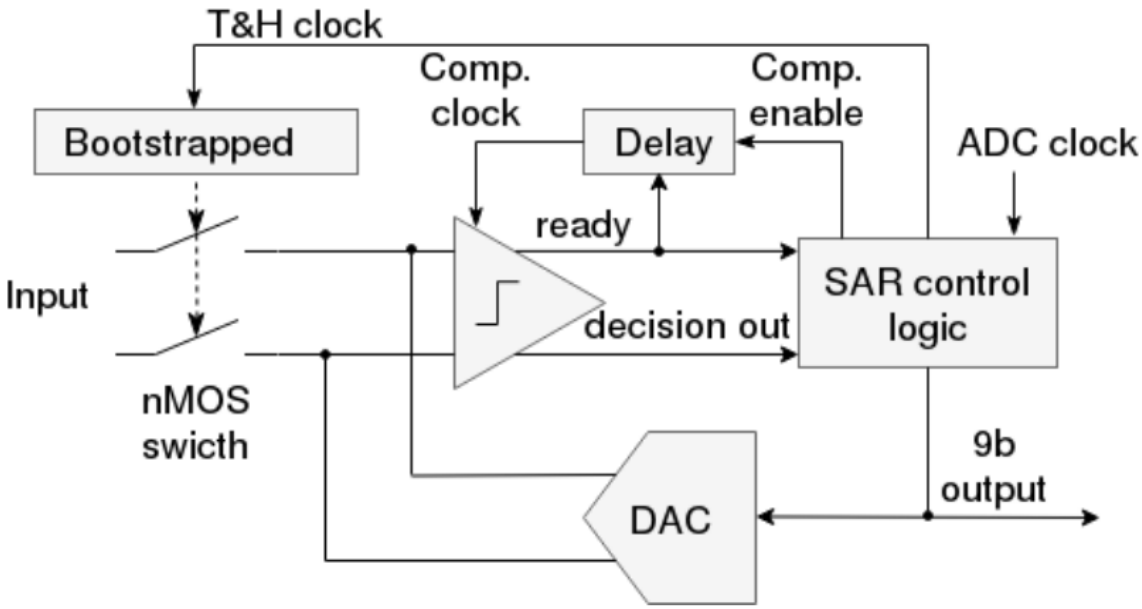
B. A 1.8V 9bit 10MS/s SAR ADC in 0.18µm CMOS for bioimpedance analysis

This work proposes the design of a 9-bits low power 10MS/s asynchronous SAR ADC in 180nm CMOS technology.

Figure 6 illustrates the block diagram of the designed SAR ADC. A differential architecture was used to have a good common-mode noise rejection. It is composed by a dynamic comparator, an asynchronous SAR digital logic, two bootstrapped switches and 9 bits capacitive split-array DAC (6 MSB and 3 LSB). The maximum sampling frequency of the ADC is 10 MS/s. The ADC has two operation phases (1) sampling and (2) decision. In the sampling phase the input differential signal is stored on the top plates of the capacitor array and during the decision phase the successive approximation process is performed from MSB to LSB bits solution. The decision phase starts after the falling edge of the sampling clock and it takes 9 clock cycles to determine the digital representation of the analog input.

The ADC remains in the sampling-hold after the decision phase until the next falling edges of the sampling clock. The end-of-conversion signal will be enabled (high) when the output data is ready and disabled (low) by the rising edge of the sampling clock. The merged capacitor switching strategy or the set and down scheme lead to a significant reduction of the DAC power consumption. However, these strategies use a common voltage reference which requires an extra LDO and more on-chip decoupling structures.

The prototype was designed using 0.18µm CMOS technology. Figure 8 shows the SAR ADC layout. The total area of the SAR ADC is 0.124mm2 with 523µm of width and 238µm of length. Figure 9 shows the measured FFT spectrum with an input frequency of close to 1MHz at 1.8V supply and a 10MS/s sampling rate. The measured SNDR and SFDR are 55.29dB and 63.37dB, respectively. The SFDR represents the ratio in dB of the value of a full scale sine wave signal to the highest spurious, a value of SFDR obtained demonstrates a good linearity of the ADC.



Proposed SAR ADC architecture

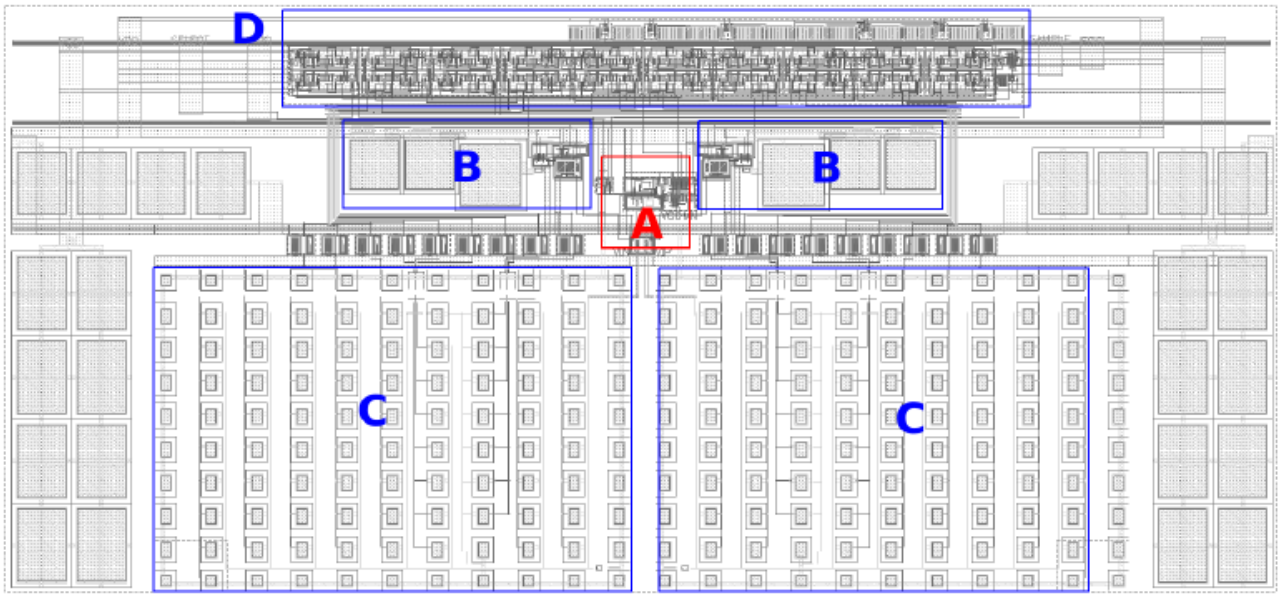


Figure 8. Layout of the SAR ADC

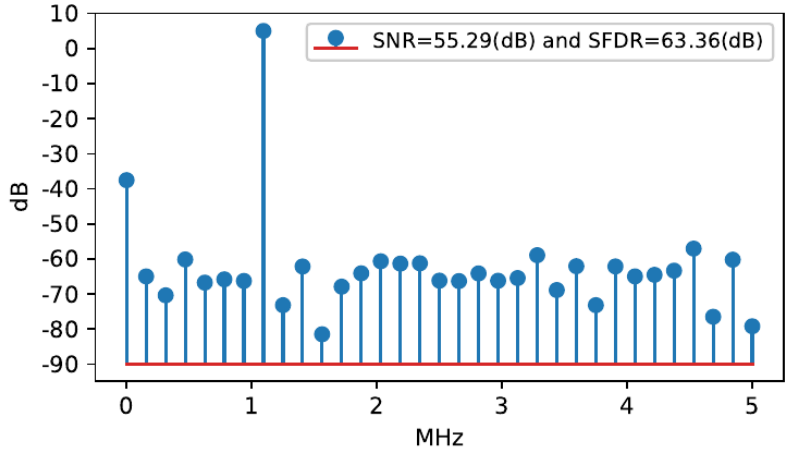


Figure 9. Measured spectrum at 1MHz and 10MS/s

C. A 0.5V LNA for Bluetooth Low Energy in 180nm CMOS

This work proposes the design of a 0.5V Low Noise Amplifier (LNA) for the Bluetooth Low Energy (BLE) network in 180nm CMOS technology.
The low energy profile of the BLE protocol helps with the implementation of low consuming radio applications in CMOS technology. The use of a reduced power supply voltage, allied with techniques for the development of low power topologies result in a significant reduction on the overall power consumption of such systems.
Figure 10 shows the schematic of the proposed circuit, which includes a LNA using a cascode common source with inductive source degeneration topology. The chosen topology is compatible with the optimal noise reduction. Also it allows the operation with the proposed 0.5 V supply. Due to the high threshold voltage (Vth) values simulated for the 180nm TSMC technology used, a technique of Forward Bulk Biasing (FBB) is performed, increasing the bulk to source voltage (Vbs), resulting in an Vth reduction.
The LNA has a narrow-band operation realized by the reactive input matching and LC tank load, helping with off-band filtering for the BLE protocol specified frequency band (2400 - 2483.5 MHz).
Figure 11 shows the layout developed for the LNA. The source inductance used in the input matching network is composed by the bonding wire inductance. The gate and drain connected inductors are integrated, as shown in figure 10. The layout occupies an 550 x 540 um area, and is in compliance with DRC, LVS rules, and also mutual inductance effects.
The design includes a nMOS source-follower buffer, used to interface the LNA with the 50-ohm input testing equipment.

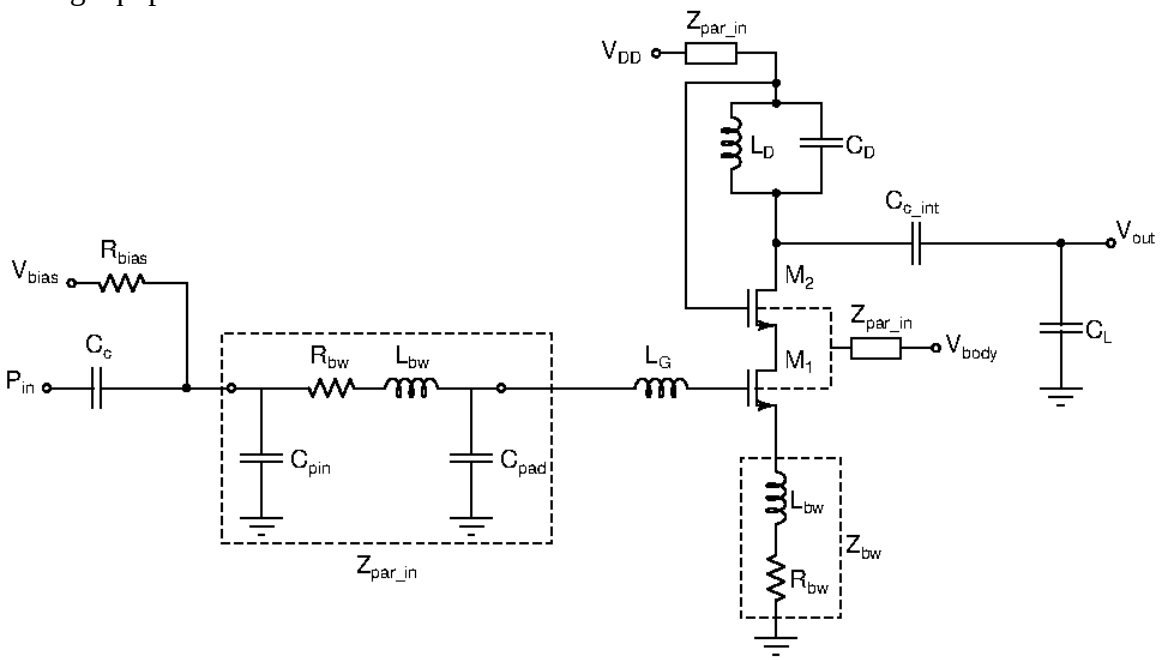


Figure 10. Cascode common source LNA with inductive source degeneration

Figure 12 shows the scattering parameters (S-Param) measurement for the LNA, showing the expected gain result, along with input and output band filtering.

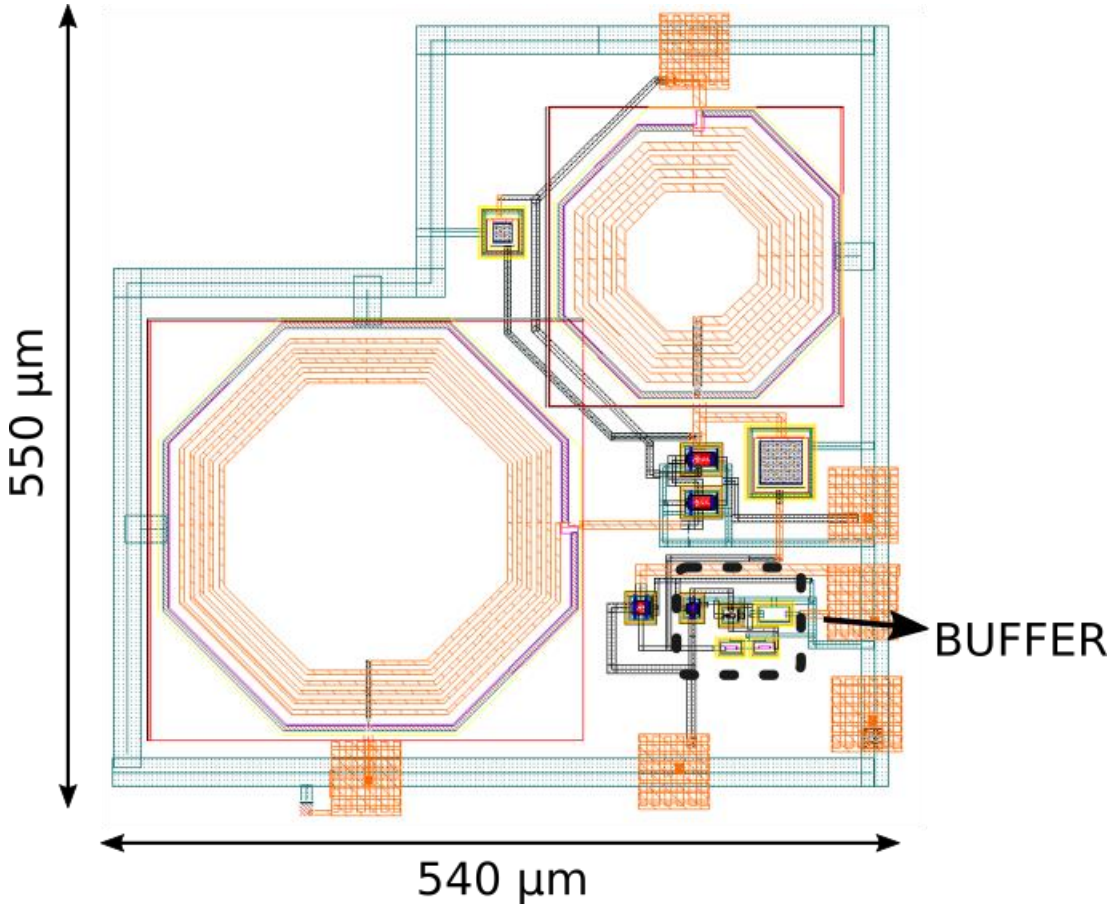


Figure 11. Layout of the LNA including input matching gate inductor and load inductor.

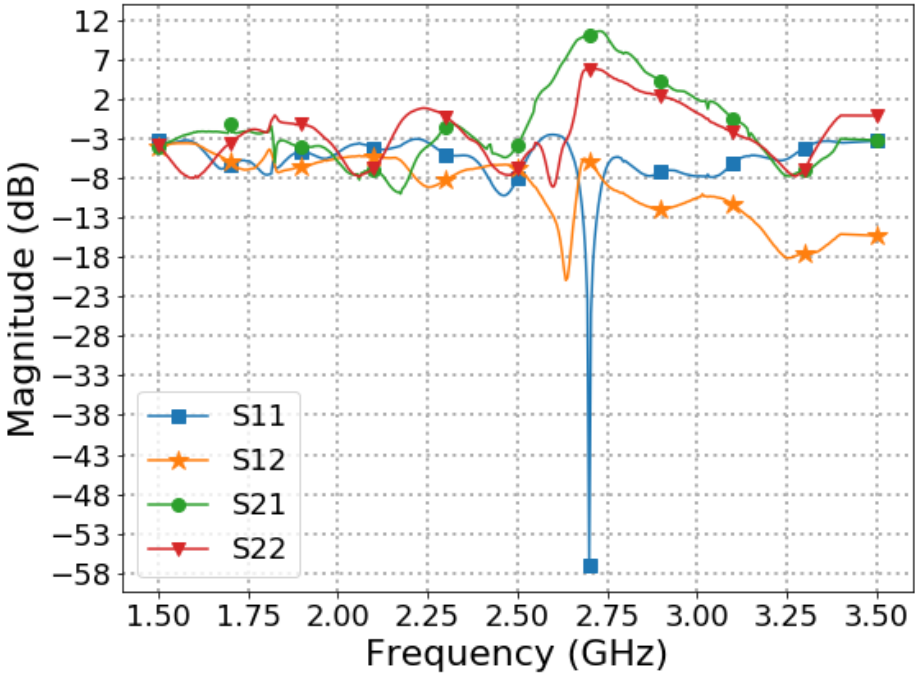


Figure 12. S-param measured results using corrected input matching.

D. A 1V 5 GHz Class-C Voltage-Controlled Oscillator (VCO) in 180nm CMOS

This work proposes the design of a 1V Class C VCO in 180nm CMOS technology to generate a reference signal of 5GHz. The use of a reduced power supply voltage and the use of techniques for the development of low power topologies result in a significant reduction on the overall power consumption of such systems.

Figure 13 shows the schematic of the proposed VCO.

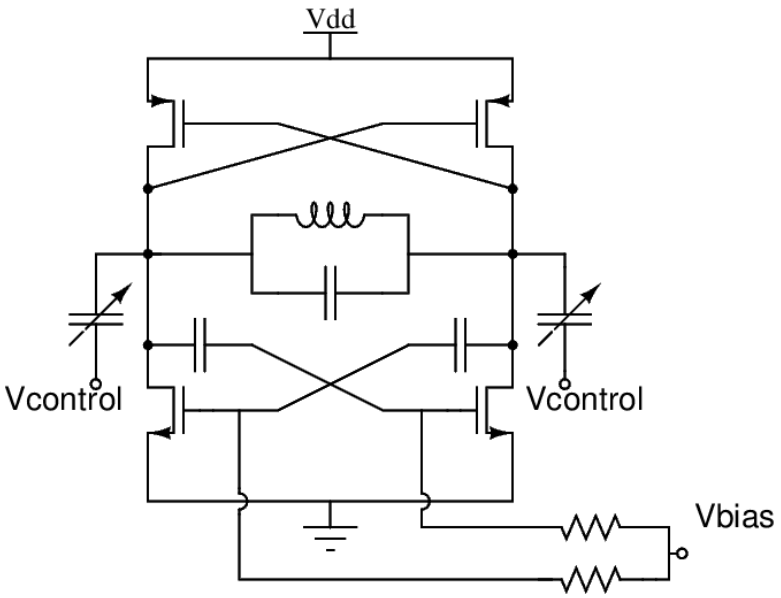


Figure 13. Class-C VCO schematic.

This VCO uses a cross-coupled topology with current reuse, which allows a lower current consumption, also to operate with only 1V a Forward Bulk Biasing (FBB) technique is performed, increasing the bulk to source voltage (Vbs), resulting in an Vth reduction. The layout, shown in Figure 14, occupies an area of 390 x 240 um^2.

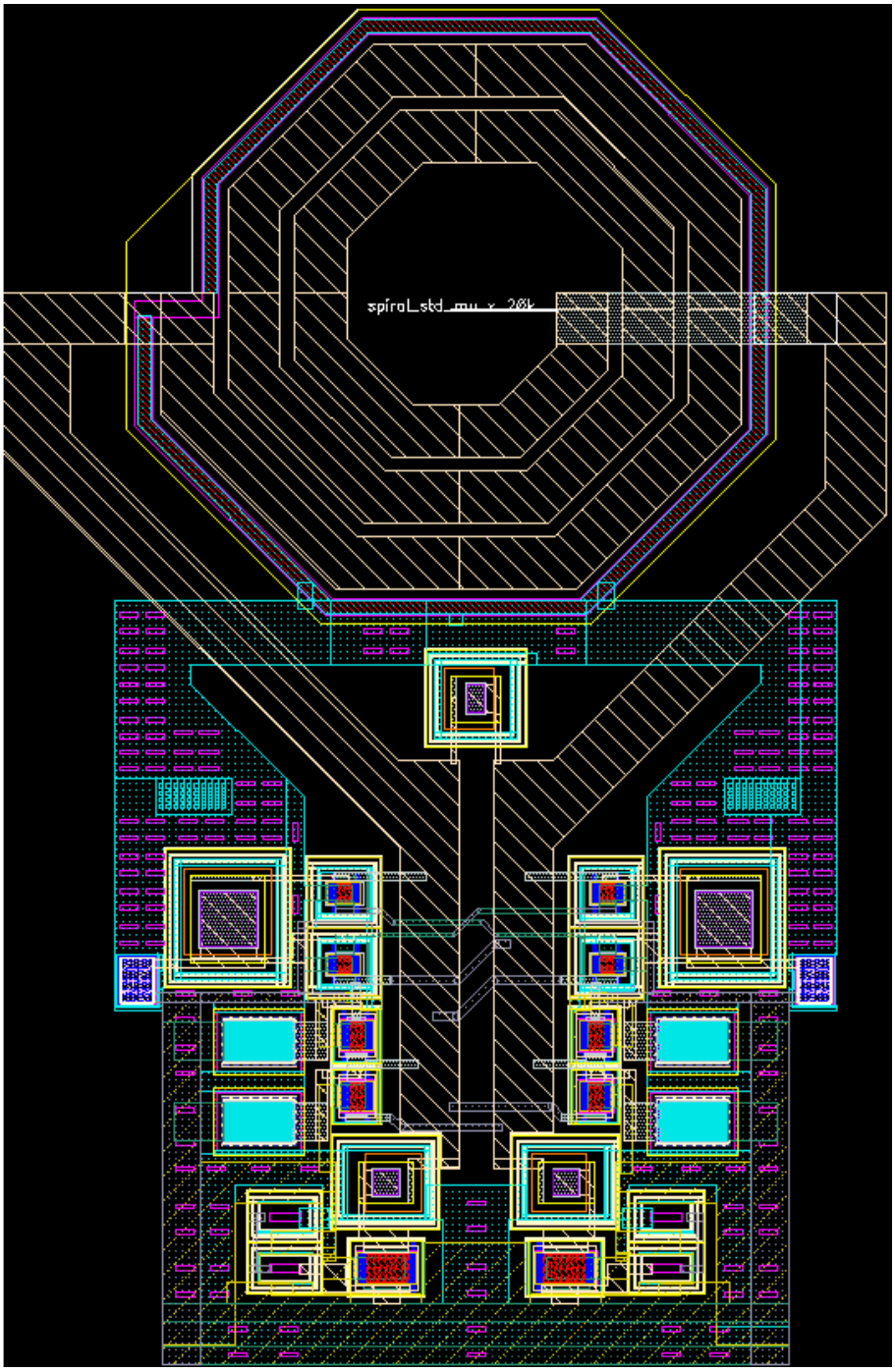


Figure 14. Class-C VCO layout.

Figure 15 shows the spectrum measurement for the VCO, showing the existence of a signal around 5GHz.

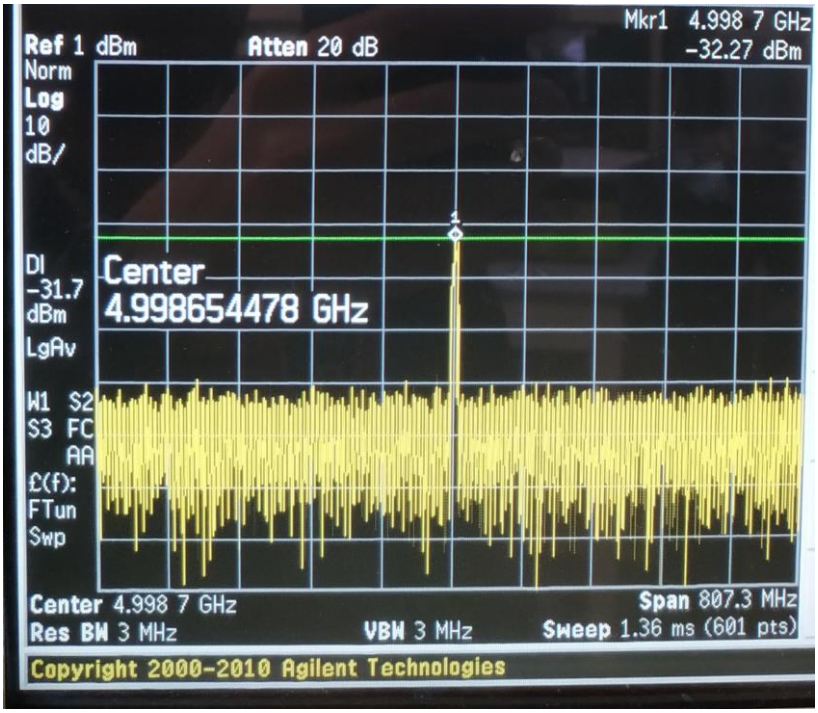


Figure 15. Measured spectrum.

Table 1 shows the comparison between the layout extracted and the fabricated VCO.

	Schematic	Fabricated
Vdd	1 V	1 V
Vbias	0.5 V	0.5 V
Power consumption	2.8mA	3mA
Signal Power @5GHz	-20dBm	-32.3dBm
Frequency for Vcontrol @0V	5.8GHz	5.45GHz
Frequency for Vcontrol @1V	4.7GHz	4.5GHz
VCO gain	1.1GHz/V	950MHz/V

Table 1. Comparison between the layout extracted and the fabricated VCO

Resulted publications (submitted, accepted or published) and degrees earned by students.

a) Publications:

1. Hugo Hernandez, Lucas Severo, Wilhelmus Van Noije: 0.5V 1OMS/S 9-Bits Asynchronous SAR ADC for BLE Receivers in 180nm CMOS Technology. In: 31st IEEE International System on Chip Conference (SOCC), 2018. Arlington, VA, USA, 4-7 Sept. 2018. **Electronic ISBN:**978-1-5386-1491-4.DOI: 10.1109/socc.2018.8618510. Pages: 314 - 317.
2. AMARAL, T. A. M.; HERNANDEZ, HUGO; NOIJE, WILHELMUS A. M. V.: A 0.5V Switched Capacitor Digital Low Dropout Regulator. In: IEEE International Conference On Electrical, Communication, Electronics, Instrumentation and Computing (ICECEIC - 2019),

2019, Enathur, Tamil Nadu, India. International Conference On Electrical, Communication, Electronics, Instrumentation And Computing. USA: IEEEXplore, 2019. p. 1-3.

3. SANTANA, D. ; HERNANDEZ, H. ; W. van Noije: A 1.8V 9bit 10MS/s SAR ADC in 0.18µm CMOS for bioimpedance analysis. In: LASCAS 2019 - Latin American Symposium on Circuits and Systems, 2019, Armenia, Quindio, Colombia. LASCAS 2019 - Latin American Symposium on Circuits and Systems. USA: IEEEXplore, 2019. p. 1-4.
4. Lucas Severo, Wilhelmus Van Noije: A Generic Test Board for the Electrical Characterization of ULP and ULV Balanced Amplifiers and Active Filters. In: EMicro 2019 - 21ª Escola Sul de Microeletrônica, e 34º Simpósio Sul de Microeletrônica. Pelotas, RS. SBC - Sociedade Brasileira de Computação, 2019. Received the Best Paper Award of EMicro 2019 - 21ª Escola Sul de Microeletrônica, e 34º Simpósio Sul de Microeletrônica, 2019.
5. Lucas Compassi-Severo, Wilhelmus Van Noije: A 0.4-V 10.9-µW/Pole Third-Order Complex BPF for Low Energy RF Receivers. In: **IEEE Transactions on Circuits and Systems I: Regular Papers** (Volume: 66, Issue: 6, June 2019). **DOI:** 10.1109/TCSI.2019.2906206. **Print ISSN:** 1549-8328. **Pages:** 2017 - 2026.

b) Conclusion of Master/PhD degrees:

1. Roberto Rangel da Silva: Bluetooth Low Energy Rf Front-end for Low-Voltage Applications In CMOS Technology. Master Thesis. Polytechnique School of Engineering, USP, August 2019.
2. Lucas Compassi Severo: ULV and ULP active-RC filters combining single-stage OTA and negative input transconductance for low energy RF receivers. PhD Thesis. Polytechnique School of Engineering, USP, February, 2019.