IMEC FreeMini@sic Fabrication on TSMC 0.18 um Technology

Title of the Circuits:

i. A PWM Nie-Tan Type-Reducer Circuit for an Interval Type-2 Fuzzy Controller
ii. A ROIC for Infrared Focal Plane Array

Adviser Professor: Prof. Dr. Lester de Abreu Faria

Students involved (names and aimed degrees):
i. Gabriel Antonio Fanelli de Souza (Doctorate's degree), ii. Rodrigo Bispo dos Santos (Doctorate's degree); iii. Adilson Batista (Master's degree); iv. Luis Felipe Duarte (Master's degree)

Institution (University/Faculty): Instituto Tecnológico de Aeronáutica (ITA)

Type of Circuit Design: ( ) Digital; ( ) mixed signal; (X) analog; ( ) RF

Date of the circuit tape-out of the run:12/09/2018
Date of receiving the chips at your institution:07/01/2019
Date of the report and/or of later update:17/06/2019

Short description of the circuit: (function, proposed innovation, number of transistors, passive components, screen shot of the chip layout, etc.)

i. <u>A PWM Nie-Tan Type-Reducer Circuit for an Interval Type-2 Fuzzy Controller</u>

Based on the Nie-Tan type-reduction method, the circuit operates with current-mode inputs, representing the firing intervals of the rules applied by the inference engine, and generates a PWM output. By restricting the number of consequents, it is possible to create the PWM output directly, without the need for analog multiplier/divider circuits. This feature makes the circuit very simple, aiding in the design process, while the PWM output makes it suitable for the control of DC-DC converters, maximum power point trackers (MPPT) for energy generators and any switching applications. It is also very low power, enabling the use in power restrained environments, such as energy harvesting systems. The circuit was designed using the TSMC 0.18μm technology in CADENCE Virtuoso software and simulated for different combinations of input values, confirming its capabilities. It was also simulated as part of a type-2 fuzzy inference system with two inputs, nine rules, and having firing intervals represented by currents within 0 and 10μA. The proposed architecture requires three independent capacitors to integrate each current. Current mirrors are used to feed the integrators, and transmission gates control which currents are injected during each part of the cycle. Simple voltage comparators are used to implement the division corresponding to each half of the period, and transmission gates switch between them to create the PWM output signal.

ii. <u>A ROIC for Infrared Focal Plane Array</u>

This circuit consists of an analog modular noise rejection in infrared sensors signal conditioning. The acquisition, integration and sampling processes can be heavily affected by noise with different sources, which can hamper the sensors operation, given it can become saturated simply by the spurious signals. Sensors operating in the infrared region of the spectrum can have many applications in military, medical, industrial, and scientific research. In every application there is a need for high performance and high resolution. Its operating principle consists in a photodetector (sensor) which converts infrared radiation emitted from a target into an electric current (photocurrent), that in turn is converted to voltage through an integrator circuit (ROIC – Read Out Integrated Circuit). Among the many possible noise sources, the dark current has some peculiarities that separate it from the others. It is generated by the sensor even when no radiation is entering the detector and is in the order of picoamperes to nanoamperes and is thus difficult to measure. The proposed circuit has a current mirror module that performs the subtraction between the current from one cell in the sensor matrix and a noise reference. Therefore, in ideal conditions, the resulting signal is the photocurrent without the noise component.

Main results and representative performance data or curves, picture of the IC, does circuit function as expected, etc.

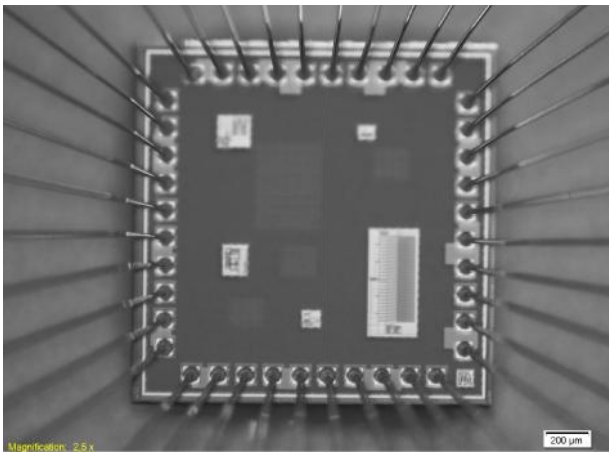
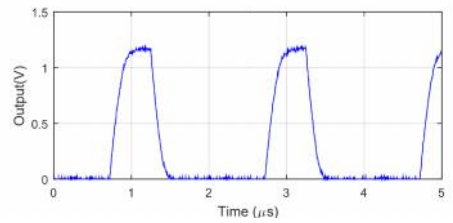
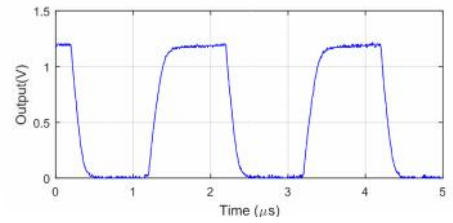


Fig. 1.





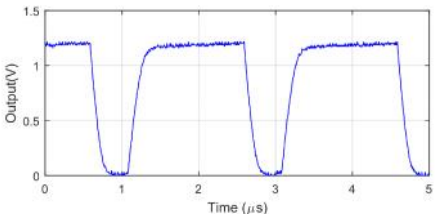


Fig.2

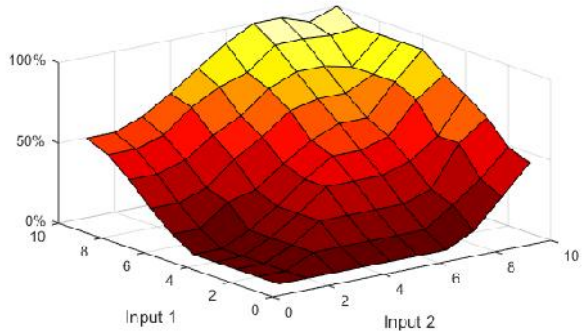


Fig.3

Fig. 1 shows the picture of the manufactured IC Prototype. Figs. 2-3 show the main results measured for the Nie-Tan Type-Reducer circuit. Fig. 2 displays different duty cycles associated with different combinations of input currents, for outputs with25%,50%, and 75%of duty cycle, while Fig. 3 shows the experimental result plot of the output surface of the Type-Reducer circuit in a complete type-2 fuzzy inference system with two inputs and nine rules. The measurements validated the circuits functionality and the measured average power consumption obtained was 53.8μW, confirming its low power characteristic.

Figs. 4-6 show the main results measured for the ROIC circuit. The ROIC has an integration capacitor that converts the current signal into voltage. At the end of one period, the capacitor has to be discharged, which is done by an NMOS transistor with the characteristics as measured in Fig.4.The integration voltage is connected to a PMOS transistor gate acting as a voltage follower, with the characteristic as measured in Fig.5. For a constant current after the noise subtraction process, the integration voltage is expected to increase linearly in the first half on the period and to retain its value in the second half, after which the capacitor is discharged and the cycle restarts, as shown in Fig. 6.

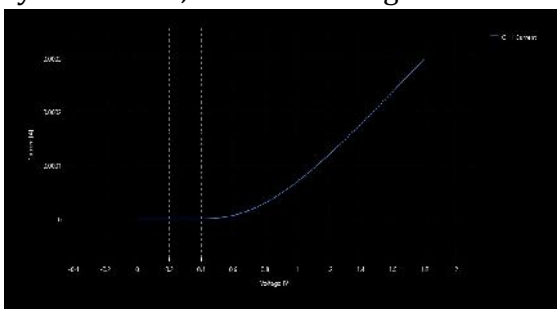


Fig.4

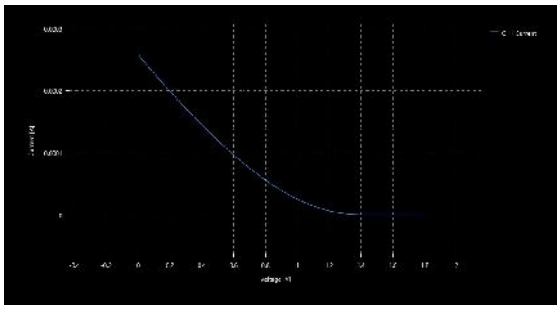


Fig.5

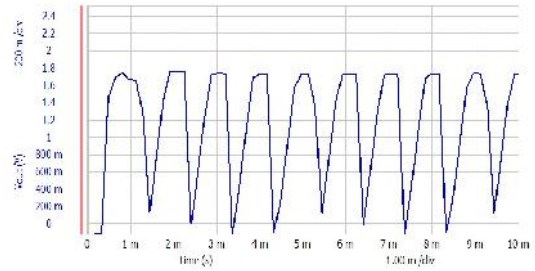


Fig. 6

Main challenges and difficulties encountered during design, submission, import process and measurements of the circuit.

The main challenge encountered once again was due to the import process. Although IMEC did not charge anything, the Brazilian Government charged high import taxes, which hampered the process, as the students and the advisorhad to pay with their own money.

Resulting publications (submitted, accepted or published) and degrees earned by students.

The previous results are currently being analyzed and are going to be part of the master's dissertation of Adilson Batista and of Luis Felipe Duarte, and the doctorate's Thesis of Gabriel Antonio Fanelli de Souza and of Rodrigo Bispo dos Santos. The results from the Fuzzy Type-2 Nie-Tan Type-Reducer Circuit are going to be part of a paper currently being written and expected to be submitted shortly.
Besides that, and although being part of the updating of the previous report, the following publications are part of the portfolio of this Institution, concerning to Free Mini-ASIC run with IMEC.

<u>Journals:</u>

1. *SOUZA, GABRIEL A.F. ; SANTOS, RODRIGO B. ; ROCHA RIZOL, PALOMA M.S. ; OLIVEIRA, DUARTE L. ; FARIA, LESTER A. . A novel fully-programmable analog fuzzifier architecture for interval type-2 fuzzy controllers using current steering mirrors. JOURNAL OF INTELLIGENT & FUZZY SYSTEMS, v. 34, p. 203-212, 2018.*
2. *FANELLI DE SOUZA, GABRIEL ANTONIO ; DOS SANTOS, RODRIGO BISPO ; DE FARIA, LESTER ABREU . Low-Power Current-Mode Interval Type-2 Fuzzy Inference Engine Circuit. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS, v. 1, p. 1-12, 2019.*
3. *FANELLI DE SOUZA, GABRIEL ANTONIO ; DOS SANTOS, RODRIGO BISPO ; DE FARIA, LESTER ABREU . Low Power Membership Function Generator for Interval Type-2 Fuzzy System . Journal of Inteligen fuzzy systems, 2019.*

Lester de Abreu Faria - Prof. Dr.
Advisor