ASIC PACKAGE DESIGN RULES

1 Bondpad dimension guidelines

Concerning the bondpads, there are some dimensions to be respected (figure 1 and table 1).

		ALTER Technology		SERMA Microelectronics	
		Standard	**Non-Standard**	**Standard**	**Non-Standard**
A	Minimum size of a bondpad on metal level for single bonding	Greater than 55µm x 55µm	Greater than 40µm x 40µm	Greater than 70µm x 70µm	Greater than 36µm x 36µm
B	Minimum size of a bondpad on metal level for double bonding	Greater than 110µm x 55µm	Greater than 80µm x 40µm	Greater than 140µm x 70µm	Greater than 72µm x 36µm
C	Minimum pitch between two adjacent bondpads	Greater than 65µm	Greater than 50µm	Greater than 80µm	Greater than 40µm
D	Minimum distance between a corner bondpad	Greater than 20µm	Greater than 20µm	Greater than 15µm	Greater than 15µm

Table 1: Standard and non-standard process rules for IC Assembly.

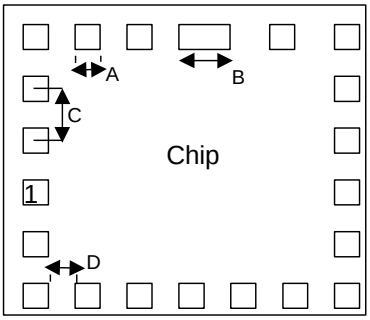


Fig. 1: Bondpads

2 Configuration of the bondpads and bondpins

2.1 Definitions

Bondpad : Pad on the chip to which the wire will be bonded
Bondpin : Areas of package on which the wire will be bonded
DIL : Dual-in-Line package
CLCC : Ceramic Leadless Chip Carrier
JLCC : J-Leaded Chip Carrier
CPGA : Ceramic Pin Grid Array
CSOIC : Ceramic Small Outline Integrated Carrier
SOIC : Small Outline Integrated Carrier (Open-Pack)
CQFP : Ceramic Quad Flat Pack
QFN : Quad Flat pack No leads (Open-Pack)

Note 1: Open-Pak packages are pre-molded open cavity plastic packages which feature a gold plated copper die attach pad and lead frame. They have the same mechanical and electrical characteristics as their transfer molded counterparts. The die thickness for Open-Pak plastic types may not exceed 280µm (11 mils). This has to be checked with the tape-out engineer responsible for the technology in question.

2.2 Remarks

1. Preferably, the bondpins are equally distributed along the 4 sides of the cavity on which the chip will be mounted.
2. Position of bondpin #1 (figure 2):

   In case of an odd number of bondpins on one side of the cavity, (ex. 17 in the case of a 68-pin carrier) pin #1 is in the middle of the row. In case of an even number of bondpins on one side of the frame (for ex. 48-pin DIL) pin #1 is the first pin counter clockwise from the middle of the row of pins. For the CPGA's, CQFP's and QFN's, bondpin#1 is located in the corner, generally starting upperleft bondpad and counting counter clockwise.
3. For ceramic packages, bondpin #1 can also be recognized by the bevelled edge.

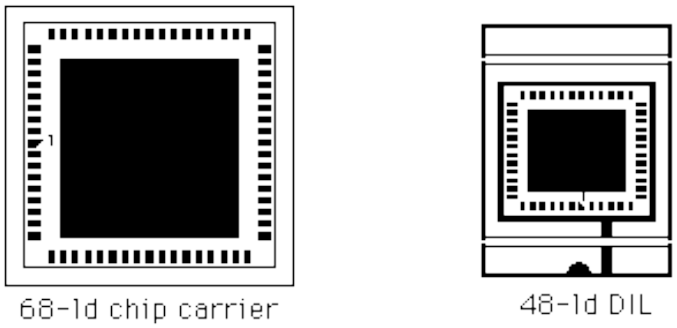


Fig. 2: Position of bondpin #1

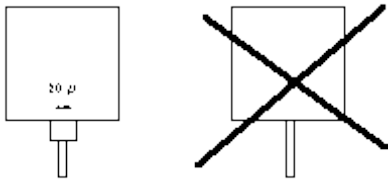
2.3 Guidelines

1. It is highly recommended for the bondpads to be equally distributed along the four sides of the chip
2. Minimum ratio of length/width of the chip: 1:2
3. Max. size of the chip as designed (without scribes) :

   i. (cavity size X - 900 µm) x (cavity size Y - 900 µm)

   The assembly house can choose the best cavity size to bond the circuit.
4. Try to keep the maximum length of the bonding wires, from middle bondpad to middle bondpin as small as possible (normally 3 mm for industrial purpose).

5. Do not use minimum metal width for connection to the bondpad. Use 20 µm width at least.



! 6. To determine the right position of the bondpads, it is advised to draw the chip together with the bondpins of the package. The chip has to be partitioned in equal segments (4 to 8). Bondpads and bondpins have to be located in the same segment (figure 3).

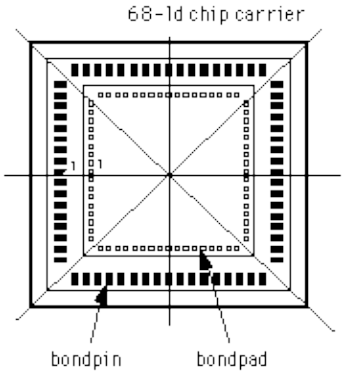


Fig. 3: Partitioning of the bondpads

7. Bondpad #1 should be identified (if possible) by means of a number "1" character or company logo (height 50µm) near the bondpad.

8. Bondpad #1 has to be the middle one of the bondpads, except for CPGA, CQFP and QFN package. Bondpads are numbered counter clockwise. By default, chips are attached to the frame by conductive die-attach. If the designer wants to have an extra connection from VSS (most negative voltage) to the substrate via the cavity, an extra bondwire has to be provided from the VSS bondpin to the cavity of the frame.

9. Crossing of bonding wires is not allowed (figure 5).

! 10. The angle between the bond wire and the normal through the middle of the bondpad should be maximum 45° (figure 4).

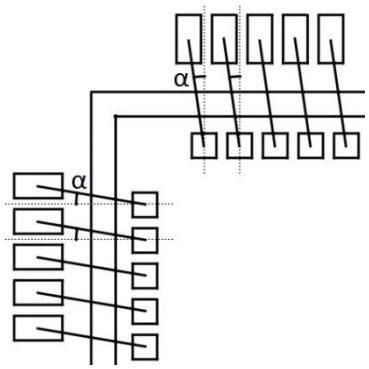


Fig. 4: Angle between the wire and the normal through the middle of the bondpad

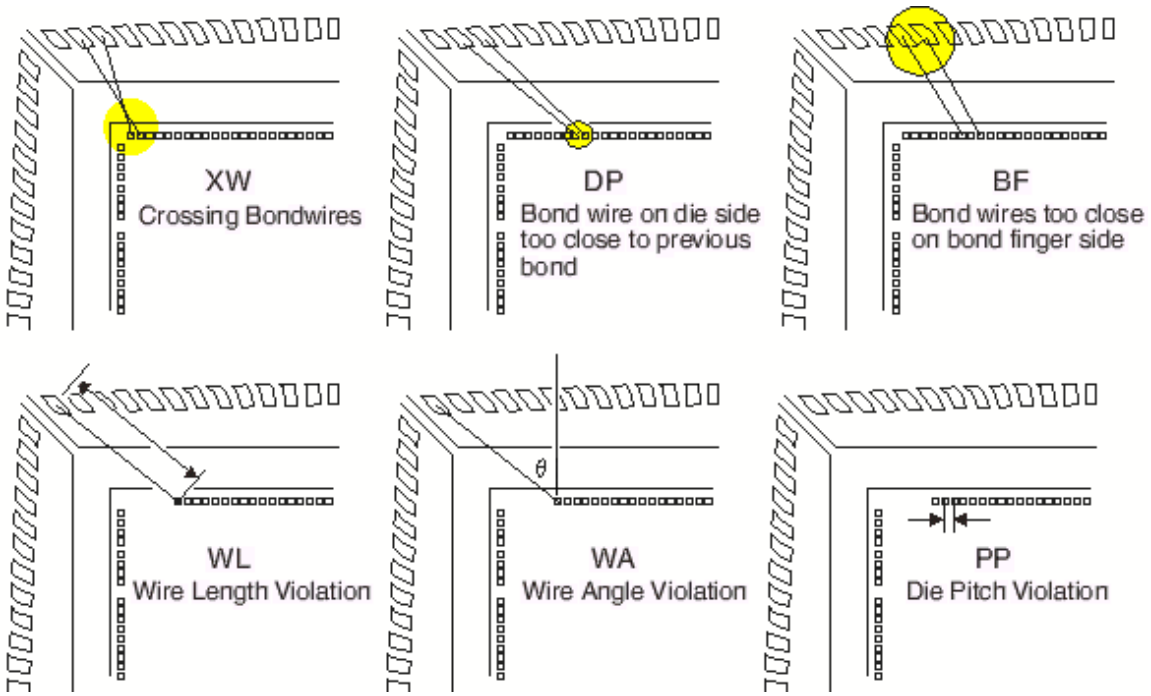


Fig. 5: Mistakes to avoid when we are creating a bonding diagram.

3 Generating a bonding scheme

It is preferable that the designer makes a clear bonding scheme (figure 6). Please be aware that for prototype assembly the bonding diagram will need to be verified case by case to examine feasibility!

To generate a bonding scheme, the next steps have to be followed:

- Open the GDS file containing all the packages listed on the Europractice website.

  For cadence users there is also a "gds-number to layername conversion table" available.

  The following files could be sent by the tapeout team:
  - AN-Guidelines to create a bonding diagram.pdf
  - ep_pack.layertable
  - ALL_PACK_CUSTOMER.gds.gz
- After the GDS file has been uploaded into Cadence, a library with 51 different types of packages is available, which can be used for all the different technologies supported by Europractice.
- Create a **<topcell>_PACK**.
- Add to this cell the desired package-cell (always use the _A4 or _A3 version!) and put the created **<topcell>** in the middle of the package cavity (the design can be rotated if necessary).
- Now the bondpads of the circuit can be connected to the bondpins of the package using a path of 25.4 µm wide (more or less). Use one of the available METAL layers to draw the connections. Use different colours for stacked bond pads, double wires,...
- Fill in the necessary design information (lower (A4) or right (A3) side):
  1. **Design name**: Please insert the name of your design.
  2. **General comments**: Please fill these fields by measuring the relevant parameters in your design's back-end GDS. Please delete any lines that don't apply to your design.
  3. **MPW**: Please specify the Europractice run number.
  4. **Die**: Top cell (= project name) of the final version of your GDS file.
  5. **Qty packaged**: The number of dies that need to be packaged.
  6. **Qty Naked**: The number of dies that will not be packaged based on this bonding diagram. This number therefore either corresponds to the number of unpackaged dies, or to the number of dies packaged using a different bonding diagram.
  7. **Die Attach**: The material to be used to attach a die to a package. By default, the die attach is EPO-TEK H20E conductive epoxy (please fill in "Default" for this field if you have no specific requirement). For specific requirements, please ask your technical imec contact for advice.

8. **Wire:** Type of wire to be used (Default is 1.2mil gold wire). Please fill in "Default" for this field if you have no specific requirement; otherwise, please ask your technical imec contact for advice.
9. **Size incl scribe**: Size of the dies. Please indicate the approximate size rounded to the nearest tenth of a millimetre.
10. **Lid**: Type of Lid requested. Please put a cross in the right square (mark with X)
    - ➔ **Taped ( )** = The lid is secured with scotch tape to the body.
    - ➔ **Sealed ( )** = It consists to apply a continuous bead of adhesive around all four package walls and then fit and seal the lid.
    - ➔ **Glued ( )** = The lid is glued (tacked) at the 4 corners to the body
    - ➔ **Glass ( )** = The lid is transparent. The glass lid is glued (tacked) at the 4 corners to the body. Glass lids are provided by Imec and do not have any special purpose unless mentioned otherwise.
    - ➔ **Tacked** = QFN's are too small to tape, you end up surrounding the complete package, this stops the part from going into a socket. We can **tack** the lids in place, a small dot of epoxy at each corner will hold the lid in place, this can be removed by a scalpel being placed between the lid and package to remove the lid. This can normally be carried out by the customer when required.

- Generate a GDS-file of the whole design library.
- Transfer the design data to imec.

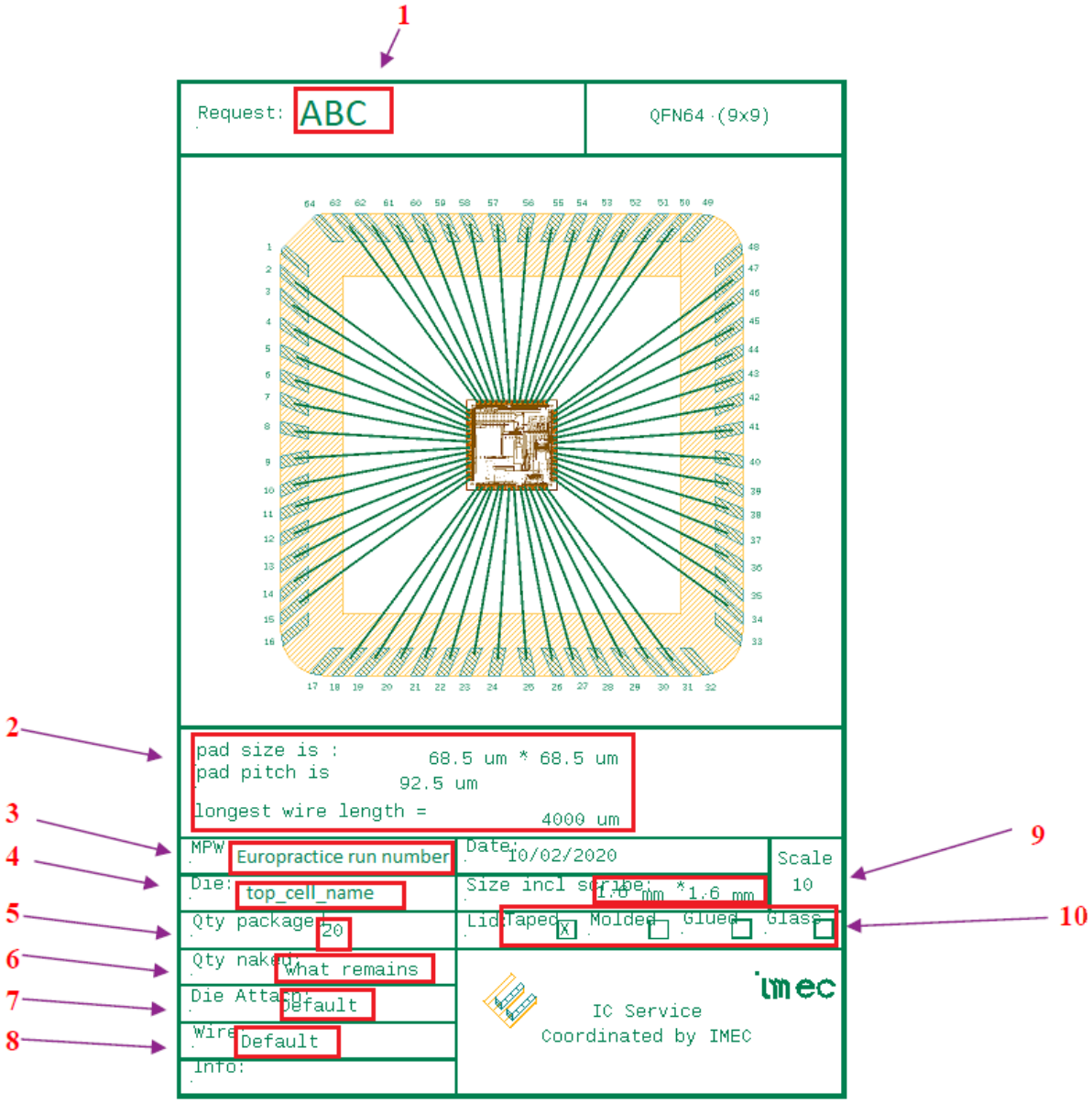


Fig. 6: Bonding scheme example

4 Generating a bonding request

To prepare a bonding request, the GDS-file of the bonding generated previously has to be sent by e-mail. This e-mail should mention the reference number of the design and should also contain the responses to the questions on below:

1. **Package**: The package you require. The name inserted here should correspond to the package name indicated on the bonding diagram?

2. **Technology**: Foundry and technology node your design was made in. For example, TSMC 180nm?

3. **CUP (Circuit Under Pad)**: If your design contains metal paths or TSMC IO cells beneath the pads, other than the metal of the pad itself, then it's a CUP and you should answer "Yes". Otherwise, answer "No"?

4. **Min bond pad pitch**: Find the pads in your circuit that are closest to each other and measure the pitch between these 2 pads?

5. **Passivation/polyimide**: Passivation is basically an electrically non-conductive layer that is "grown" on top of the die, for example Silicon Nitride or doped glass. It serves as a protective layer. Polyimide is a layer that is put on top of this passivation as an extra protective measure, mostly for environmental stresses. It is the same material as high-temperature tape (Kapton), but much thinner. If your design contains a polyimide layer, answer "Yes". Otherwise, answer "No"?

6. **Die size**?

7. **Passivation opening**: Measure the dimensions in micro-meters of the passivation openings in your design. The passivation opening layer is called CB and corresponds to CAD layer 19?

8. **Die material**: Please put "Silicon" here since this is the standard die material?

9. **Total number of naked dies**: Please specify the total number of dies you have for this design. Usually this is 40 dies (for 8 inch technologies) or 100 dies (for 12 inch technologies) unless you order additional dies?

10. **Dies to be packaged**: Please specify the number of dies to be packaged using the wirebonding diagram you are submitting a wirebonding request for?

11. **Wafer thickness**: Please specify the wafer thickness in mils and in micrometers (1 mil = 25.4µm)?

12. **Lid attach method**: Taped/tacked/glued/glass/sealed?

13. **Die attach**: In most cases, conductive epoxy is used (default). When conductive epoxy is used, the package cavity is electrically connected to the substrate of your chip. In the IO cells that you use, there is a substrate connection that ensures that the substrate of your chip is connected to ground. When conductive epoxy is used, this material ensures that the package cavity is also connected to ground. When non-conductive epoxy is used, the cavity of the package is not electrically connected to the substrate of your chip. In this case, to connect the package cavity to ground, cavity connections are necessary. A cavity connection in this case is done using a wirebond that goes from a pin on the package to the cavity of the package and another wirebond that goes from a VSS pin on your chip to the cavity of your package. Conductive/Non-conductive?

Two lines of marking will be added to the package with a maximum of 10 (dependent also on the package size) characters allowed per line: **Line 1** and **Line 2**.

5 What is an acceptable bonding diagram?

When a packaging request is sent to the suppliers, it is important that the bonding diagram shows (figure 7):

- Package pins
- Pin numbers
- Wirebonding
- Die outline
- Die pads
- Logo on the die
- Everything should be on scale

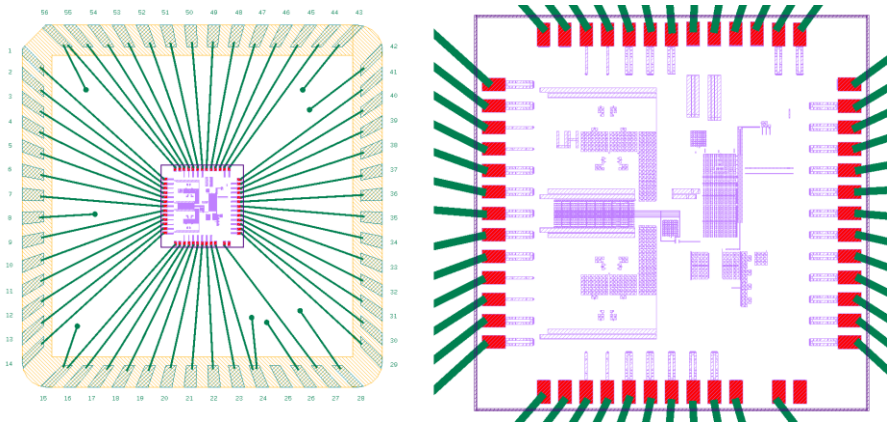


Fig. 7: Example of 'good' bonding diagram for QFN56

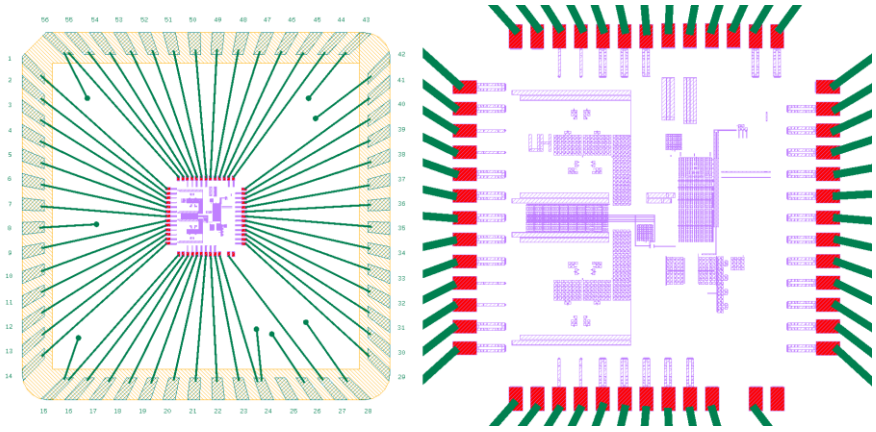


Fig. 8: Example of 'bad' bonding diagram for QFN56 (Without die outline)

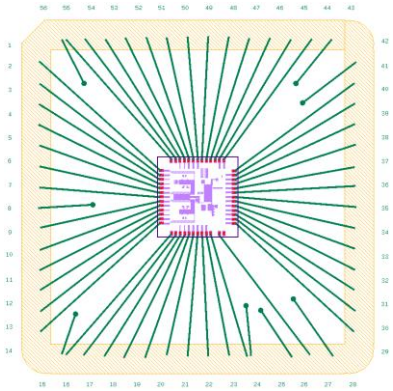


Fig. 9: Example of 'bad' bonding diagram for QFN56 (Without package pins)

Note 1:
Do not worry about warnings concerning the y* layers which are not translated to GDS format. Imec will fetch the necessary package cell from their own library. Only make sure that the wires and text are on a translated layer (ex. METAL).

Note 2:
If you have any questions, please check the cell in the gds-file called EXAMPLE_PACK.

Note 3:
There is a minimum order of 10 pieces per packaging request. The dies should come from the same tray (waffle pack). If the dies come from separate trays need to be packaged, there will be additional costs.
The same bonding diagram must apply for all dies to be packaged.

Note 4:
From the day the bare dies are shipped to the assembly house, it takes on average 1 month before the packaged dies return to imec.

Note 5:
For prototype assembly, we have to see the bonding diagram case by case to examine feasibility.

IMPORTANT:

All the packages in this library have isolated cavities (this means that there is no prefabricated connection between the cavity and one of the package pins). By default, the die is attached to the cavity with conductive glue. If a connection from the lowest or most negative potential (VSS) to the backside of the die is needed for achieving a better substrate contact, a bond wire can be added from the package pin to the cavity.