ASIC PACKAGE DESIGN RULES

I. Bonding guidelines:

Note: restrictions on wire grouping and layers may apply, bonding diagram must be reviewed by the assembly house prior to quotation and acceptance of order.

Standard-Non-standard wire/pad guidelines and configuration:

Item	Standard Service	Non-Standard Service
Die Thickness for QFN, SOIC TSSOP,QFP,SOT ,PSOT	Less than 12 Mil / 300um	
Die Thickness for Ceramic	Less than 24 Mil / 600um	
# Die Attach per Package	1	Multi-die quoted on request
Die Attach (conductive epoxy)	Epotek H20E Cure time 1 hour @ 150deg	Alternatives subject to availability
Die Attach (non-conductive epoxy)	Epotek H70E Cure time 1 hour @ 150 deg	Alternatives subject to availability
Package Identification	Printed label / Handwritten on device 8mm x 8mm minimum	Laser Marking available, please enquire for quotation (refer Laser Chapter)
Die placement accuracy	±100µm (manual placement)	If greater accuracy is required machine placement may be quoted on request.
Wire bond	25µm Au ball wire bonding (140 -150 degrees)	17µm, 20µm, 33µm and 50µm Au ball bonding. See table 2 for pad and pitch guidelines.
Minimum distance between a corner bond pad	Greater than 20µm	Greater than 20µm
Lidding	Refer to Lidding chapter	Solder Seam, Parallel Seam or Projection Weld (To Can) can be quoted on request.
Bond pad opening (Fig.1)	Greater than 55µmx55µm	See table 2 for pad and pitch guidelines.
Bond pad pitch (Fig.1)	Greater than 65µm	
Wire bond length	6mm or less, only for 25um wire STD.	
Bond wire angle	Less than 45˚	
Max. number of wires per package finger / pad	2	As required / possible (Limited by available bond area)
Maximum number of wires per package	256 Maximum	To be discussed – depends on process/wire chosen

Table 1: Standard and non-standard process rules for IC Assembly.

Au ball bonding:

Wire Diameter (um)	Pad size min. (um)	Pad Pitch min. (um)	Wire Length max. (mm)	Wire Angle min.
17.5	40	50	4.5	45˚
20	46	56	5.0	45˚
25	55	65	6.0	45˚
33	70	80	7.0	45˚

Table 2: Non-standard wire/pad guidelines

II. Configuration of the bond pads (die) and bond pins (packages)

1. Die configuration:

- **Bond-pad:** Pad on the chip to which the wire will be bonded.
- **Bond-pin:** Areas of package on which the wire will be bonded.

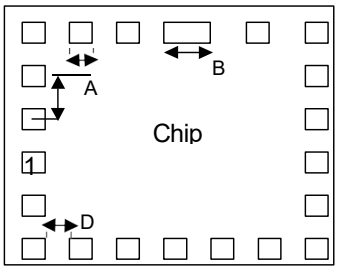


Fig. 1: Die & Bond pads

- **Die to die distance definition: 250µm minimum**

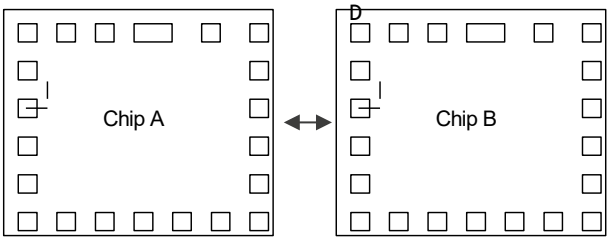


Fig. 2: Die to die distance

ASIC PACKAGE DESIGN RULES

2. List of packages:

DIL : Dual-in-Line package
CLCC : Ceramic Leadless Chip Carrier
JLCC : J-Leaded Chip Carrier
CPGA : Ceramic Pin Grid Array
CSOIC : Ceramic Small Outline Integrated Carrier
SOIC : Small Outline Integrated Carrier (Open-Pack)
CQFP : Ceramic Quad Flat Pack
QFN : Quad Flat pack No leads (Open-Pack)
QFN Ompp : Open-molded Plastic Package (OmPP) .with Ni/Pd/Au platin is a pre-molded, air cavity QFN package (Quad Flat No-Lead)

3. Notes:

Note 1: Open-Pak packages are pre-molded open cavity plastic packages which feature a gold plated copper die attach pad and lead frame. They have the same mechanical and electrical characteristics as their transfer molded counterparts. The die thickness for Open-Pak plastic types may not exceed 280µm (11 mils). This must be checked with the tape-out engineer responsible for the technology in question.

Note 2: The above list is not exhaustive and other options may be offered depending on the feasibility and availability of the package requested.

Note 3: The drawings provided on our website are examples of the packages offered and may not reflect the latest revisions. For the most up-to-date drawings, please reach out to our assembly team (ep.assembly@imec.be)

Note 4: Position of bond pin #1 (figure 3):

In case of an odd number of bond pins on one side of the cavity, (ex. 17 in the case of a 68-pin carrier) pin #1 is in the middle of the row. In case of an even number of bond pins on one side of the frame (for ex. 48-pin DIL) pin #1 is the first pin counter clockwise from the middle of the row of pins. For the CPGA's, CQFP's and QFN's, bondpin#1 is located in the corner, generally starting upper left bond pad and counting counter clockwise.

Note 5: For ceramic packages, bond pin #1 can also be recognized by the bevelled edge.

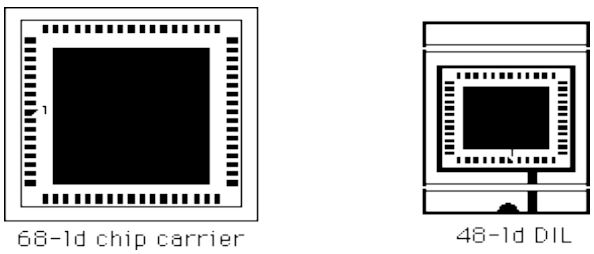
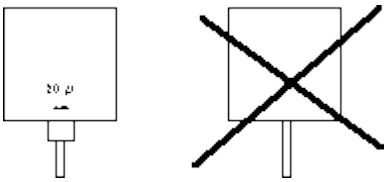


Fig. 3: Position of bondpin #1

4. Guidelines:

1. It is highly recommended for the bondpads to be equally distributed along the four sides of the chip
2. Minimum ratio of length/width of the chip: 1:2 (Highly recommended)
3. Max. size of the chip as designed (without scribes) :
   i. (cavity size X - 900 µm) x (cavity size Y - 900 µm) The assembly house can choose the best cavity size to bond the circuit.
4. Try to keep the maximum length of the bonding wires, from middle bondpad to middle bondpin as small as possible (refer to table 2).
5. Do not use minimum metal width for connection to the bondpad. Use 20 µm width at least.



6. To determine the right position of the bondpads, it is advised to draw the chip together with the bondpins of the package. The chip has to be partitioned in equal segments (4 to 8). Bondpads and bondpins have to be located in the same segment (figure 4).

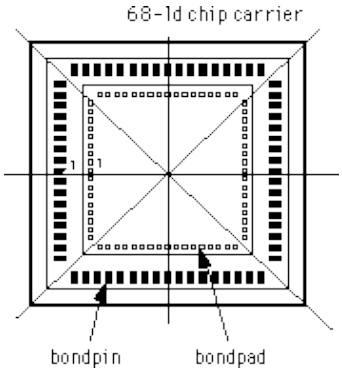


Fig. 4: Partitioning of the bondpads

7. Bondpad #1 should be identified (if possible) by means of a number "1" character or company logo (height 50µm) near the bondpad.
8. Bondpad #1 has to be the middle one of the bondpads, except for CPGA, CQFP and QFN package. Bondpads are numbered counter clockwise. By default, chips are attached to the frame by conductive die-attach. If the designer wants to have an extra connection from VSS (most negative voltage) to the substrate via the cavity, an extra bondwire has to be provided from the VSS bondpin to the cavity of the frame.
9. Crossing of bonding wires is not allowed (figure 9).
10. The angle between the bond wire and the normal through the middle of the bondpad should be

maximum 45˚ (figure 8).

11. It is highly recommended for the bondpads to be equally distributed along the four sides of the chip
12. Minimum ratio of length/width of the chip: 1:2 (Highly recommended)
13. Max. size of the chip as designed (without scribes) :
    i. (cavity size X - 900 µm) x (cavity size Y - 900 µm) The assembly house can choose the best cavity size to bond the circuit.
14. Try to keep the maximum length of the bonding wires, from middle bondpad to middle bondpin as small as possible (refer to table 2).
15. Do not use minimum metal width for connection to the bondpad. Use 20 µm width at least.

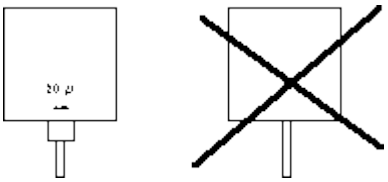


Fig. 5: Minimum metal width

16. To determine the right position of the bondpads, it is advised to draw the chip together with the bondpins of the package. The chip has to be partitioned in equal segments (4 to 8). Bondpads and bondpins have to be located in the same segment (figure 3).

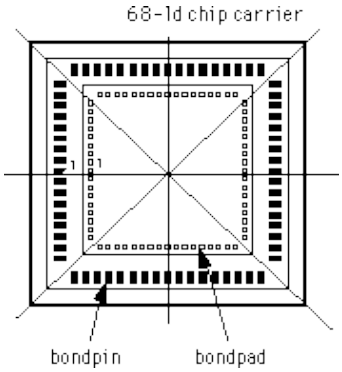


Fig. 6: Partitioning of the bondpads

17. Bondpad #1 should be identified (if possible) by means of a number “1” character or company logo (height 50µm) near the bondpad.
18. Bondpad #1 has to be the middle one of the bondpads, except for CPGA, CQFP and QFN package. Bondpads are numbered counter clockwise. By default, chips are attached to the frame by conductive die-attach. If the designer wants to have an extra connection from VSS (most negative voltage) to the substrate via the cavity, an extra bondwire has to be provided from the VSS bondpin to the cavity of the frame.

19. Crossing of bonding wires is not allowed (figure 9).

20. The angle between the bond wire and the normal through the middle of the bondpad should be maximum 45˚ (figure 8).

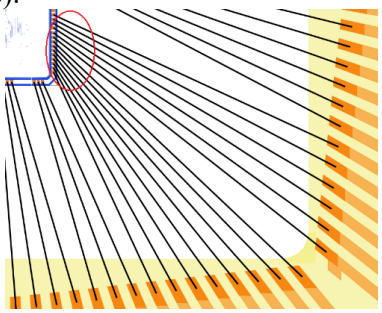


Fig. 7: Wire overlap

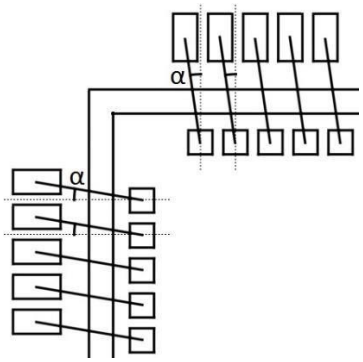


Fig. 8: Angle between the wire and the normal through the middle of the bondpad

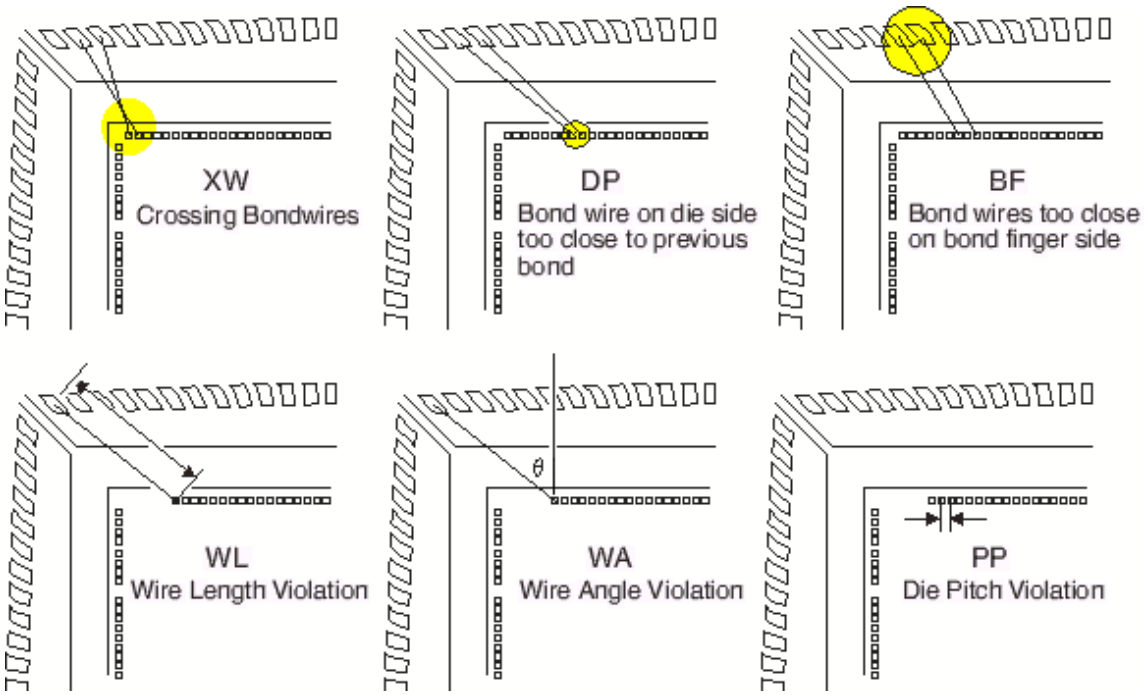


Fig. 9: Mistakes to avoid when we are creating a bonding diagram

III. Generating a bonding scheme:

The primary tool for generating a bonding scheme is Packmaker. The following steps outline how to proceed based on whether the required package is already available in Packmaker or needs to be integrated.

Please note that for prototype assembly, the bonding diagram will need to be verified on a case-by-case basis to ensure feasibility

1. Using Packmaker:

a. Package Already Available in Packmaker:

If the required package is available in Packmaker, the JSON file provided by the tape-out engineers will be used to fill out the necessary form in the link below. This form allows you to submit your Europractice assembly request and generate the bonding diagram

IC-Link File Uploader v1.3 (europractice.azurewebsites.net)

Please refer to the video instructions and provide the following design/assembly details:

- IM/Ref Number
- MPW Number
- Die Label
- Package Type
- Package Quantity
- Lid Type
- Die Attach
- Circuit Under PAD
- Polyimide on Chip
- Maximum Wire Length [um]
- PAD Pitch [um]
- PAD Opening Minimum Width x Height [um x um]
- Die Thickness [mils]
- Extra Info (for more specification if needed)

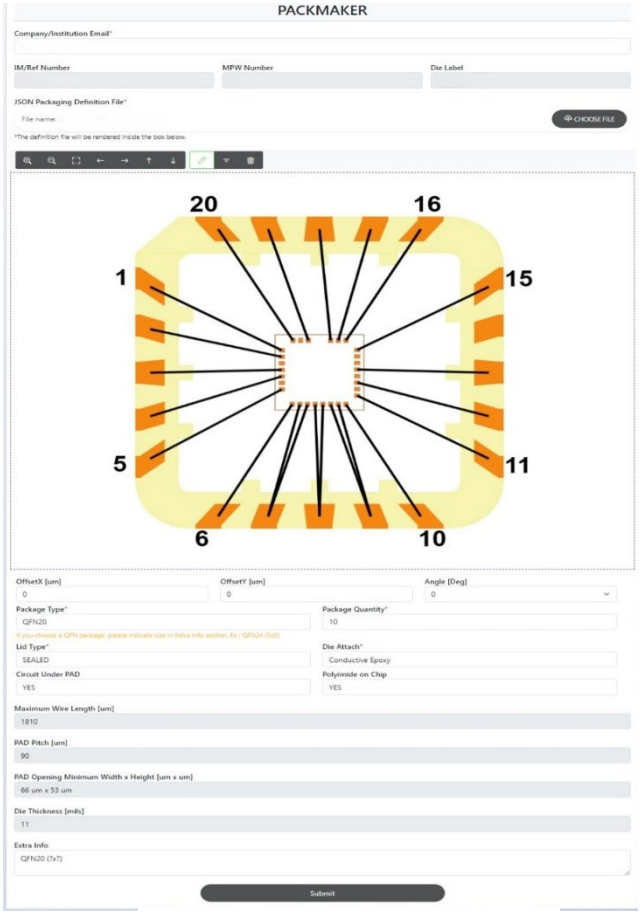


Fig. 10: Bonding scheme example

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1. **Wire:** Type of wire to be used (Default is gold wire). Please add a note in the Extra info if you have any specification or please ask your technical imec contact for advice.

2. **Package**: The package you require. The name inserted here should correspond to the package name indicated on the bonding diagram?

3. **Dies to be packaged**: Please specify the number of dies to be packaged using the wirebonding diagram you are submitting a wirebonding request for?

4. **Total number of naked dies**: Please specify the total number of dies you have for this design. Usually this is 40 dies (for 8 inch technologies) or 100 dies (for 12 inch technologies) unless you order additional dies?

5. **Lid attach method:** Taped / tacked / glued / glass / sealed?

   Lid: Type of Lid requested. Please put a cross in the right square (mark with X)

Lid Type	Lid Choice		Lid Sealing	Sealing Choice
Ceramic			Taped on Lid (Taped)	
Plastic			Solder Seal (Sealed) An additional charge will be made for a solder sealing applied only for ceramic packages	
Glass (will increase turn time and cost)			Epoxy Seal (Glued)	
Other (will increase turn time and cost)			Epoxy on four corners (Tacked)	

Table 3 : ***Type of lid and sealing***

Taped : The lid is secured with scotch tape to the body. Except for QFNs, which cannot be taped because they are too small, you end up taping around the whole package, preventing the part from going into a socket.

Sealed : It consists to apply a continuous bead of adhesive around all four package walls and then fit and seal the lid.

Glued : The lid is glued (tacked) at the 4 corners to the body
Tacked : A small dot of epoxy at each corner will hold the lid in place, this can be removed by a scalpel being placed between the lid and package to remove the lid. This can normally be carried out by the customer when required.

Glass : The lid is transparent. The glass lid is glued (tacked) at the 4 corners to the body. Glass lids are provided by Imec and do not have any special purpose unless mentioned otherwise

6. **Technology**: Foundry and technology node your design was made in. For example, TSMC 180nm

ASIC PACKAGE DESIGN RULES

7. **Die size and position**

8. **Maximum Wire length**

9. **Min bond pad pitch**: Find the pads in your circuit that are closest to each other and measure the pitch between these 2 pads.

10. **Passivation opening**: Measure the dimensions in micro-meters of the passivation openings in your design. The passivation opening layer is called CB and corresponds to CAD layer 19

11. **Wafer thickness**: Please specify wafer thickness in mils and in microns (1 mil = 25.4µm), Note that the die thinning is not performed by XFAB, so in general most packages require some backgrinding, a non-exhaustive list includes QFN,SOIC,TSSOP,QFP,SOT,TSOP

12. **Die attach**: In most cases, conductive epoxy is used (default). When conductive epoxy is used, the package cavity is electrically connected to the substrate of your chip. In the IO cells that you use, there is a substrate connection that ensures that the substrate of your chip is connected to ground. When conductive epoxy is used, this material ensures that the package cavity is also connected to ground. When non-conductive epoxy is used, the cavity of the package is not electrically connected to the substrate of your chip. In this case, to connect the package cavity to ground, cavity connections are necessary. A cavity connection in this case is done using a wirebond that goes from a pin on the package to the cavity of the package and another wirebond that goes from a VSS pin on your chip to the cavity of your package. Conductive/Non-conductive?

13. **CUP (Circuit Under Pad)**: If your design contains metal paths or TSMC IO cells beneath the pads, other than the metal of the pad itself, then it's a CUP and you should answer "Yes". Otherwise, answer "No"?

14. **Passivation/polyimide**: Passivation is basically an electrically non-conductive layer that is "grown" on top of the die, for example Silicon Nitride or doped glass. It serves as a protective layer. Polyimide is a layer that is put on top of this passivation as an extra protective measure, mostly for environmental stresses. It is the same material as high-temperature tape (Kapton), but much thinner. If your design contains a polyimide layer, answer "Yes". Otherwise, answer "No"?

15. **Die material**: Please put "Silicon" here since this is the standard die material.

16. **Laser Marking (if needed) :**

    Two lines of marking will be added to the package with a maximum of 10 (dependent also on the package size) characters allowed per line: **Line 1** and **Line 2**.

DESIGN RULES FOR LASER MARKING

	SERMA Microelectronics	
	Standard	**Non-Standard**
Maximum Engraving Area	100mmx100mm	<100mmx100mm
QFN 4mmx4mm	Font's height : 0.6mm 5 characters max per line	
QFN40 6X6 mm or QFN44 7X7 mm	Font's height : 0.6mm to 0.8mm 7 characters max per line	
QFN56 8X8 mm	Font's height : 0.6mm to 1mm 9 characters max per line	
QFN64 9X9 mm	Font's height : 0.6mm to 1.4mm 5 characters max per line	

Table 4: marking design rules

b. Package Not Available in Packmaker:

If the required package is not available in Packmaker, we will need 2-3 working days to integrate it into the tool. Once integrated, you will be able to use Packmaker to generate the bonding diagram.

2. Bonding Diagram Creation on Behalf of the Customer:

In case of a technical issue with Packmaker or if manual intervention is required, we can create the bonding diagram for you. To do this, please provide us with the following:

- A list of networks and pin assignments for the connecting wires.

Once we complete the bonding diagram, it will undergo a thorough review before being sent to you for final approval

IV. Customized Packages

We provide customized packaging solutions, including molded BGA and LGA types, featuring tailored substrates for your ASIC designs.
For specific requirements and detailed support, please don't hesitate to contact our Business Development Manager. BDM