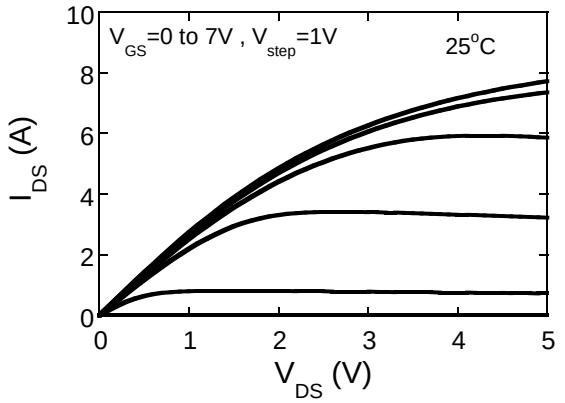
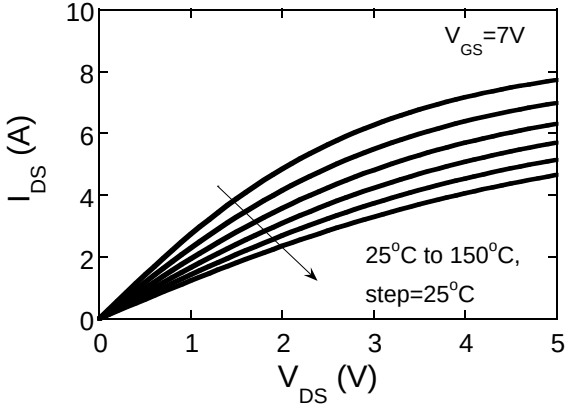
650 VOLTS
KEY ELECTRICAL SPECS

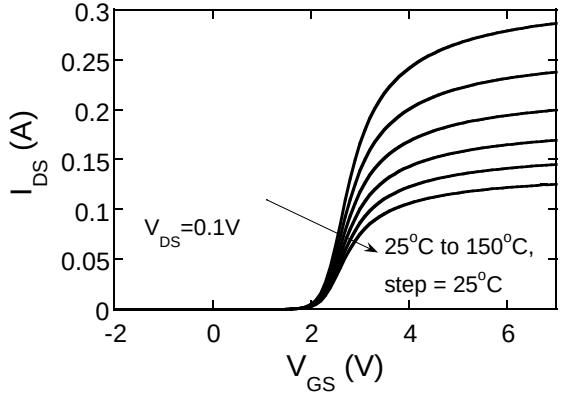
Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Absolute Maximum Ratings						
BV_{DS}	Drain-Source voltage		650			V
I_D	Pulsed Drain current	1 ms pulse			7.5	A
V_{GS}	Gate-Source voltage				7	V
ON/OFF-State Characteristics						
BV_{DS}	Drain-Source voltage	V_{GS} = 0 V	650			V
I_{DSS}	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 650 V T=25˚C		100	1000	nA/mm
	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 650 V T=150˚C		50	500	µA/mm
I_{GSS}	Gate reverse leakage	V_{GS} = 0 V, V_{DS} = 650 V T=25˚C		50	500	nA/mm
$R_{DS\text{-}ON}$	Drain-Source ON resistance	V_{GS} = 7 V, V_{DS} = 0.1 V T=25˚C		14	18	Ω.mm
	Drain-Source ON resistance	V_{GS} = 7 V, V_{DS} = 0.1 V T=150˚C		30	35	
V_{TH}	Gate threshold voltage	maximum g_m	2.1	2.5	2.9	V
Dynamic Characteristics						
C_{ISS}	Input capacitance	V_{GS} = 0 V V_{DS} = 650 V f = 1 MHz		47.2		pF
C_{OSS}	Output capacitance			14.6		pF
C_{RSS}	Reverse transfer capacitance			0.12		pF



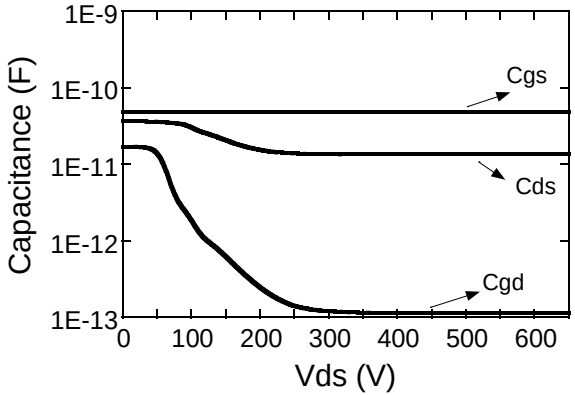
Typical I_{DS} vs. V_{DS} curve at T=25 °C



Temperature dependence of I_{DS} vs. V_{DS} curve at V_{GS}=7V



Temperature dependence of I_{DS} vs V_{GS} curve at V_{DS}=0.1V



Typical C_{GS} , C_{DS} and C_{GD} vs VDS at T=25 oC
Measurements on-wafer (no packaging parasitics included).