General Schedule 2020

Version 201207 – v18

EUROPRACTICE
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2020 GENERAL EUROPRACTICE MPW RUN SCHEDULE AND PRICELIST

Picture: imec

All the EUROPRACTICE General Multi-Project-Wafer runs listed below are accessible for universities, research institutes and companies. Please make sure to:

▶ Check the schedule version number

Run dates are subject to modification. To keep you informed, we constantly update the EUROPRACTICE MPW run schedules, which is reflected in the version number and the date when the last change was made. Make sure you downloaded the latest version.

▶ Read the footnotes carefully

For different foundries, different conditions are valid. For instance, the indicated run dates can be GDS Submission deadlines or Registration Deadlines. Such crucial information is always reflected in the footnotes.

▶ Contact us

We are open for any questions. You can find detailed contact information on our website europractice-ic.com

ams

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO		10				22				19		
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO		10				22				19		
ams 0.35µ HV CMOS H35B4D3 120V 4M					11						2	
ams 0.35µ SiGe-BiCMOS S35D4M5 / CMOS-RF C35B4M3 4M/4P Thick MET4 - MIM						15						

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **2 weeks** in advance.

EM Microelectronic

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
IC 0.18µm CMOS EMALP18 logic				24			15			30		

GLOBALFOUNDRIES

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
GLOBALFOUNDRIES SiGe 8HP		3		20		22		3		5		
GLOBALFOUNDRIES 130nm BCDlite	7		9		4		20		1		30	
GLOBALFOUNDRIES 130nm LP	7		9		4		20		1		30	
GLOBALFOUNDRIES 90WG Silicon Photonics			2			2			1		16	
GLOBALFOUNDRIES 55 nm LPx-NVM/ LPx-RF		17		20		22		17		5		
GLOBALFOUNDRIES 55 nm Lpe		17		20		22		17		5		
GLOBALFOUNDRIES 45RFSOI	1*				11				14			7
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave			9			15			1			14
GLOBALFOUNDRIES 28 nm SLP/SLP-RF		10			11			3			16	
GLOBALFOUNDRIES 22 nm FDSOI	1*		9		18		13		7		2	

Important notes: Dates are **Registration** deadlines after which designs cannot be accepted. Final GDSII file must be submitted within **6 weeks** after this date. A **cancellation fee** is applicable if the registration is cancelled later than 2 weeks after the Registration deadline or if the customer is unable to provide a DRC-clean GDS before the Tapeout deadline.
Dates in red are preliminary.
*Registration deadline for this run is 16 December 2019.

IHP

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V		7					24					
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V		7					24					
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics				17						23		
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)							17					
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV	10		20			19			4			14**
IHP SG13C SiGe:C CMOS 7M/MIM	10		20			19			4			14**
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV	10		20			19			4			14**
IHP SG13G2Cu FEOL process SG13G2 together with Cu BEOL option				3		19*			4			14**
IHP SG13SCu FEOL process SG13S together with Cu BEOL option				3		19*			4			14**
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV			6									

Important notes: Dates are **Registration** deadlines. Final GDSII file must be submitted within **10 days** after this date (see exceptions below).
* Additional MPW runs offered only when the cumulative area > 10mm².
Bumping is available for all IHP technologies with extra charge, limited to 200 bumps.
** 14 December is a Registration deadline. Final **GDSII** file must be submitted within **21 days** after this date.

ON Semiconductor

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	3		23			2		10		26		
ON Semi 0.7µ C07M-I2T100 100V - 2M & 3M options	3		23			2		10		26		
ON Semi 0.5µ CMOS EEPROM C5F & C5N – 200 mm			23				27				23	
ON Semi 0.35µ C035U - 4M (3M & 5M optional) only thick top metal	27			14			1		14			1
ON Semi 0.35µ C035 - I3T25U 3.3/25V 4M (3M & 5M optional) only thick top metal	27			14			1		14			1
ON Semi 0.35µ C035 - I3T80U 80V 4M - 3M optional (5M on special request)	2			1			6			5		
ON Semi 0.35µ C035 - I3T50U (E) 50V 4M - 3M optional (5M on special request)			2		25				1			1
ONC18MS (0.18 µm - 1.8/3.3V - 15V DMOS - 5LM - MiMC - ESD - HiR - EPI)		3		6		8		10		15		7
ONC18MS-LL (=ONC18MS + High Vt)		3		6		8		10		15		7
ONC18HPA (= ONC18MS + DNW + Zener + Stacked MiMC + Native Dev + Schottky)		3		6		8		10		15		7
ONC18-I4T 45/70V HV CMOS (=ONC18MS + 30V + 45V + 70V DMOS)		3		6		8		10		15		7

Important notes: Dates are **GDS submission** deadlines. Design registration has to be done at least **3 weeks** in advance.

STMicroelectronics

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
ST 28nm CMOS28FDSOI		10							14			
ST 55nm BiCMOS055		17					27					
ST 65nm CMOS065		4				5						
ST 130nm BiCMOS9MW			2			2					2	
IC 0.16µm BCD8sP			12							1		
IC 0.16µm BCD8s-SOI						16						

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **4 weeks** in advance.

TSMC

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	1,29	19	4	8,22	6,20	10,17	8,22	5,19	2,30	7,21,28	18	2,23
TSMC 0.18 CMOS High Voltage BCD Gen II	1	19	4	15,29		3,10,17	8	5,26	2	7,28	11	2,23
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (8-inch)			11	15			8					9
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (12-inch)	1	12			6	10		5	9	7	11	16
TSMC 90nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power		5	4		6,27		22			21		16
TSMC 65nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power*	22	26	25	22	20	24	22	26	23	28	25	9
TSMC 40nm CMOS Logic or Mixed-Signal/RF, GP or Low Power (no triple gate oxide)	22	26		8,22		3	8,29		9,30	28	25	
TSMC 28nm CMOS Logic HPL/HPC/HPC+, RF HPL/HPC/HPC+*	29		4,25	29		3	1,29		2,30		4	2,16
TSMC 16nm CMOS Logic FinFET Compact*	22			1	20		22		23		18	

See **Important notes** for TSMC on the next page **(Page 4)**

Important notes for TSMC: Dates are **GDS submission** deadlines.
Design registration must be done at least **4 weeks** in advance unless otherwise specified in the table above.
*For these technologies, please make reservation **4 months** in advance.
Bumping is available upon request for all 12-inch technologies.
Contact eptsmc@imec.be if any of the following options are used:
Bumping, MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS.

UMC

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
UMC L180 Logic GII, Mixed-Mode/RF		3		27			27		28			14
UMC L180 EFLASH Logic GII			2							5		
UMC CIS180 Image Sensor – CONV/ULTRA diode					29							
UMC L130 Logic/Mixed-Mode/RF		24				29					2	
UMC L110AE Logic/Mixed-Mode/RF		24		27		22		31		26		14
UMC L65N Logic/Mixed-Mode/RF - LL	27 *	24		6 *			13 *	3	28 *			14
UMC L65N Logic/Mixed-Mode/RF - SP	27 *	24		6 *			13 *	3	28 *			14
UMC 40N Logic/Mixed-Mode – LP *			9	10		29		24			23	
UMC 28N Logic/Mixed-Mode – HPC *	27			27			27				2	

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **3 weeks** in advance.
*Please contact epumc@imec.be when planning to participate in runs with an asterisk.
Dates in red are preliminary.

UMC Technology Options

Options Regular Runs	Metallization	Core	IO	MIM	Topmetal	Remarks
UMC CIS18 - Image Sensor - 2P4M - ULTRA Diode	max. 2P4M	1.8V	3.3V	1fF	5kA	Colorfilters and microlenses. Ultra diode topology is a 4T pinned structure. PIP capacitor possible.
UMC CIS18 - Image Sensor - 1P4M - CONV Diode	max. 1P4M	1.8V	3.3V	1fF	5kA	Colorfilters and microlenses included.
UMC L180 EFLASH Logic GII	max. 2P6M	1,8V	3.3V	/	8kA	Please get in touch with us for the EEFLASH macro information.
UMC L180 Mixed-Mode/RF	max. 1P6M	1.8V	3.3V	1fF	8kA/12kA/ 20kA	Redistribution and bumping on request.
UMC L180 Logic GII	max. 1P6M	1.8V	3.3V	1fF	8kA	Redistribution and bumping on request.
UMC L130 Mixed-Mode/RF	max. 1P8M2T	1.2V	3.3V	1fF/ 1.5fF/2fF	8kA/20kA	Two types (out of 3) of devices can be combined: HS,LL, SP. Redistribution to Aluminium.
UMC L130 Logic	max. 1P8M2T	1.2V	3.3V	1fF/ 1.5fF/2fF	8kA	Two types (out of 3) of devices can be combined: HS,LL, SP. Redistribution to Aluminium.
UMC L110AE Logic/Mixed-Mode/RF	max. 1P8M	1.2V	1.8V/2.5V/ 3.3V/5V	1fF/ 1.5fF/2fF	8kA/12kA/ 20kA/40kA	Metallization is Aluminium. 5V device possible! HS,LL,SP can be combined.
UMC 65N Logic/Mixed-Mode/RF - SP	max. 1P10M	1.0V & 1.1V	1.8V/2.5V/ 2.5V_OD3.3V/3.3V	2fF	8kA/32.5kA	Metallization recommendation on request. Redistribution to Aluminium.[1]
UMC 65N Logic/Mixed-Mode/RF - LL	max. 1P10M	1.2V	1.8V/2.5V/ 2.5V_OD3.3V/3.3V	2fF	8kA/32.5kA	Metallization recommendation on request. Redistribution to Aluminium.[2]
UMC 40N Logic/Mixed-Mode - LP	max. 1P11M	0.9V	1.8V/2.5V	2fF	8kA/12kA/ 32.5kA	Metallization recommendation on request. Redistribution to Aluminium.
UMC 28N Logic/Mixed-Mode - HPC	max. 1P11M	1.0 & 1.1V	1.8V/2.5V	2fF	8kA/12kA/ 32.5kA	Metallization recommendation on request. Redistribution to Aluminium.

[1] 6x (H) metal, LVT, MIM in development. Please contact epumc@imec.be if you use this option.
[2] 6x (H) metal in development. Please contact epumc@imec.be if you use this option.

X-FAB

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
XH018 0.18µ HV NVM CMOS E-FLASH	20			17			27			23		
XT018 0.18µ HV SOI CMOS	10		16			8		24			2	
XS018 0.18µ OPTO		28							11			
XP018 0.18µ NVM CMOS		7				19				9		
XH035 0.35µ HV CMOS	10				1			7			6	
XR013 0.13µ RF SOI CMOS		24			26			25			2	
XMB10 MEMS					27							

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **2 weeks** in advance.

X-FAB Technology Options

Options Regular Runs	Process modules included
XH018 0.18µ HV NVM CMOS E-FLASH 6M	LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS,HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO
XT018 0.18µ HV SOI CMOS 6M	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY,MIMH, MET3, MET4, METMID, METTHK, HWC
XS018 0.18µ OPTO 6M	MOS3LP, MOSLP, MET3, MET4, MET5, METMID, MRPOLY, ISOMOS, LVTN3D,BCH, MIM23, PPDB, 4TPIX, SFLATPV
XP018 0.18µ NVM CMOS 6M	LP5MOS, MET3, MET4, METMID, METTHK, MRPOLY, HRPOLY, ISOMOS,LVT, MIM, NVM
XH035 0.35µ HV CMOS 4M	MOS, MOS5A, ISOMOS, HVMOSMID, HRPOLY, MIM, METAL4
XR013 0.13µ RF SOI CMOS 4M	MET1, MET2, MIM, METRB, NOPIMIDE, 2V5DT, HRPOLY, CORE, METBQ
XR013 0.13µ RF SOI CMOS 5M	MET1, MET2, METTHKI, MIM, METRB, NOPIMIDE, 2V5DT, IV2DT, LNGI,HRPOLY, CORE, DGOXA, METBQ, LNG2

AMF

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Si-Photonics fabrication process AMF			9								4	

Important notes: Dates are **GDS submission** deadlines. Please register on myCMP at least **2 weeks** in advance.

CEA-LETI

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Si-Photonics ICs Si310-PHMP2M			20							16		

Important notes: Dates are **GDS submission** deadlines. Please register on myCMP at least **2 weeks** in advance.

CORNERSTONE

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
CORNERSTONE Si-Photonics 220nm SOI Passives			6						25			
CORNERSTONE Si-Photonics 220nm SOI Actives			6									
CORNERSTONE Si-Photonics 340nm SOI Passives	10											18
CORNERSTONE Si-Photonics 500 nm SOI Passives						26						

Important notes: Dates are **GDS submission** deadlines. Registration should be done at least **4 weeks** in advance.

imec

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
imec Si-Photonics Passives+				8				26				
imec Si-Photonics iSiPP50G		26			27					14		
imec SiN-Photonics BioPIX 300									7			
imec GaN-IC on SOI 200V				22								
imec GaN-IC on SOI 650V										18		

Important notes: Dates indicate deadlines for both **Registration** and submission of the **first version of the GDS** file.

LioniX

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
LNX SiN-Photonics TriPleX VIS							15					
LNX SiN-Photonics TriPleX 1550							31				30	
LNX SiN-Photonics TriPleX 850						30						11

Important notes: Dates are **GDS submission** deadlines.
For registration dates and other details, please contact europratice.gateway@tyndall.ie

MEMSCAP

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
PolyMUMPs				7			20				3	
SOIMUMPs		18			19			18			24	
PiezoMUMPs	14				5			25				

Important notes: Dates indicate deadlines for both **Registration** and submission of the **first version of the GDS** file.

EUROPRACTICE
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2020 PRICELIST FOR GENERAL EUROPRACTICE MPW RUNS

Prices are valid for General EUROPRACTICE MPW runs from 1 January 2020
Prices and conditions are subject to modification at any time without prior notice.

Discounted price

Three conditions for discounted prices:

- A customer represents an academic institution or a research facility from one of the 28 EU countries together with Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, North Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine.
- A customer is a registered EUROPRACTICE member who has paid the Full-IC annual membership fee.
- The intended design will be done for educational purposes or for publicly funded research.

Standard price

Standard prices apply to all other customers.

Number of prototypes

ams: 40 samples
GLOBALFOUNDRIES: 50
IHP: 40 for SG25 & SG13;
25 using TSV module, PIC & EPIC
ON Semi: 30
TSMC: 8-inch: 40; 12-inch: 100
UMC: 50
X-FAB: 50

CORNERSTONE: 10
imec: Si-Photonics Passives+ and iSiPP50G: 20 for 1 block or larger
10 for half block or smaller
imec SiN-Photonics: 20
imec GaN-IC on SOI: 100
LNX TriPleX VIS and 1550: 4
LNX TriPleX 850: 20
MEMSCAP: 15

If you need more prototype samples, please contact us for a quotation.

Plots

You can order plots/PDF of your designs:

- First plot/PDF costs 50 euro
- Next plots cost 20 euro each

Packaging

Prices are given for the delivery of unpackaged, untested prototypes. Encapsulation and testing will be charged separately.

See separate prices and available packages on europractice-ic.com/schedules-prices/

ams

Technology	Standard EUR / mm²	Discounted EUR / mm²
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	640 [1]	580 [1]
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	800 [2]	700 [2]
ams 0.35µ HV CMOS H35B4D3 120V 4M	880 [1]	800 [1]
ams 0.35µ SiGe-BiCMOS S35D4M5 / CMOS-RF C35B4M3 4M/4P Thick MET4 - MIM	880 [1]	800 [1]

Important notes: [1] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 7mm²
[2] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 20mm²

EM Microelectronic

Technology	Standard EUR / mm²	Discount EUR / project
0.18µm EMALP18 logic (Area < 5mm²)	1,650	600
0.18µm EMALP18 logic (Area > 5mm²)	1,250	600

Important notes: Area = X*Y including seal ring.

GLOBALFOUNDRIES

Technology	Standard EUR / mm²	Discounted EUR / mm²
GLOBALFOUNDRIES SiGe 8HP	3,800 [1]	3,600 [1]
GLOBALFOUNDRIES 130 nm BCDlite	1,500 [2]	1,400 [2]
GLOBALFOUNDRIES 130 nm LP	1,500 [2]	1,400 [2]
GLOBALFOUNDRIES 90WG Silicon Photonics	5,250 [1]	5,000 [1]
GLOBALFOUNDRIES 55 nm LPx-NVM/LPx-RF	4,000 [2]	3,800 [2]
GLOBALFOUNDRIES 55 nm LPe	4,000 [2]	3,800 [2]
GLOBALFOUNDRIES 45RFSOI	7,350 [2]	7,000 [2]
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	5,000 [2]	4,700 [2]
GLOBALFOUNDRIES 28 nm SLP/SLP-RF	10,200 [2]	9,700 [2]
GLOBALFOUNDRIES 22 nm FDSOI	14,000 [2]	13,200 [2]

Important notes: [1] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 25mm². Any edge length between 1.0mm to 12.5mm is possible. The mentioned die size is referred to the Pre-Shrink die size.
[2] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 9mm². Any edge length between 1.0mm to 12.5mm is possible. The mentioned die size is referred to the Pre-Shrink die size.

IHP

Technology	Standard EUR / mm²	Discounted EUR / mm²
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	2,500 [1]	2,125 [1]
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	3,800 [1]	3,230 [1]
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics	8,000 [1]	6,800 [1]
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)	3,800 [1]	3,230 [1]
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV	6,300 [1]	5,355 [1]
IHP SG13C SiGe:C CMOS 7M/MIM	4,500 [1]	3,825 [1]
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV	7,300 [1]	6,205 [1]
IHP SG13G2Cu FEOL process SG13G2 together with Cu BEOL option	7,000 [1]	5,950 [1]
IHP SG13SCu FEOL process SG13S together with Cu BEOL option	6,100 [1]	5,185 [1]
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV	1,000 [1]	850 [1]
IHP Special Services		
Bumping (available for all IHP technologies)	6,500 [2]	6,500 [2]
Localized Back side Etching (available for all IHP technologies) not offered for EPIC/PIC runs	5,000 [2]	4,250 [2]
TSV to ground (SG13)	5,000 [2]	4,250 [2]
Non-Standard wafer thickness in SG13	3,000	3,000
Non-Standard wafer thickness in SG25	2,000	2,000

Important notes: [1] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 0.8mm².
The chip area is inclusive of the filler cells outside the seal ring.
[2] Price = per submitted design. For bumping (no size limit, limited to 200 bumps) final wafer thickness for TSV is 75µm.

ON Semiconductor

Technology	Standard EUR / mm²	Discounted EUR / mm²
ON Semi 0.7µ C07M-D 2M/1P	300 [1]	270 [1]
ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	350 [1]	315 [1]
ON Semi 0.7µ C07M-I2T100 100V - 2M	525 [2]	485 [2]
ON Semi 0.7µ C07M-I2T100 100V - 3M	560 [2]	525 [2]
ON Semi 0.5µ CMOS EEPROM C5F & C5N – 200 mm	1,150 [1]	1,100 [1]
ON Semi 0.35µ C035U 4M (default) including analog options	720 [2]	670 [2]
ON Semi 0.35µ C035U 3M (optional) including analog options	700 [2]	650 [2]
ON Semi 0.35µ C035U 5M (optional) including analog options	800 [2]	750 [2]
ON Semi 0.35µ C035 - I3T80U 80V 3M	850 [2]	800 [2]
ON Semi 0.35µ C035 - I3T80U 80V 4M	925 [2]	875 [2]
ON Semi 0.35µ C035 - I3T80U 80V 5M	1,050 [2]	995 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50V 3M	850 [2]	800 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50V 4M	925 [2]	875 [2]
ON Semi 0.35µ C035 - I3T50U (or E) 50V 5M	1,050 [2]	995 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25V 3M (optional)	750 [2]	700 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25V 4M (default)	770 [2]	720 [2]
ON Semi 0.35µ C035 – I3T25U 3.3/25V 5M (optional)	800 [2]	750 [2]
ONC18MS 0.18 µm - 1.8/3.3V - 15V DMOS - 5LM - MiMC - ESD - HiR - EPI	1,100 [2]	1,050 [2]
ONC18MS-LL (=ONC18MS + High Vt)	1,225 [2]	1,195 [2]
ONC18HPA (= ONC18MS + DNW + Zener + Stacked MiMC + Native Dev + Schottky)	1,350 [2]	1,290 [2]
ON 0.18 µm I4T 40/75V - 5LM – DTI (=ONC18MS + 30V + 45V + 70V DMOS)	1,540 [2]	1,480 [2]

Important notes: [1] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 5mm².
[2] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 10mm².

ST Microelectronics

Technology [1]	Standard EUR / mm²	Discount EUR / project
ST 28nm CMOS28FDSOI	9,000 [2,7] 18,000+[(Area-2) x 6,750] [5]	1,500
ST 55nm BiCMOS055	5,500 [2] 11,000+[(Area-2) x 4,250] [5]	1,200
ST 65nm CMOS065	4,500 [3] 22,500+[(Area-5) x 3,750] [6]	1,200
ST 130nm BiCMOS9MW	2,600 [3] 13,000+[(Area-5) x 2,200] [6]	1,000
ST 130nm H9SOI-FEM	2,200 [3] 11,000+[(Area-5) x 1,500] [6]	700
ST 130nm HCMOS9GP	2,500 [3] 12,500+[(Area-5) x 2,200] [6]	700
ST 130nm HCMOS9A	2,500 [3] 12,500+[(Area-5) x 2,200] [6]	700
ST 0.16µm BCD8sP	2,500 [4] 12,500+[(Area-5) x 2,200] [6]	1,000
ST 0.16µm BCD8s-SOI	2,500 [4] 12,500+[(Area-5) x 2,200] [6]	1,000
STMicroelectronics Wafer Level Bumping		
on 300mm ST 55nm BiCMOS055 process	25,000 [8]	1,500 [8]
on 300mm ST 65nm CMOS065	23,000 [8]	1,500 [8]
on 300mm ST 28nm CMOS28FDSOI	33,000 [8]	1,500 [8]

Important notes: [1] Area = X*Y including seal ring.
[2] Price for Area ≤ 2mm² with minimum charge of 1.25mm².
[3] Price for Area ≤ 5mm² with minimum charge of 1.25mm².
[4] Price for Area ≤ 5mm² with minimum charge of 3.43mm².
[5] Price for 2mm² ≤ Area ≤ 10mm². Contact CMP when Area is larger.
[6] Price for 5mm² ≤ Area ≤ 15mm². Contact CMP when Area is larger.
[7] Special additional discount for CNRS Institutions: 1500 €/project.
[8] Prices per project.

TSMC

Prices for all TSMC technologies can be calculated through the online Price Request Form http://europractice-ic.com/requests/tsmc-price-request/.
When 4 or more independent sub-designs are registered in one MPW submission to optimise the minimum charged area, an additional verification charge of 1,000 USD is applicable. This is regardless of the request and charges for sub die sawing (5 USD per additional die obtained from the base MPW submission).

UMC

Technology	Standard EUR / block	Discounted EUR / block
UMC L180 Logic GII, Mixed-Mode/RF	14,200 [1]	13,500 [1]
UMC L180 CIS 2P4M CONV or 2P4M ULTRA	22,700 [1]	21,580 [1]
UMC L180 EFLASH Logic GII	18,000 [1]	17,100 [1]
UMC L130 Logic/Mixed-Mode/RF	23,650 [1]	22,480 [1]
UMC L110AE Logic/Mixed-Mode/RF	26,050 [1]	24,760 [1]
UMC L65nm Logic, Mixed-Mode/ RF – LL/SP	37,450 [2]	35,580 [2]
UMC 40N Logic/Mixed-Mode – LP	72,500 [2]	68,880 [2]
UMC 28N Logic/ Mixed-Mode – HPC	On request. Please, contact epumc@imec.be	

Important notes: [1] Price = per block of 5mm x 5mm needed to fit the design in.
[2] Price = per block of 4mm x 4mm needed to fit the design in.

X-FAB

Technology	Standard EUR / mm^2	Discounted EUR / mm^2
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, MET4, METMID, MET-THK)	1,605	1,525
X-FAB XT018 0.18µ HV SOI CMOS (MET3, MET4, METMID, METTHK)	1,635	1,555
X-FAB XS018 0.18µ OPTO (MET3, MET4, MET5, METMID)	1,375	1,310
X-FAB XP018 0.18µ NVM CMOS (MET3, MET4, METMID, METTHK)	1,415	1,345
X-FAB XH035 0.35µ HV CMOS (MET4)	1,035	985
X-FAB XR013 0.13µ RF SOI CMOS (METRB, METBQ)	1,830	1,745
X-FAB XR013 0.13µ RF SOI CMOS (METTHK1, METRB, METRQ)	2,280	2,165
XMB10 MEMS	10,500 [1]	9,800 [1]

Important notes: Price = area (mm^2) * price/mm^2 with min. fabrication cost equivalent to 10mm^2.
Area will be rounded upwards to the next mm^2 (for instance, 12.24mm^2 will be charged as 13mm^2).
[1] The price includes delivery of 5 dies with maximum size per die of 10mm^2. Additional dies can be purchased for 10EUR/die (50 dies maximum).

AMF Si-Photonics

Options	Standard EUR / mm^2	Discount EUR / project
Area = 6mm^2	7,500 [1]	700
Area = 12mm^2	12,000 [1]	1,000
Area = 24mm^2	20,100	1,500
Area = 48mm^2	37,900	1,500

Important notes: Area = X*Y including seal ring.
[1] Price and design size ONLY for academia.

CEA-LETI Si-Photonics Si310-PHMP2M

Options	Standard EUR / mm^2	Discount EUR / project
Area ≤ 10mm^2 with minimum charge of 2 blocks or 4mm^2	1,600 [1]	700
Additional blocks above 10mm^2 with minimum charge of 16,000€	16,000 + (900/mm^2) [1]	700

Important notes: Charged Area = multiples of 2mm^2 blocks including seal ring.
[1] Each block is multiple 1 x 2 mm^2 and/or 2 x 1 mm^2.

CORNERSTONE

Options	Standard EUR	Discounted EUR
Half block - Passives only, all platforms (5.5mm x 4.9mm)	5,100	4,800
Full block - Passives only, all platforms (11.47mm x 4.9mm)	8,100	7,700
Half block - Passives with heaters, all platforms (5.5 x 4.9mm)	9,600	9,100
Full block - Passives with heaters, all platforms (11.47mm x 4.9mm)	14,000	13,300
Half block - Actives, 220nm SOI platform (5.5mm x 4.9mm)	25,000	23,750
Full block - Actives, 220nm SOI platform (11.47 x 4.9mm)	44,000	41,800
Extra Options		
Extra set of blocks – Passives (10 samples)	+2,200	+2,200
Extra set of blocks – Passives with heaters (10 samples)	+3,000	+3,000
Extra set of blocks – Actives (10 samples)	+5,000	+5,000

Important notes: Standard number of samples for all platforms is10. If more prototypes are needed, please see Extra Options in the table above.

imec Si-Photonics Passives+

Options	Standard EUR	Discounted EUR
Half block - horizontal (5.15mm x 2.5mm) or vertical (2.5mm x 5.15mm)	6,100	5,800
1 block (5.15mm x 5.15mm)	11,600	11,000
2 blocks - horizontal (10.45mm x 5.15mm) or vertical (5.15mm x 10.45mm)	20,600	19,600
Larger sizes	Please, contact epsiphot@imec.be	
Extra Options		
Extra set of half block chips (10 samples)	+2,000	+2,000
Extra set of chips (1 block or larger; 20 samples)	+2,000	+2,000

Important notes: Imec Si-Photonics Passives technology is replaced by imec Si-Photonics Passives+ technology in 2019. Imec Si-photonics passives+ allows for metal heaters and edge-couplers, but its introduction also implies a few other changes to the offer. Existing users, please be cautious.
Number of prototypes in base order depends on design size: 20 for 1 block or larger, 10 for half block or smaller.
Due to the nature of MPW logistics, more chips than ordered may sometimes be shipped.

imec Si-Photonics iSiPP50G

Options	Standard EUR	Discounted EUR
Quarter block (2.5mm x 2.5mm)	10,000	9,500
Half block - horizontal (5.15mm x 2.5mm) or vertical (2.5mm x 5.15mm)	20,000	19,000
1 block (5.15mm x 5.15mm)	40,000	38,000
2 blocks - horizontal (10.45mm x 5.15mm) or vertical (5.15mm x 10.45mm)	80,000	76,000
4 blocks (10.45mm x 10.45mm)	150,000	142,500
Other sizes	Please, contact epsiphot@imec.be	
Extra Options		
Extra set of quarter block chips (10 samples)	+2,000	+2,000
Extra set of half block chips (10 samples)	+2,000	+2,000
Extra set of chips (1 block or larger; 20 samples)	+2,000	+2,000

Important notes: Number of prototypes in standard order depends on design size: 20 for 1 block or larger, 10 for half block or smaller.
Due to the nature of MPW logistics, more chips than ordered may sometimes be shipped.

imec SiN-Photonics BioPIX 300 and 150

Options	Standard EUR	Discounted EUR
1 block (5.30mm x 4.75mm)	23,000	21,850
2 blocks - horizontal (10.75mm x 4.75mm)	46,000	43,700
2 blocks - vertical (5.30mm x 9.65mm)	46,000	43,700
4 blocks (10.75mm x 9.65mm)	92,000	87,400
Other sizes	Please, contact sinmpw@imec-int.com	
Extra Options		
Extra set of chips (20 samples)	+1,000	+1,000

Important notes: Number of prototypes in base order: 20 samples, for each design block registration irrespective of the block size.
Due to the nature of MPW logistics, more chips than ordered may sometimes be shipped.

imec GaN-IC on SOI 200V and 650V

Options	Standard EUR / block	Discounted EUR / block
Area = 2.5mm x 5.18mm*	15,000	14,200
Area = 5.18mm x 5.18mm	30,000	28,500
Area = 10.54mm x 5.18mm	60,000	57,000
Extra Options		
Extra set of chips (50 samples)	+5,000	+5,000

Important notes: Regular number of samples is 100.
Due to the nature of MPW logistics, more chips than ordered may sometimes be shipped.
*This option is only available to academic institutions.

LioniX SiN-Photonics TriPleX

Options	Standard EUR	Discounted EUR
LNX TriPleX VIS (4 samples of 8mm x 24mm or 2 samples of 16mm x 24mm)	16,000	8,500 [1]
LNX TriPleX 1550 (4 samples of 16mm x 16mm or 8mm x 32mm)	16,000	8,500 [1]
LNX TriPleX 850 (20 samples of 5mm x 10 mm)	16,000	8,500 [1]

Important notes: For academic customers, the discount on the device manufacturing is offered on the condition that LioniX International will be co-author or aknowledged in the publications related to these devices.

MEMSCAP

Technology	Standard EUR / block	Discounted EUR / block
PolyMUMPs (10mm x 10mm), SOIMUMPs (11 mm x 11mm), PiezoMUMPs (11mm x 11mm)	3,700	3,500