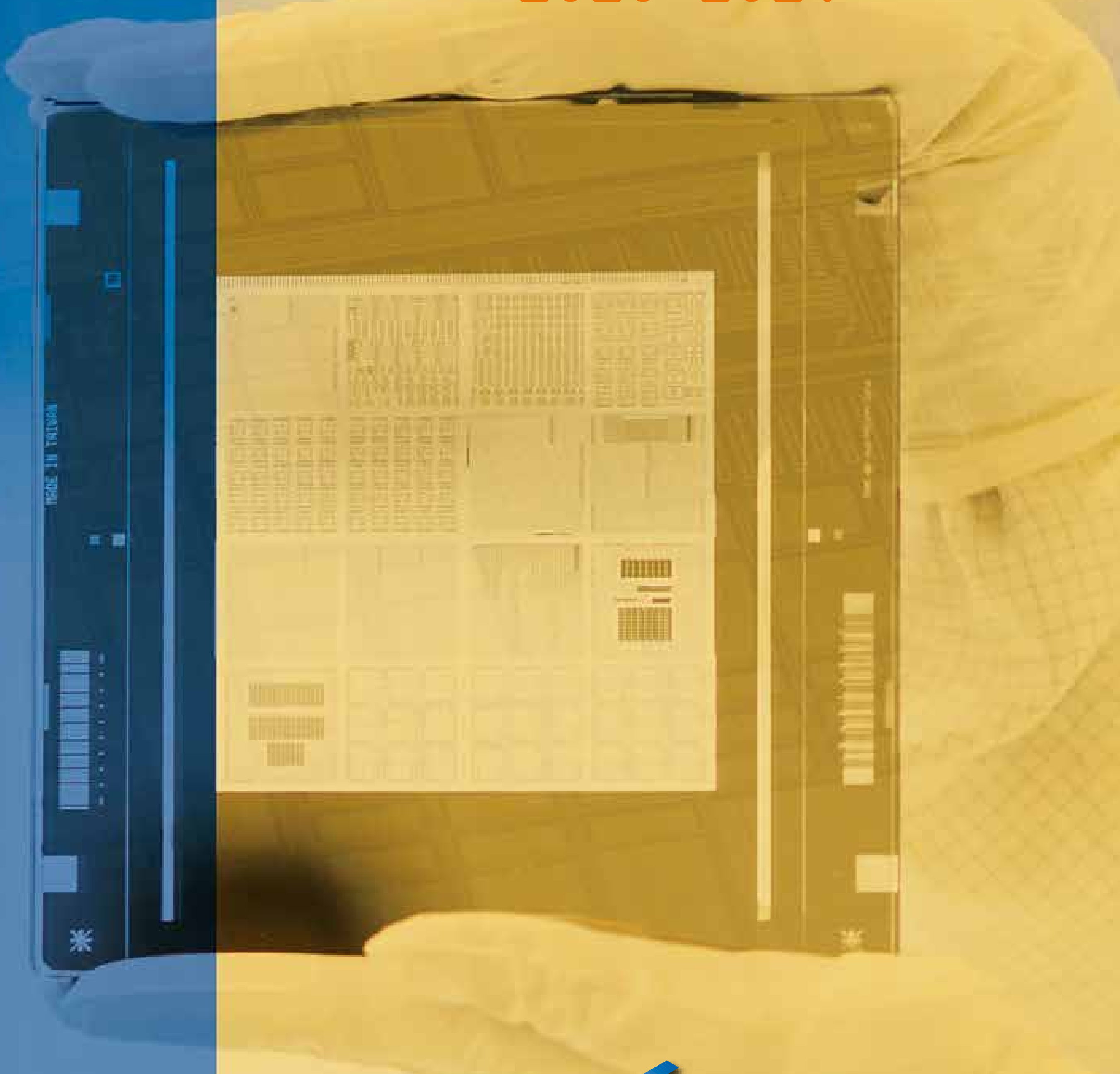
ACTIVITY REPORT

2020-2021



EUROPRACTICE


EUROPRACTICE
The access point to develop
electronic components and systems
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FOREWORD

Dear customers, colleagues and friends,

What a year it has been! Who could have imagined that a worldwide pandemic would fall upon us in 2020. We sincerely hope that you have all managed to stay safe during this turbulent period. Even though it has been an unusual and difficult time, EUROPRACTICE has uninterruptedly continued to support its customers with access to microsystem technologies. The achievements obtained in 2020 are summarized in the new EUROPRACTICE Activity Report 2020-2021, which is in your hands now. We hope you will enjoy reading it and looking forward together with us to the new year where we can slowly return to normality.

Even though the majority of ***2020*** was affected by a global pandemic and related restrictions, it has been a very busy year. We realized a total of ***896 design submissions*** in a wide range of technologies with 80% of the designs submitted by European universities, research institutes and companies. EUROPRACTICE offers a good technology mix for its customers. Advanced technologies, older technology nodes and More-than-Moore technologies are all used in significant volume by our customers. Notably, the total number of design submissions is slightly higher than for the previous year, which is remarkable for such an unusually difficult year as 2020. It demonstrates that research and innovation could continue at the same pace, and EUROPRACTICE together with its foundry partners have continued to support its customers despite the COVID-19 restrictions.

In ***2020***, the outreach activities from EUROPRACTICE were severely impacted by the global pandemic. Except for MEMS2020 and ISSCC2020, which were organized in January and February, all other conferences and exhibitions had to turn to a virtual format. Such online conferences and fairs have proven to be not as effective as their physical counterparts. EUROPRACTICE anticipated this by increasing its digital presence. For instance, regular news and updates were posted on our EUROPRACTICE LinkedIn account focusing on enlarging and strengthening our user community. Next to that, different webinar series were organized to create awareness in emerging fields such as Silicon Photonics, Microfluidics and Advanced Packaging. The majority of those webinars are uploaded to our YouTube channel, where anyone interested in those topics can watch them at their convenience. When it became clear that COVID-19 restrictions would remain for some considerable time, existing physical training courses were reconfigured and adapted so they could be presented online as live instructor-led training including (where appropriate) hands-on practical sessions using remotely accessible design tool environments.

In ***2021***, EUROPRACTICE will continue to deliver a high-quality service to customers. Thanks to the results of the customer survey, which has been conducted at the end of last year, we know even better how we can improve and enhance our services for the entire user community. Customers can access new technologies which were recently added to our portfolio, such as the Si-Photonics processes from LioniX International and CORNERSTONE. New virtual training courses and webinars will be developed and presented to a broad range of users, including traditional electronic sectors and non-traditional sectors (such as MedTech). Moreover, in 2021 the enhanced service offering towards smart system integration will be put more in the spotlight. Ultimately, EUROPRACTICE will act as a true one-stop shop for technologies enabling fully integrated systems and providing direct routes for industrial up-scaling of those systems. Consequently, it will contribute to creating and sustaining new jobs in Europe, especially in the areas of design and fabrication of microelectronic components and systems.

We thank the European Commission (DG Connect) for their support. In 2021, we will work towards an extension of our program within Horizon Europe. The EC funding ensures that we hold our commitment to continue the EUROPRACTICE service and to offer the European academic institutions and SMEs easy and affordable access to state-of-the-art design tools and IC technologies.

Finally, we thank all of you – our academic and industrial customers, our technology and design tool suppliers – for supporting our services, and we wish you all a more 'normal' 2021.

Looking forward to supporting your innovative projects and creating more success stories together.

Romano Hoofman (EUROPRACTICE General Manager)
On behalf of the entire EUROPRACTICE team at imec, UKRI-STFC, FhG-IIS, CMP and Tyndall

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EUROPRACTICE SERVICES

THE ACCESS POINT FOR ELECTRONIC COMPONENTS AND SYSTEMS

EUROPRACTICE offers a platform to develop electronic circuits and smart integrated systems. For more than 25 years, we have provided the European academia and industry with affordable access to a wide range of CAD tools, training courses and state-of-the-art fabrication technologies. We support customers in all critical steps on the way from prototype design to volume production.

OUR OFFER

A true one-stop shop, EUROPRACTICE provides all range of services needed to design and fabricate electronic devices and systems, complemented by extensive customer support:

- Affordable access to industry-standard and state-of-the-art design (CAD) tools, especially for European academia and SMEs
- Prototyping in multiple technologies, such as ASICs, Photonics and MEMS, via Multi-Project-Wafer (MPW) runs
- Smart system integration and advanced packaging
- Route to a small-volume production, including test and characterization services
- Training courses and webinars in design flows and on various technologies

OUR STORY

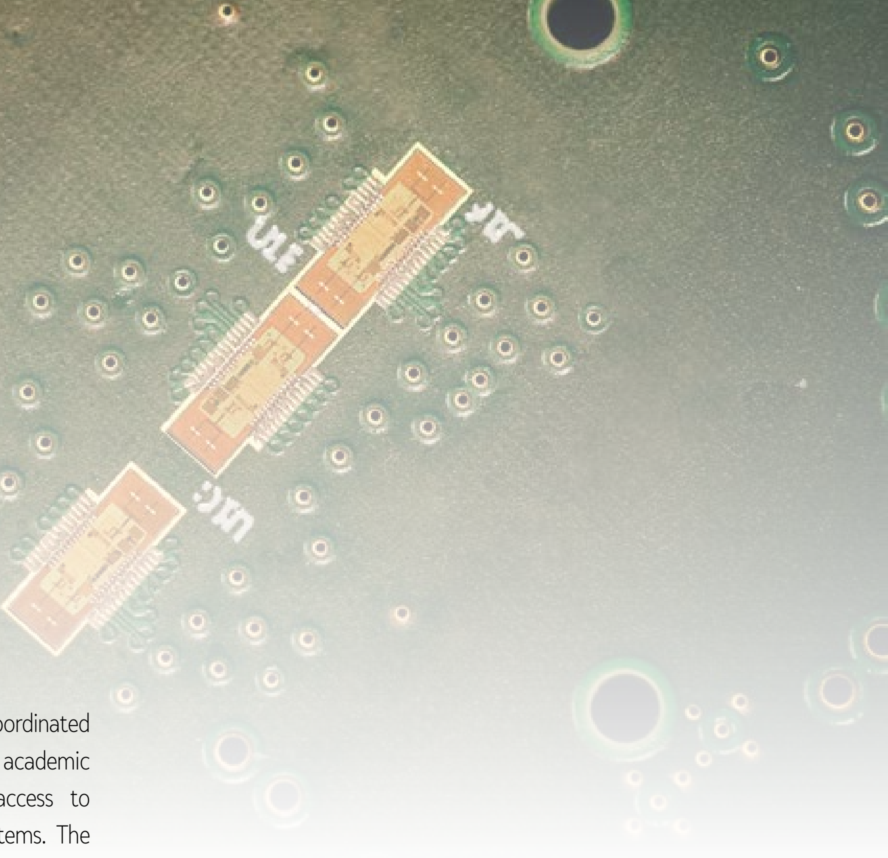
EUROPRACTICE was launched by the European Commission in 1995 succeeding its forerunner EUROCHIP (1989-1995). The service aimed to enhance European industrial competitiveness in the global marketplace by opening easy access to design tools and IC prototyping.

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by supporting more than 600 European universities and research institutes, and over 300 SMEs.

Our current consortium members are imec (Belgium), UKRI-STFC (UK), Fraunhofer IIS (Germany), CMP (France) and Tyndall (Ireland). The two latter partners have joined the EUROPRACTICE consortium and reinforced it with their expertise at the start of the NEXTS project.

NEXTS is a three-year H2020 project funded by European Commission, addressing the call topic ICT-07-2018: Electronic Smart Systems (ESS). NEXTS stands for "Next EUROPRACTICE eXtended Technologies and Services" as it continues and expands a well-established EUROPRACTICE service portfolio.

In NEXTS, we extend our support to the European SMEs and startups, in particularly those originating from universities and research labs. In addition, we encourage customers to adopt Smart System Integration to discover new technologies that enable new application possibilities.



EUROPRACTICE BUSINESS MODEL

The EUROPRACTICE business model is based on a coordinated brokerage service for industrial companies and academic institutions who look for affordable and easy access to technologies in the domain of electronic smart systems. The service builds on the many years' experience of five consortium partners: imec, UKRI-STFC, Fraunhofer IIS, CMP and Tyndall.

EUROPRACTICE offers customers technology access through a vast network of suppliers that includes design-tool and IP-library vendors, foundries, assembly and test houses – who all provide state-of-the-art industry-grade technologies.

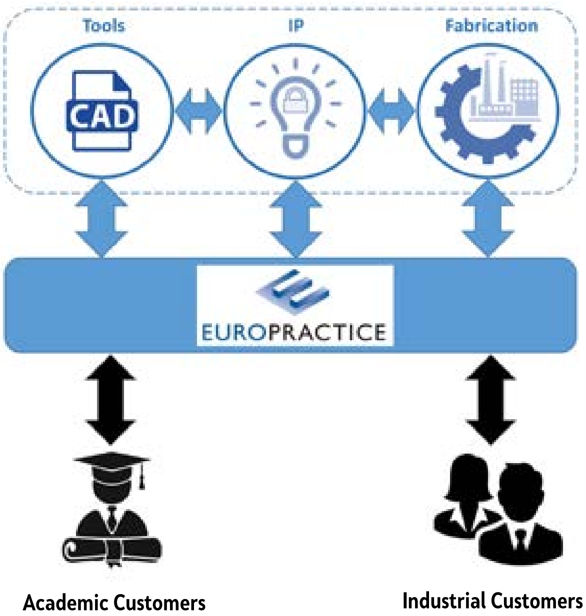


Fig. 1: Schematic representation of the entire EUROPRACTICE ecosystem, depicting a central role of the EUROPRACTICE service as prime interface between the technology suppliers (on top) and the customers (at the bottom).

The overall concept is that EUROPRACTICE acts as the prime interface between the customers and the technology providers. Such a prime interface (or one-stop function) has advantages for both the supply and demand side of the value chain. It is schematically represented in Figure 1, where the supply side is depicted on top, the demand side at the bottom and EUROPRACTICE in the center.

The supply side corresponds with the current service portfolio, where design tools are provided by design tool vendors, IP by dedicated library vendors and fabrication services by various foundries. In addition, the portfolio is extended with emerging technologies typically offered by leading research institutes, and technologies brokered by other service providers (such as CMC in Canada for Silicon Photonics by AMF).

Although EUROPRACTICE represents a large customer base, it is considered as one user by its suppliers. Design tool vendors, IP-vendors and foundries need to deal only with EUROPRACTICE to have their products and technologies promoted and securely distributed all over Europe. Thanks to this, EUROPRACTICE has been able to negotiate technology access on very favorable terms for its customers. This would not be possible when operating on a national level with only few users. Since the service functions on a pan-European level, the know-how and experience has only to be built up once.

AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated lower prices with the major design tool vendors world-wide, as well as with IP and programmable device vendors. Consequently, European academic institutions can access EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics etc.) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows our customers to participate in EC-funded projects, ranging from IP block and component design to complete system design.

DESIGN TOOLS FOR SMEs

European SMEs can access certain design tools at low cost via EUROPRACTICE in order to produce a proof-of-concept IC to demonstrate their IP/product. The resultant IP can then be fully commercialized for an additional agreed fee. The SME gains access to an industry-standard full IC design flow, suitable for all IC technologies.

EUROPRACTICE works flexibly with academic institutes and SMEs to facilitate effective innovation. For instance, we have mechanisms in place if an academic institute has developed a design using EUROPRACTICE tools and subsequently wishes to exploit this design commercially, either via a spin-out or by transferring the IP to an existing SME.

EASY ACCESS TO PROTOTYPING FOR ASICS, MEMS AND PHOTONICS

In general, it is challenging for academic institutes and small companies to obtain access to foundry fabrication lines since they often need a high level of technical support and require only a small-volume production for prototyping purposes.

Over the last decades, leading IC-foundries have recognized that EUROPRACTICE is the ideal partner to offer low-cost prototyping services to smaller users and academia as EUROPRACTICE is the entity that offers technology access, fabrication services and technical support.

The current portfolio includes a wide range of technologies, such as ASIC processes ranging from 0.7µm to 12nm, MEMS, Si-Photonics and SiN-Photonics. The ASIC processes contain digital logic, RF, mixed-signal and high-voltage solutions.

Currently, seven of the nine ASIC foundries (namely, ams, EM Microelectronic, GLOBALFOUNDRIES, IHP, ON Semiconductor, STMicroelectronics and X-FAB) have manufacturing facilities in Europe and most of Si-photonics fabrication takes place in IHP, imec and CEA-Leti, where the last two are leading European RTOs. Over the past year, the Photonics offer has been complemented with the platforms of two more European foundries: LioniX International and CORNERSTONE.

The cost of producing a new IC for a dedicated application within a small market can be high, if directly produced by a commercial foundry. EUROPRACTICE has reduced the prototyping cost, especially for ASIC prototyping, by two techniques: Multi-Project-Wafer (MPW) runs and Multi-Level Masks.

MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto the same mask set of a prototype run, known as Multi-Project-Wafer (MPW) run, the high cost of the mask set and the fabrication process is shared among the participating customers.

Fabrication of prototypes can therefore be as low as 5% to 10% of the cost of a wafer run for only one dedicated customer. A limited number of IC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function “right first time”. To achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the designs fabricated for educational purposes are much smaller than the minimum block size on regular MPW runs, the concept of **mini@sic** was introduced in 2003. This solution allows to further lower prototype fabrication costs compared to standard MPW runs. The mini@sic principle is based on the following methodology: Several times per year, a foundry standard MPW block is bought and resold in smaller and cheaper sub-blocks or mini@sics. This program has been extended over the years and currently includes selected technologies from GLOBALFOUNDRIES, IHP, ON Semiconductor, TSMC, UMC and X-FAB.

At the end of 2020, EUROPRACTICE has introduced a new ultra-flexible pricing solution for mini@sics in the most popular TSMC technologies. The minimum areas for customers have been significantly reduced (for instance, down to 1mm^2 for TSMC 28nm and 65nm) and their X and Y dimensions have become free to choose.

TECHNOLOGY PORTFOLIO

In 2020, technologies of two new foundries have been added to the EUROPRACTICE portfolio: LioniX International and CORNERSTONE.
For 2021, EUROPRACTICE will continue to extend and update its technology portfolio.
Currently, customers can have access to prototype and production fabrication in the following technologies:

ams

- ams 0.35µm CMOS C35B4C3
- ams 0.35µm CMOS C35OPTO + BARC Diode option
- ams 0.35µm HV CMOS H35B4D3
- ams 0.35µm SiGe-BiCMOS S35
- WLSCP for ams C35B4C3

em microelectronic

- EM Microelectronic 0.18µm EMALPC18 logic

GLOBALFOUNDRIES

- GF SiGe 8XP
- GF 130nm BCDlite
- GF 130nm LP
- GF 55nm LPe-RF/LPx-NVM
- GF 45RFSOI
- GF 40nm LP/LP-RF/RF-mmWave
- GF 28nm SLP/SLP-RF
- GF 22nm FDSOI
- GF 12nm LP+

ihp

- IHP SGB25V 0.25µm SiGe:C
- IHP SG25H3 0.25µm SiGe:C
- IHP SG25H5_EPIC (BiCMOS + Photonics)
- IHP SG25 PIC (Photonics)
- IHP SG13S 0.13µm SiGe:C
- IHP SG13C 0.13µm SiGe:C
- IHP SG13G2 0.13µm SiGe:C
- IHP SG13G2Cu FEOL + Cu BEOL option
- IHP SG13SCu FEOL + Cu BEOL option
- IHP BEOL SG13

ON Semiconductor

- On Semi 0.7µm C07M-D
- On Semi 0.7µm C07M-A
- On Semi 0.7µm C07M-I2T100 100V
- On Semi 0.5µm CMOS EEPROM C5F & C5N
- On Semi 0.35µm C035U
- On Semi 0.35µm C035-I3T80U 80V
- On Semi 0.35µm C035-I3T50U (E) 50V
- On Semi 0.35µm C035-I3T25U 3.3/25V
- ONC18MS 0.18µm
- ONC18MS-LL 0.18µm
- ONC18HPA 0.18µm
- ONC18-I4T 0.18µm 45/70V

ST life.augmented

- ST 28nm CMOS28FDSOI
- ST 55nm BiCMOS055
- ST 65nm CMOS065
- ST 130nm BiCMOS9MW
- ST 130nm HCMOS9GP
- ST 130nm HCMOS9A
- ST 0.16µm BCD8sP
- ST 0.16µm BCD8s-SOI

tsmc

- TSMC 0.18µm CMOS Log/MS/RF (G)
- TSMC 0.18µm CMOS HV BCD Gen II
- TSMC 0.13µm CMOS Log/MS/RF (G, LP)
- TSMC 90nm CMOS Log/MS/RF (G ,LP)
- TSMC 65nm CMOS Log/MS/RF (G, LP)
- TSMC 40nm CMOS Log/MS/RF (G, LP)
- TSMC 28nm CMOS Log/RF HPC/HPC+
- TSMC 16nm CMOS Log/RF FinFET Compact

UMC

- UMC L180 Logic GII, MM/RF
- UMC L180 EFLASH Log GII
- UMC L130 Log/MM/RF
- UMC L110AE Log/MM/RF
- UMC L65N Log/MM/RF (SP)
- UMC L65N Log/MM/RF (LL)
- UMC 40N Log/MM – LP
- UMC 28N Log/MM – HPC

xfab

- X-FAB XH035 0.35µm HV
- X-FAB XH018 0.18µm HV NVM E-Flash
- X-FAB XT018 0.18µm HV SOI
- X-FAB XS018 0.18µm OPTO
- X-FAB XP018 0.18 µm NVM
- X-FAB XR013 0.13µm RF SOI
- X-FAB XMB10 MEMS

amf ADVANCED MICRO FOUNDRY

- AMF Si-Photonics

leti CEA tech

- CEA-leti Si-Photonics Si-220
- CEA-leti Si-Photonics Si-310
- CEA-Leti SiN-Photonics Si_3N_4-800
- CEA-Leti MAD200 130nm NVM
- OPEN 3D post-process for 3D integration

CORNERSTONE

- CORNERSTONE Si-Photonics 220 passives/actives
- CORNERSTONE Si-Photonics 340 passives
- CORNERSTONE Si-Photonics 500 passives

imec

- imec GaN-IC on SOI
- imec Si-Photonics Passives+
- imec Si-Photonics ISiPP50G
- imec SiN-Photonics BioPIX 150/ BioPIX 300

LioniX INTERNATIONAL

- LNX SiN-Photonics TriPleX VIS
- LNX SiN-Photonics TriPleX 550
- LNX SiN-Photonics TriPleX 850

MEMSCAP The Power of a Small World™

- MEMSCAP PolyMUMPS
- MEMSCAP SOIMUMPS
- MEMSCAP PiezoMUMPS

MULTI-LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi-Level Mask (MLM). With this technique the available mask area (for example 20mm × 20mm field for stepper equipment) is typically divided in four quadrants (4L/R : four layers per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is therefore reduced by a factor of four. By adapting the lithographical procedure, it is possible to use one mask four times for the different layers by using the appropriate quadrants. This technique allows to significantly decrease the mask costs.

The advantages of using MLM single user runs are:

- lower mask costs
- an MLM run is organized for one customer
- it can be scheduled for any date since it does not depend on regular MPW runs
- a customer receives a few wafers, resulting in a few hundreds of prototypes

The MLM technique is preferred over MPW runs when the chip area becomes large and when the customer would like to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low volume production.

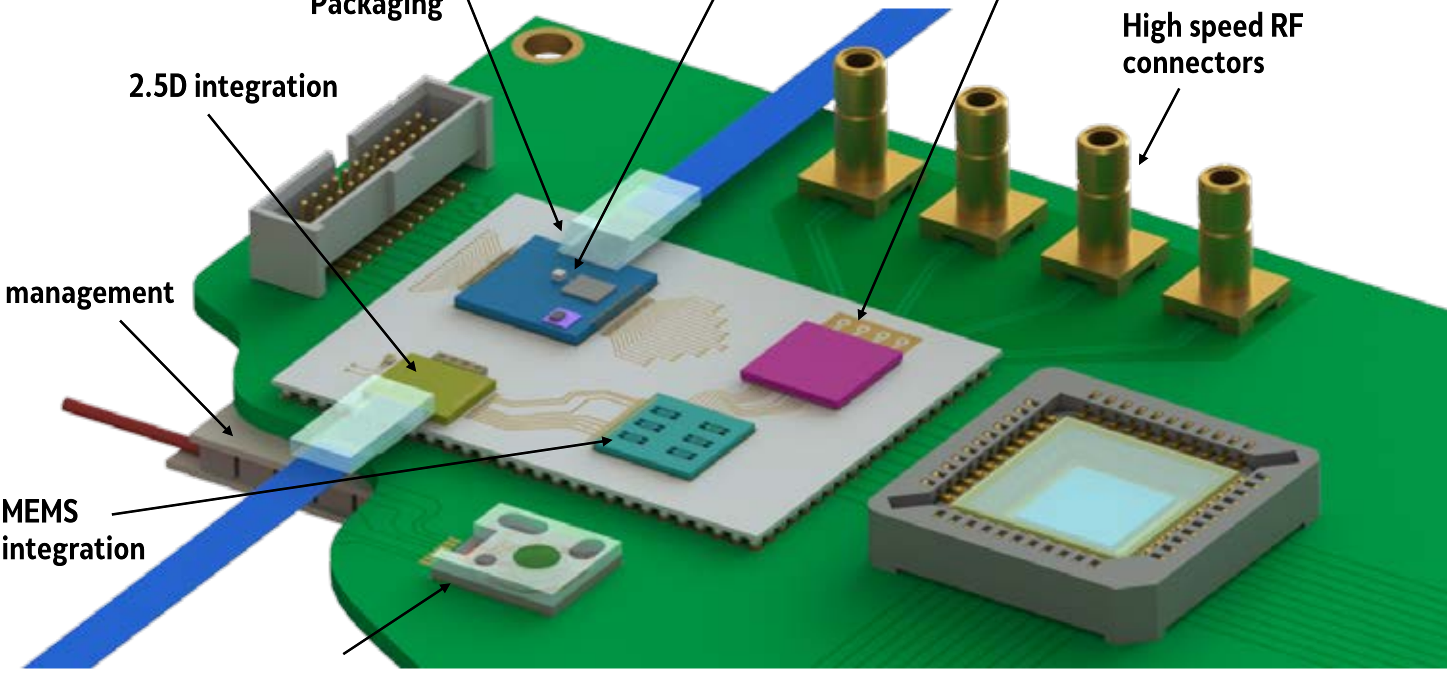
MLM runs are only available for technologies from GLOBALFOUNDRIES, IHP, ON Semiconductor and XFAB.

STANDARD PACKAGING

Standardly, EUROPRACTICE delivers unpackaged untested prototypes. However, EUROPRACTICE offers a low-cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of ceramic and plastic packages are available, ranging from DILs (Dual-in-line) to PGAs (Pin Grid Array) and QFNs (Quad-Flat No-leads).

Side by side with world class partners and our long-term agreements, EUROPRACTICE boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.

In addition, photonics packaging is offered by Tyndall. The photonics ecosystem continues to gather momentum attracting new users (from both academia and industry) and increasing the technical scope of the photonics offering via EUROPRACTICE. Finally, advanced packaging and system integration now complements EUROPRACTICE portfolio.



VIRTUAL DEMO

ADVANCED PACKAGING AND SMART SYSTEM INTEGRATION

There is a growing demand for advanced packaging and system integration in the semiconductor industry. This trend has been fueled by the need from a wide range of applications for better integration of more functionalities in a system-on-chip (SoC) and/or system-in-package (SiP). System integration is a scientific and engineering challenge of combining/putting together a variety of technology modules, such as microsystems, microelectronics, optics, photonics, MEMS, microfluidics and combinations of thereof. Examples of system integration in the semiconductor industry are vast, such as high-speed high-density datacom, artificial intelligence (AI), Internet of Things (IoT), bio-medical devices, sensors and many more.

Currently, the EUROPRACTICE portfolio is being extended with advanced packaging and system integration services enabling customers to realize complex multi-technology devices that can be upscaled from early-stage prototypes to volume manufacturing. This is achieved by adding specific processes or technologies in combination with the development of design rules and thereby facilitating advanced package design for system-on-chip integration.

EUROPRACTICE is showcasing the new system integration offer by means of virtual demonstrators, which are depicted on this page. They demonstrate how different building blocks or process modules make integration between multiple technologies possible. This covers advanced packaging of ASICs, photonics, MEMS, microfluidics and combinations of these technologies, from their design to their fabrication and integration.

System integration is made possible through EUROPRACTICE's unique access to a variety of specialized process modules, including 2.5/3D integration of ASICs and PICs through die stacking techniques using pick-and-place, flip-chip, BGAs, Cu pillars as well as silicon interposers. Access to wafer level fan-out packaging is also provided, where dies from different sources or different technologies with varying thickness and size can be handled and packaged with one integration technology. Finally, add-on processes for noble metal finishes and microfluidic building blocks will be added to the technology portfolio, which are prerequisites for many bio-medical sensor devices. Most importantly, all solutions use industry standard processes making them scalable to high volume and more cost effective.

FROM PROTOTYPES TO VOLUME PRODUCTION

After successful ASIC prototyping, we can also provide customer access to the full production and qualification stage (from low to mid-high volumes).

PROTOTYPE FABRICATION

When all the checks have been performed, the ASIC can be fabricated on one of the MPW's or on a dedicated mask set. EUROPRACTICE takes care of the production for the first prototypes of the customer and organizes the assembly in ceramic or plastic packages if required. Using their own bench tests, the designer can check the functionality of the ASIC in an early stage.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a volume production test program. The test can be performed on both wafer level and on packaged devices. The goal is to reduce the test time and to examine the ASIC for manufacturing problems using the ATPG (Automatic Test Pattern Generation) and functional patterns. EUROPRACTICE supports you during the development of single-site test solution as well as with a multi-site test solution when high-volume testing is required. Based on the test strategy, different solutions can be implemented.

DEBUG AND CHARACTERIZATION

Before going into production, a characterization test program checks if all the ASIC specifications meet the customer's expectations. Threshold values are defined for each tested parameter. The software tests all the IP blocks and the results are verified with the bench test results. A characterization at Low (LT), Room (RT) and High (HT) temperature is performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be strong against process variations, the product qualification can start. EUROPRACTICE can support you through the full qualification process using different kind of qualification flows, including Automotive, Consumer, Industrial, Medical, Space, Military, Jedec and ESCC standards.

In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

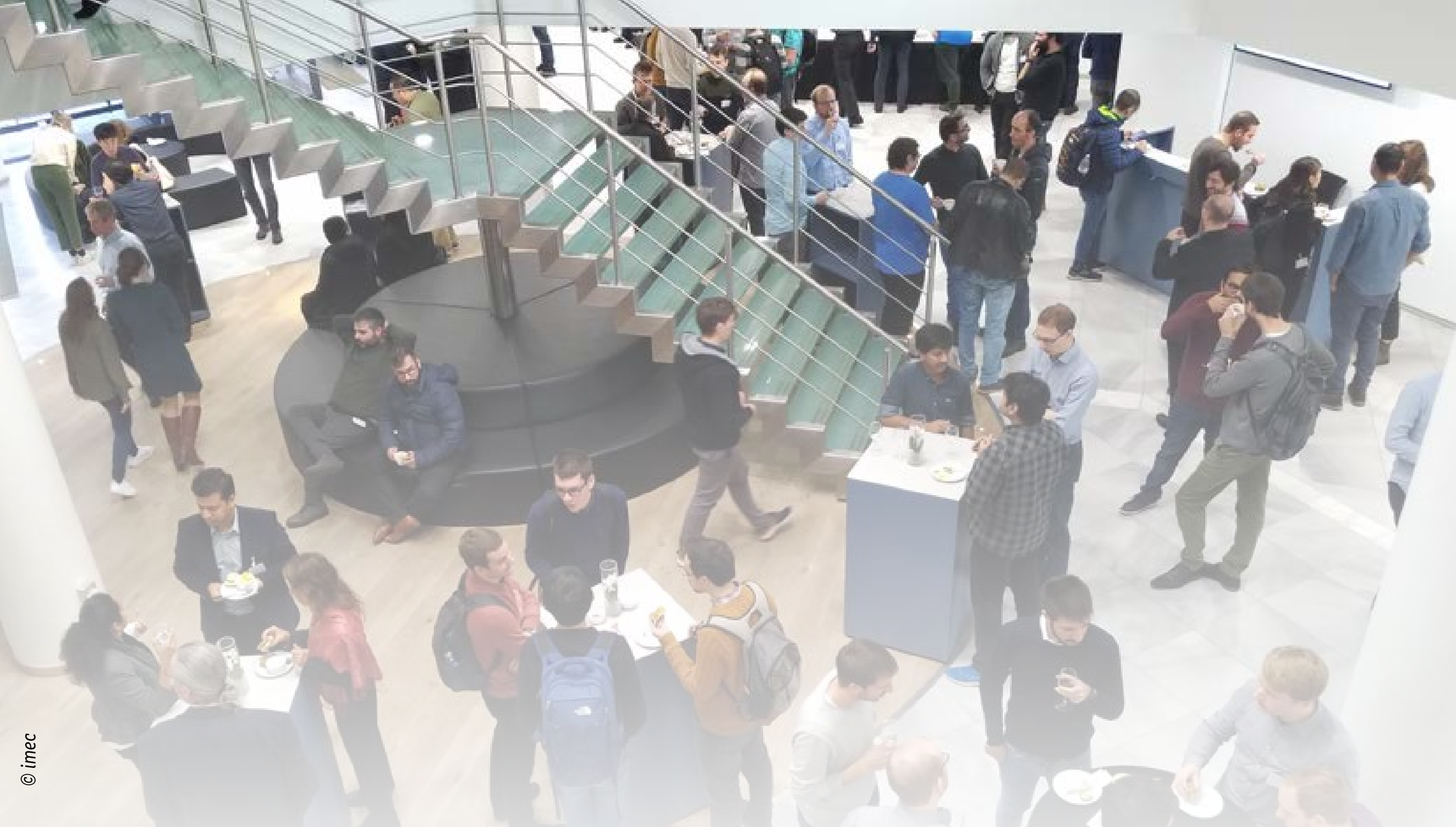
YIELD IMPROVEMENT

EUROPRACTICE can perform yield analysis to determine critical points during the production and suggest the correct solution to maximize the yield. During the characterization and qualification of the device on corner lots, EUROPRACTICE can support the customer in defining the final parameter windows. Depending on the device sensitivity to process variations, the foundry will use the optimal process flow. During the ramp-up phase, data of hundreds of wafers are analyzed to check for yield issues related to assembly or wafer production. EUROPRACTICE is using the well proven tool Examinator™ from Galaxy Semiconductor that enables our engineers to perform fast data and yield analysis studies.

SUPPLY CHAIN MANAGEMENT

EUROPRACTICE is responsible for the full supply chain. This highly responsive service takes care of allocating in the shortest time the customer orders during engineering and production phases. Integrated logistics is applied across the partners to accurately achieve the final delivery dates.
Customer products are treated internally as projects and followed closely by the EUROPRACTICE engineers. Our strong partner's relations empower us to deal with many of the changing requests of our customers. EUROPRACTICE therefore acts as an extension of the operational unit of the customers by providing them a unique interface to the key required sub-contractors.

- **Ceramic assembly partners:** Alter Technology, Kyocera, SERMA Microelectronics, Teledyne e2v
- **Plastic assembly partners:** Amkor Technology, ASE, Greatek Electronics, Integra Technologies, Kyocera, StatsChipPac
- **Wafer bumping partners:** ASE, FlipChip International, Pactech
- **Si-Photonics packaging:** Alter Technology, PIXAPP, Tyndall
- **Test partners:** Alter Technology, Aptasic, ASE, Bluetest, Delta, EAG Laboratories, Salland Engineering, Microtest, RoodMicrotec
- **Failure analysis:** Maser Engineering, RoodMicrotec
- **Library partners:** Aragio, ARM, Cadence, eMemory, Faraday, INVECAS, Synopsys
- **Rad test facility:** LLN, RADEF
- **Tape & Reel:** Reel Service
- **Long-term storage:** HTV



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TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

EUROPRACTICE traditionally has organized high-quality training courses in design tools and technologies. With the beginning of the COVID-19 pandemic, these face-to-face events had to be suspended as of March 2020. To remain in close contact with existing customers and to introduce EUROPRACTICE services to new potential users, highly successful webinar series were organized.

TRAINING COURSES

EUROPRACTICE provides training courses targeting academic staff and PhD students from European universities and research institutes. Unlike training courses which address single topics or individual design tools, the EUROPRACTICE training courses typically address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow.

Since the courses are based on the EUROPRACTICE design tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the EUROPRACTICE infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants have an opportunity to extensively practice the concepts described in lectures and have access to experts who can answer questions about the concepts, design tools or technology processes discussed on the course.

Where a design flow is well supported by multiple vendors and/or processes, multiple course variants are offered that reflect the typical practice within European industry.

Since EUROPRACTICE Training courses began in April 2014, a total of 1285 delegates from 302 Member Institutes in 40 countries have attended 143 training courses making 4585 days of practical training.

Due to the COVID-19 pandemic, physical training courses were suspended from March 2020 onwards. Therefore, existing physical training courses were reconfigured and adapted so they could be presented online as live instructor-led training including (where appropriate) hands-on practical sessions using remotely accessible design tool environments. The consortium partners have also focused on development of webinars.

WEBINARS

Over the past year, EUROPRACTICE has become increasingly involved in developing and hosting webinars. These online sessions were free of charge and open to everyone. They were meant to raise awareness of the constantly growing EUROPRACTICE service portfolio and share valuable technology insights.

Recordings of all webinars in the series on Advanced Packaging, Microfluidics and Si-Photonics are available on the official YouTube channel of EUROPRACTICE Services.

Webinars usually included informative presentations given by experts from world-leading companies, foundries or academic institutions, followed by a short Question & Answer session. To provide useful and interesting content for a broad audience, different webinars were adjusted for participants with different skills, ranging from general overview talks to advanced technical sessions.

Three EUROPRACTICE webinar series including more than 20 episodes took place in 2020:

Advanced Photonics Packaging

This series was created by Tyndall and included seven webinars that were meant to make participants better acquainted with the existing photonics packaging offer provided by EUROPRACTICE services. The first three webinars were broad with a general scope compared to the last four that examined specific technical topics in depth.

Introduction to Microfluidics

This six-webinar series was prepared by imec in cooperation with experts from leading European microfluidic companies. Since the EUROPRACTICE community is traditionally familiar with the design and implementation of devices and circuits in silicon, the main goal of these webinars was enlarging the technical scope of the community and introducing its members to the domain, new for many of them.

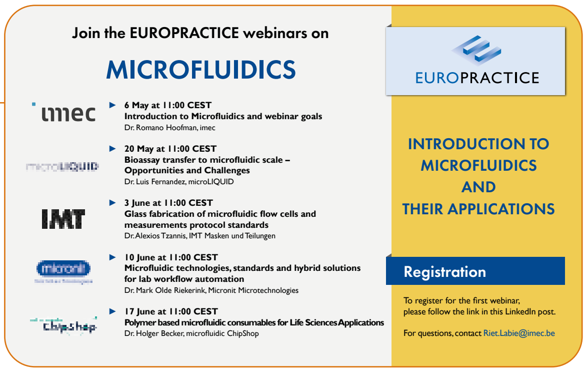
Silicon-Photonics

EUROPRACTICE partners invited speakers from six world-leading Si-Photonic foundries who shared their first-hand insights in six episodes. Each session was dedicated to the technologies of one particular foundry. In their talks, manufacturers shared how they fabricate PICs and what makes their technology unique.

In addition, STFC in partnership with Coventor gave a short highly technical two-webinar series on approaches to **MEMS design**. Further, STFC also organized a webinar that outlined the **design flow for a digital ASIC** to address inexperienced designers, for example new PhD students or others without current ASIC design knowledge.

All EUROPRACTICE webinars were highly popular: The live streamed webinars were attended by 1787 delegates. Including 1388 delegates from EUROPRACTICE member institutions, 94 from potential new EUROPRACTICE member institutions and 194 from European Industry.

For 2021, various new webinars are being planned, for instance a series on MEMS Technologies and Applications will be organized by Tyndall and will take place in March-April.



OUTREACH AND COMMUNICATION

2020 was a very challenging year for communication and outreach activities since majority of face-to face events have been cancelled due to COVID-19 restrictions. To remain in touch with our customers and reach new users, EUROPRACTICE has actively used virtual tools, such as websites, social media and online events.

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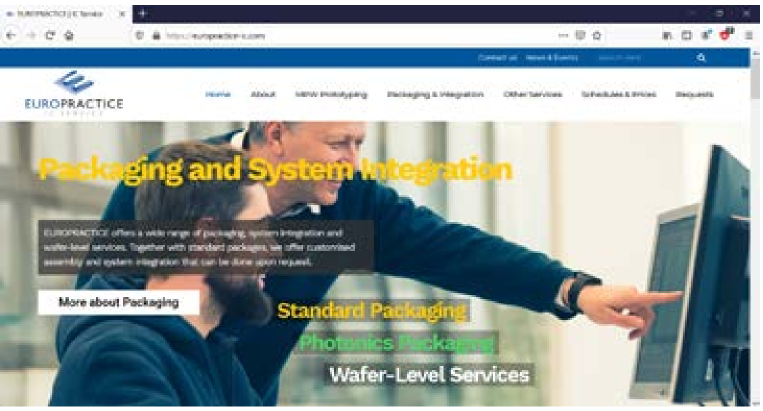
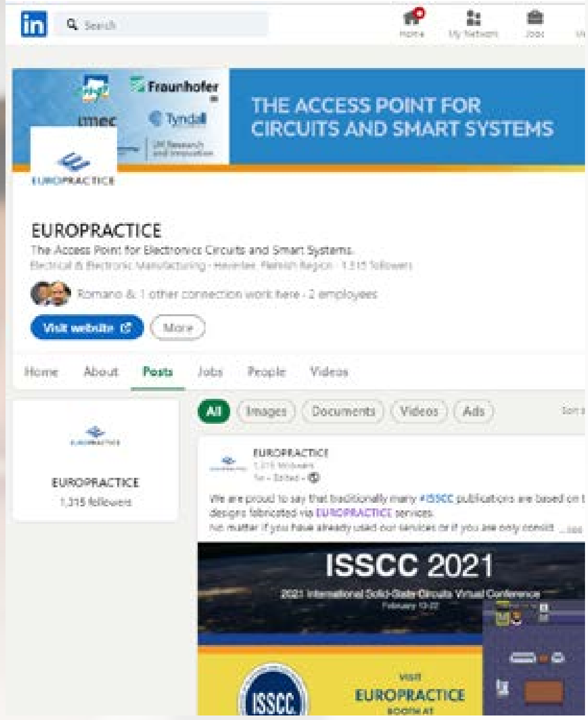
WEBSITES

Information on a very broad and diverse EUROPRACTICE offer is split between two websites that cover different aspects of the service portfolio.

www.europractice-ic.com : The Technology & Fabrication website is regularly updated with the latest news on MPW offer, run schedules and pricing. On this website, visitors can find all information related to fabrication process, including detailed technology descriptions, packaging offer, system integration solutions, volume production and test services. The website is maintained by imec.



www.europractice.stfc.ac.uk : The Design Tool & Training website is hosted and maintained by UKRI-STFC. It presents information related to EUROPRACTICE membership and purchase of design tool licenses. The website also provides a detailed overview of the upcoming training courses and webinars, and a possibility to register for them.

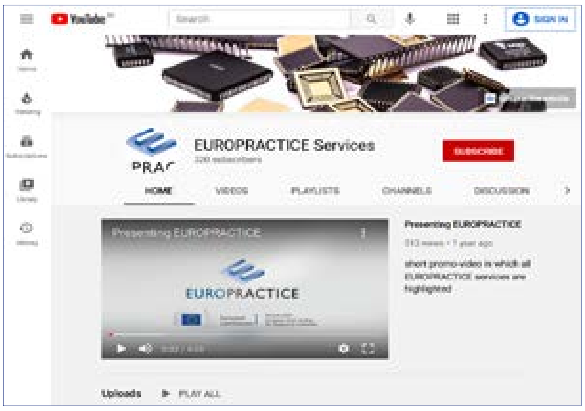


SOCIAL MEDIA

To enlarge and strengthen EUROPRACTICE user community, we started to actively develop accounts on LinkedIn and YouTube. By the end of 2020, we managed to creat a strong presence in both social networks.

LinkedIn

Following EUROPRACTICE on LinkedIn is an effective way for customers to receive most relevant news, such as upcoming webinars, new additions in the technology portfolio and approaching events where participants can meet EUROPRACTICE representatives in person or online. In December 2020, our official LinkedIn account had close to 1300 followers.



YouTube

This channel gives an opportunity to watch all EUROPRACTICE webinars from the series on Advanced Photonics Packaging, Introduction to Microfluidics and Silicon Photonics. It also contains videos introducing EUROPRACTICE services and user stories. By the end of 2020, the channel had 7386 views and 283 subscribers.

EVENTS IN TIMES OF COVID-19

Every year, EUROPRACTICE is present at various scientific conferences, industrial trade shows and fairs in order to present its services to existing customers and to attract new prospects. Although physical events planned for 2020 have been cancelled from March onward due to the COVID-19 outbreak, multiple event organizers have turned to a virtual format.

During last year, EUROPRACTICE participated in several online events with virtual booths, posters and flyers that were developed specifically for these purposes. However, networking and direct interaction with customers remained difficult. As a result, no National Seminars took place in 2020 because active face-to-face networking is their core purpose.

To compensate for the lack of physical outreach and communication opportunities, EUROPRACTICE has been successfully using online communication by means of webinars and social media. In 2021, we are planning to remain in close contact with our customers and prospects. To achieve this, we will keep hosting virtual events, such as new webinar series and an upcoming industry-cluster event co-organized with DSP Valley. In addition, we will attend at least the following conferences and fairs:

EUROPRACTICE team at MEMS2020 in Vancouver.

EUROPRACTICE poster for virtual events.

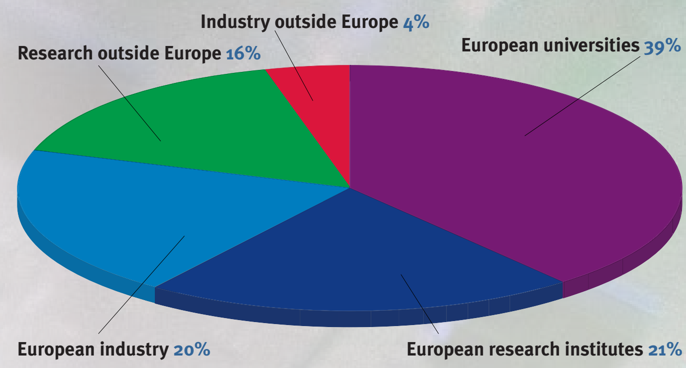
LinkedIn invitation to visit virtual EUROPRACTICE booth at EFECS2020.

ISSCC 2021	Virtual event	13-22 February
SSI 2021	Virtual event	27-29 April
TRANSDUCERS 2021	Virtual event	20-25 June
PRIME 2021	Virtual event	19-22 July
ESSDERC / ESSCIRC2021	Grenoble, France	6-9 September
EFECS 2021	Amsterdam, the Netherlands	23-25 November

RESULTS 2020:
MPW PROTOTYPING SERVICES

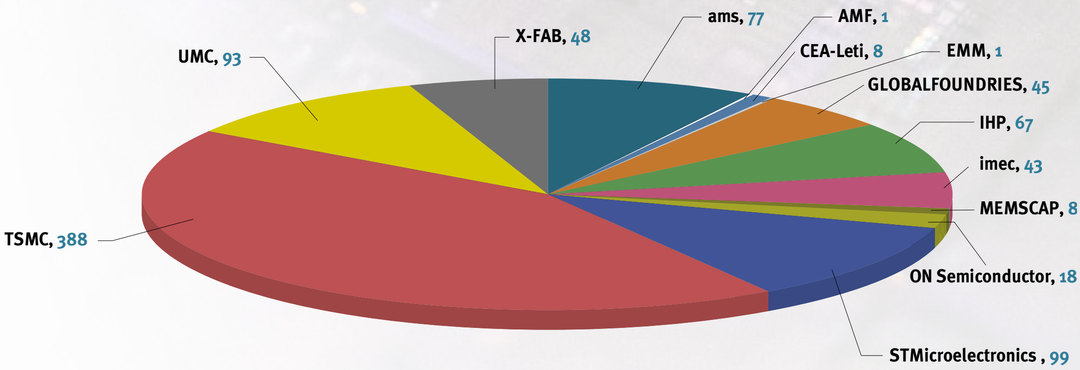
PROTOTYPED CIRCUITS ON MPW RUNS

In 2020, a total of 896 design projects have been submitted for prototyping on EUROPRACTICE MPW runs. This number is slightly higher than for the previous year, which is remarkable for such an unusually difficult year as 2020. It demonstrates that research and innovation could continue at the same pace and EUROPRACTICE together with its foundry partners continued to support its customers despite the COVID-19 restrictions.



MPW designs in 2020

60% of the prototypes were designed by European universities and research institutes, while 20% of the designs are coming from European industry (mainly SMEs). The remaining 20% of the designs are coming from outside Europe, namely 16% from research institutions and 4% from industry.

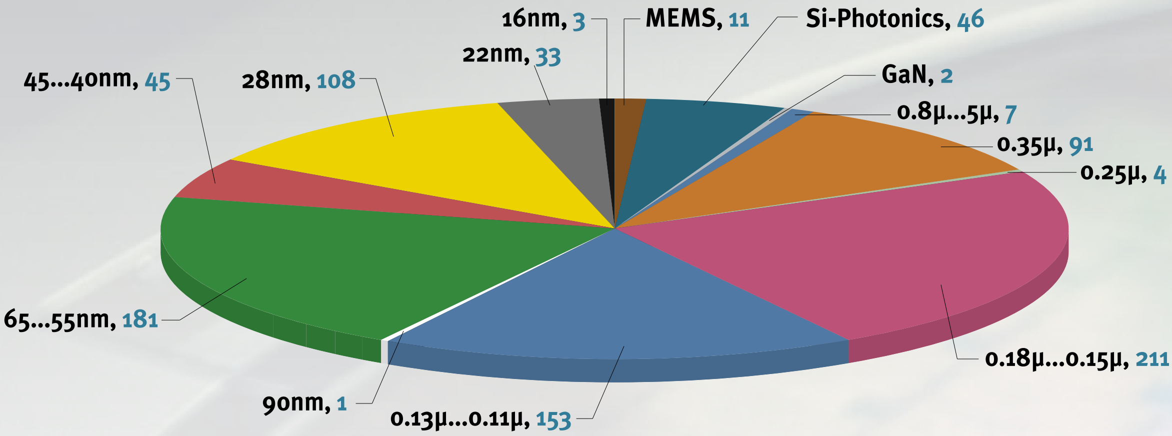


Number of fabricated designs in 2020 per foundry

ACCESS TO TECHNOLOGIES OF WORLD-LEADING FOUNDRIES

EUROPRACTICE provides affordable access to technologies of world-leading foundries (ams, GLOBALFOUNDRIES, ON Semiconductor, STMicroelectronics, TSMC, UMC and X-FAB), complemented by specialty fabs at CEA-Leti, IHP, imec and MEMSCAP. This year, the first design projects were submitted in AMF and EM Microelectronic technologies. Similar to last year, most of the submitted designs in 2020 were fabricated in TSMC, which is also the leading foundry for the global industry.

Remarkably, two of the European foundries – STMicroelectronics and austriamicrosystems (ams) – have the second and fourth largest number of designs fabricated. One of the other European foundries, X FAB, has increased its number of fabricated designs once again as compared to last year(s).



Number of fabricated designs in 2020 per technology (node)

GOOD TECHNOLOGY MIX

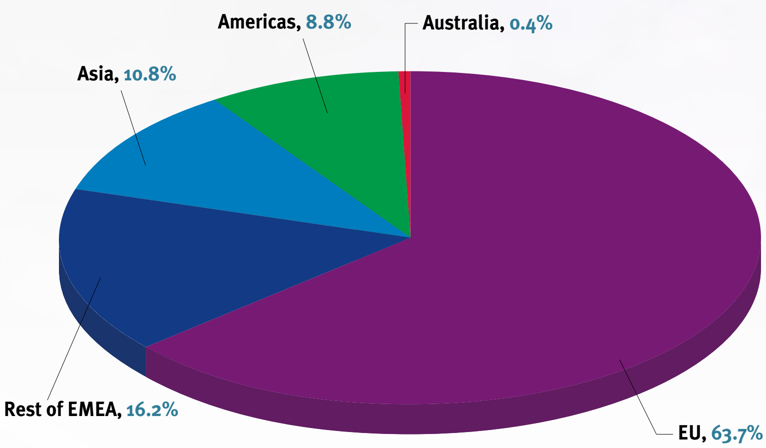
EUROPRACTICE offers a good technology mix to its customers. Advanced technologies, older technology nodes and More-than-Moore technologies are all used in significant volume by the EUROPRACTICE customers. The older technology nodes (ranging from 0.11µm to 0.8µm) are still very popular and represent approximately half of the total designs submitted. For the more advanced nodes, 65nm and associated nodes are the most popular with 181 fabricated designs.

In addition, the 28nm technology node is used very frequently by the customers and its share has significantly grown compared to last year. 33 designs in total were realized in 22nm nodes. The 22nm FDSOI technology from GLOBALFOUNDRIES has once again shown tremendous growth in the number of designs, as it has more than doubled the figures: from 15 last year to 33 this year. The access to 16nm FinFET technology from TSMC can only be offered to a restricted set of customers, reflected by only 3 prototypes in 2020.

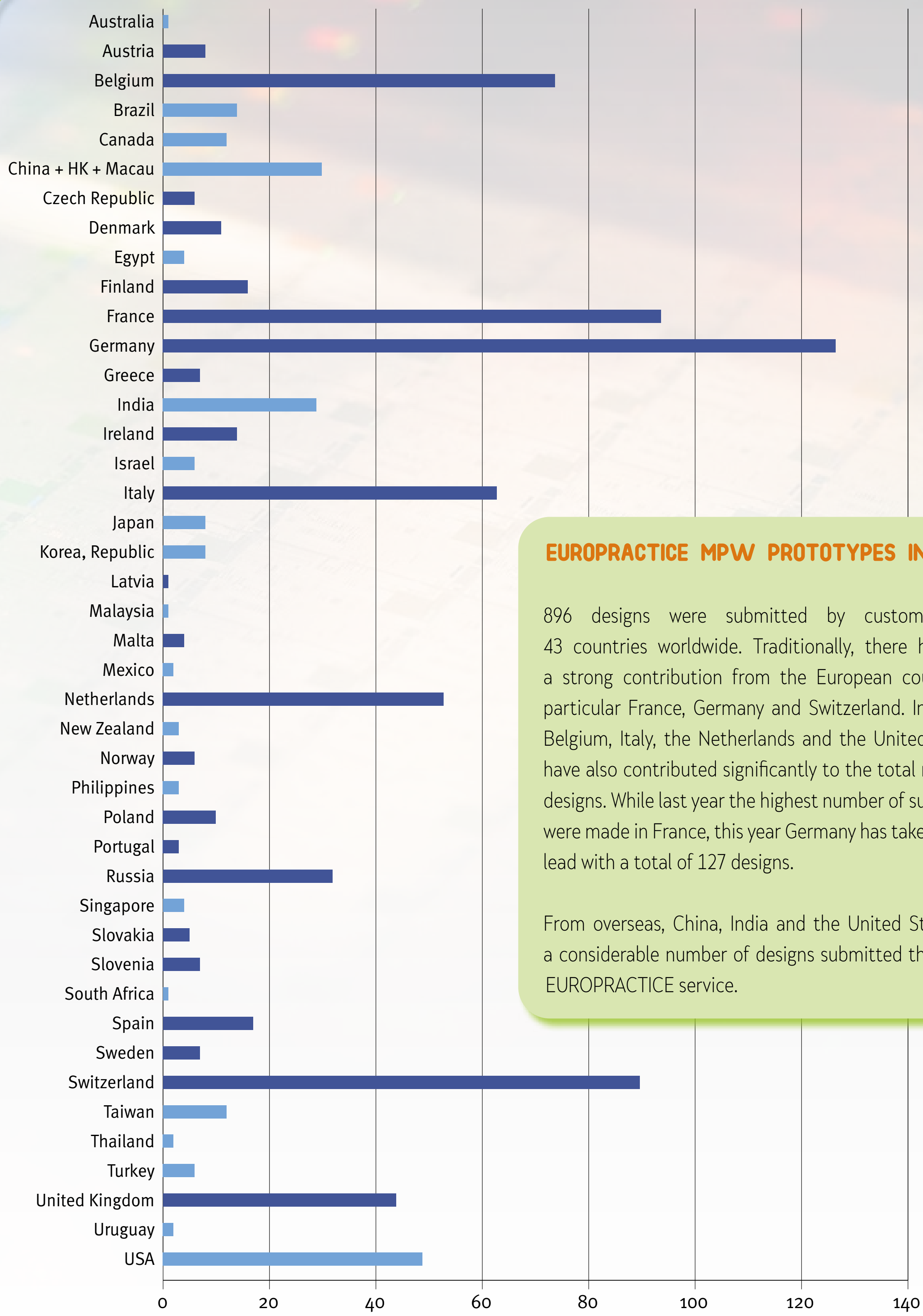
The number of designs in Silicon Photonics technologies has mildly decreased due to a reduced number of designs in the imec Si-Photonics technologies in the first half of the year. It seems that those technologies were the only ones who saw an impact of the COVID-19 pandemic. The number of MEMS designs has slightly increased thanks to the X FAB XMB10 design competition. Finally, 2 designs have been fabricated in the GaN-IC technology, which was added only last year to the EUROPRACTICE technology portfolio.

GEOGRAPHICAL DISTRIBUTION

Although EUROPRACTICE focuses mainly on European customers, its services are also accessible for customers outside Europe. 64% of the fabricated designs are coming from the European Union and another 16% from other countries in the EMEA (Europe, Middle East and Africa) zone. A significant number of customers from Asia are also using the EUROPRACTICE prototyping services – representing a total volume of 97 designs in 2020. Finally, the remaining 9% of the designs fabricated are coming from the Americas and the Australian continent.



Geographical distribution of MPW designs in 2020

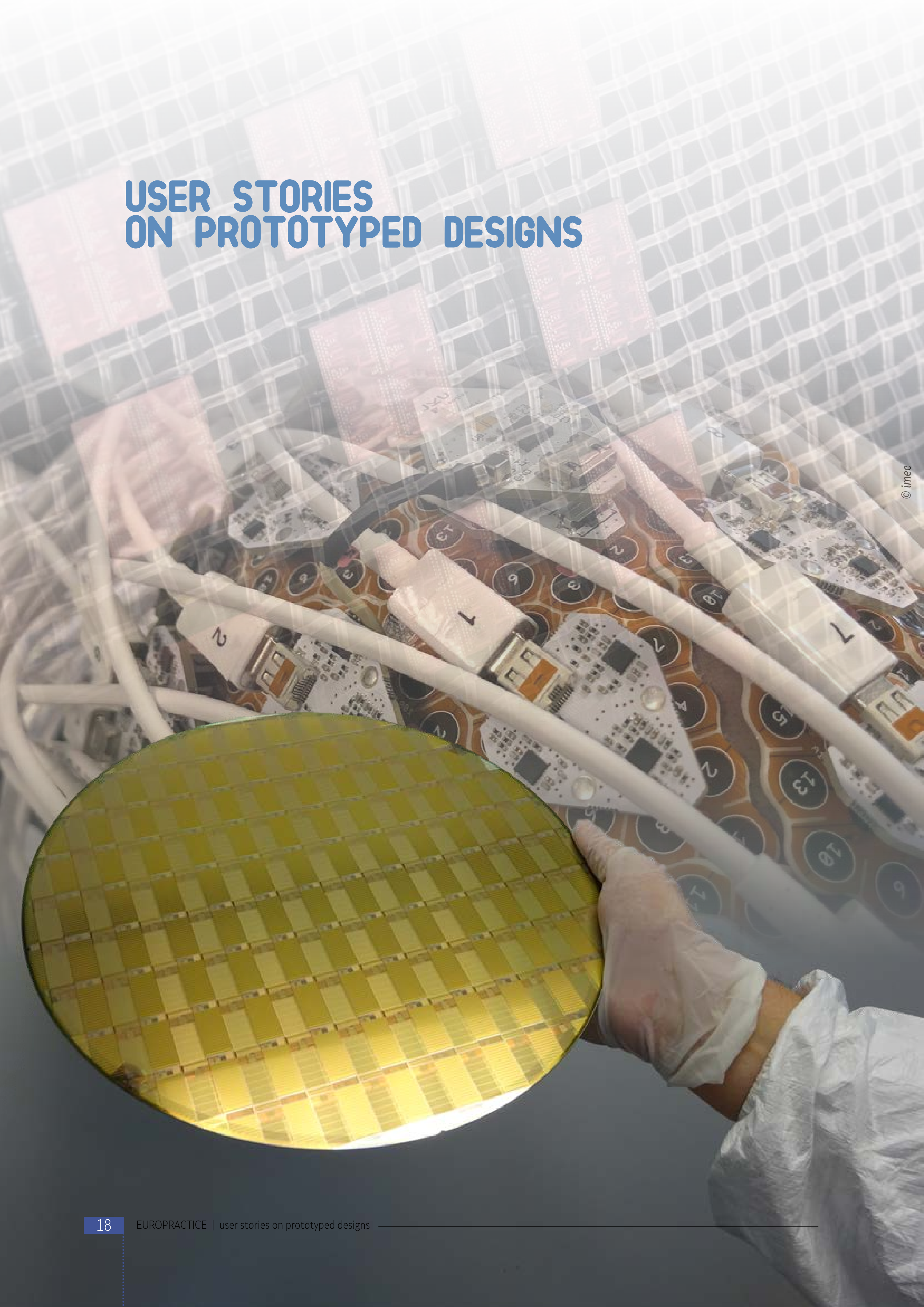


EUROPRACTICE MPW PROTOTYPES IN 2020

896 designs were submitted by customers from 43 countries worldwide. Traditionally, there have been a strong contribution from the European countries, in particular France, Germany and Switzerland. In addition, Belgium, Italy, the Netherlands and the United Kingdom have also contributed significantly to the total number of designs. While last year the highest number of submissions were made in France, this year Germany has taken over the lead with a total of 127 designs.

From overseas, China, India and the United States have a considerable number of designs submitted through the EUROPRACTICE service.

USER STORIES ON PROTOTYPED DESIGNS



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Warm front-end for X-ray cryogenic detectors

APC Laboratory, Paris, France

Contacts: Damien Prêle, Si Chen
E-mail: prele@apc.in2p3.fr
Technology: ams SiGe BiCMOS 0.35µm S35D4M5
Die size: 26.146 mm^2

Introduction

AwaXe_v3 (Athena Warm Asic for the X-ifu Electronics - version 3) is an upgrade ASIC developed for the Warm Front End Electronics (WFEE) of a future X-ray observatory: ATHENA, a space mission of ESA.
It is dedicated to an early demonstration model (Phase B) to validate the Time-Division Multiplexing (TDM) readout of the X-IFU (X-ray Integral Field Unit) instrument of the ATHENA telescope. It includes two TDM channels for low noise amplification and the bias of the TES/SQUID cryogenic detection chain.
This ASIC belongs to the "AwaXe and SQmux ASIC families" developed at APC Laboratory for SQUID/TES readout. The development is funded by CNES and CNRS.

Description

AwaXe_v3 integrates two TDM readout channels of the X-IFU instrument. It is a mixed ASIC, mainly composed of:

- 2 identical fully-differential Low Noise Amplifiers (1/CH) to amplify scientific signals, with proper voltage gain ≈170 V/V, bandwidth (-3 dB) ≈24 MHz, ultra-low equivalent input noise < 1 nV/√Hz, low non-linearity <1% and low gain drift < 350 ppm/K in the range of [11°C, 75°C]. Input and output impedance matching is also practicable;
- 10 differential configurable current sources for the bias of SQUIDs and TES (5/CH), with maximum output 3.6mA or 600 µA. 4 of the 10 sources further respectively have an attached fixed current source (2/CH), allowing to have an alternative bias range of [-1.8 mA, 1.8 mA] or [-300 µA, 300 µA]. Current noise has been optimised down to low frequencies (1-100 Hz);

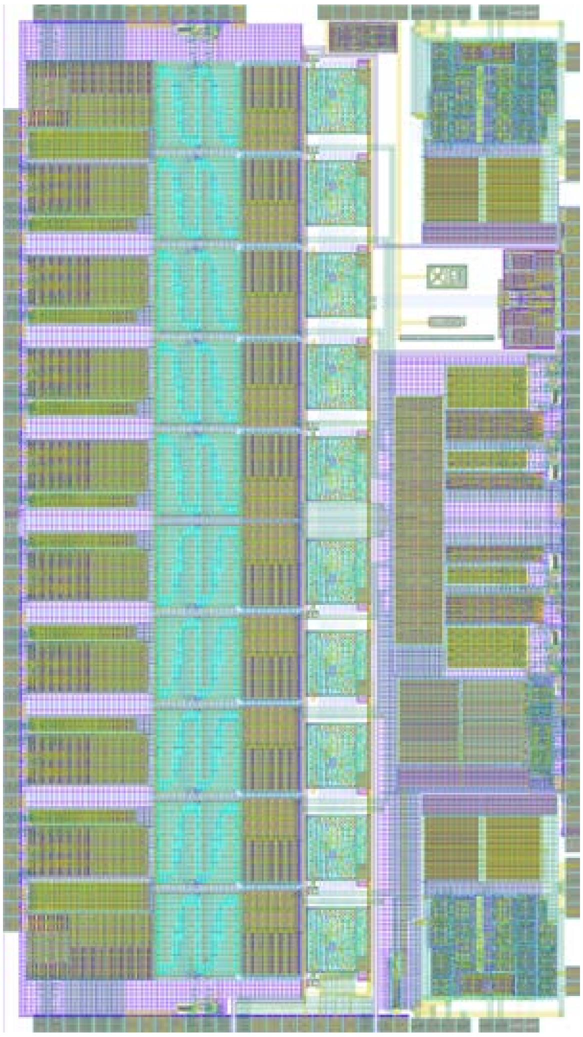


Fig.1: Layout of the circuit.

- A digital RadHard series bus RS485/I2C of 8-bit for the slow control of all 10 configurable current sources;
- Housekeeping elements to monitor temperature, current and voltage of the ASIC;
- 6 heating modules (3/CH) with nominal output 18 mA to heat/deflux cryogenic devices.

Sub 30 GHz VCOs in 22nm FDSOI for radar and communication applications

Institut für Mikroelektronik und Schaltungstechnik, Universität der Bundeswehr München, Germany

Contacts: MSc. Piyush Kumar, Dipl.-Ing Dario Stajic, Prof. Linus Maurer
E-mail: piyush.kumar@unibw.de

Technology: GLOBALFOUNDRIES 22nm FD-SOI 22FDX
Die size: VCO in mm-Wave Spectrum: 345µm × 446µm; push VCO: 448µm × 652µm
Design tools: Cadence IC advance, Mentor Calibre (for DRC, LVS, XACT checks), ADS-Momentum for the EM simulation of the coil

Introduction

Ocean 12 is an ECSEL co-funded project which is an Opportunity to Carry European Autonomous driving further with FDSOI technology. Based on the innovative FDSOI technology to develop new processors and applications design that leverage Fully Depleted Silicon On Insulator (FD-SOI) technology to offer the industry's lowest power integrated circuits, especially for automotive and aeronautic applications.
The Institute for Microelectronic and Integrated Circuit (EIT4) at Universität Der Bundeswehr, München (UniBwM), is focused on realizing the building blocks for the frequency generation of mm-Wave FMCW radars.

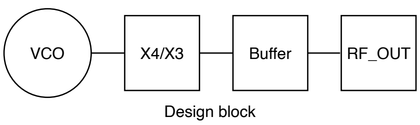


Fig.1: Design block.

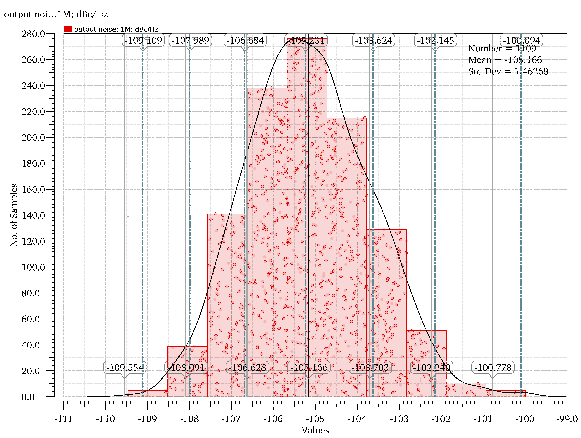


Fig.2: Monte-Carlo analysis to estimate the variation in the Phase noise. of VCO.

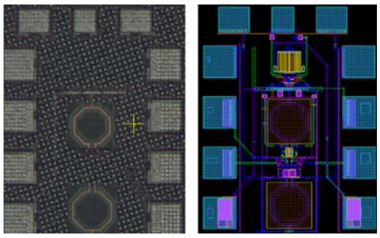


Fig.3: Die Photo and Layout of VCO in mm-Wave Spectrum.

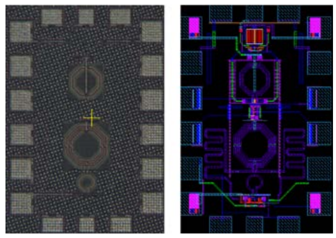


Fig.4: Die Photo and Layout of the Push-Push VCO.

The activities of UniBwM are focused on novel VCO architectures to be integrated with the Frequency Multipliers to efficiently generate signals in the 76 to 81GHz signal band used for automotive radar.

Description

After the successful tapeouts in 2018 and 2019, this year Universität Der Bundeswehr participated in the MPW tapeout from the EUROPRACTICE. We designed stand-alone VCOs and Frequency Multipliers.
The VCOs are based on the modified Collpits-Oscillator and push-push topology. The silicon is verified by wafer-prober measurements and is fully functional.
The UniBwM designed a push-push VCO with the central frequency of 20 GHz. This architecture was chosen as the 2nd harmonic can be further multiplied to the target frequency band. The characterization of this block is in progress.

Why EUROPRACTICE?

EUROPRACTICE offers prototype services and testing for state-of-the-art technologies with mature PDKs at reasonable prices, including modern nanometer scale processes such as GF22FDX, which is used in this project. Without these services we as a University could not participate in such design-centric projects. They also provide excellent support for PDKs and tape-out procedures till the GDS submission.

Acknowledgment

This work was supported through OCEAN12 (Grant Nr 783127) project, receiving funding from H2020 ECSEL JU program and German Bundesministerium fur Bildung und Forschung (BMBF).

OCEAN 12

ECSEL Joint Undertaking

GEFÖRDERT VOM

Bundesministerium für Bildung und Forschung

A D-band Differential Transmission Line Based Power Combiner

Silicon Austria Labs, Linz, Austria

Contacts: Abouzar Hamidipour, Gernot Hueber
E-mail: abouzar.hamidipour@silicon-austria.com
Technology: GLOBALFOUNDRIES 22nm FD-SOI 22FDX
Die size: 1250μm × 1250μm
Design tools: EMX for EM simulations, Spectre for circuit simulations, Calibre for fill generation and merging GDSII files, PVS for DRC/LVS check

Description

With the growing attention to 6G and frequencies beyond 100 GHz, many attempts are being made to explore novel power combining structures. This is to overcome technology limitations in providing conventionally high output power. Traditional approaches of power combining such as Wilkinson or transformer-based have been widely used in lower frequency ranges as their theory is very well-known and their design procedure is straightforward. In frequencies beyond 100 GHz, however, transmission-line based power combiners could be preferred as their size shrinks appreciably and they prove comparatively low insertion loss. To this end, a D-band differential power combiner with 1:1 impedance ratio was designed based on transmission lines in GLOBALFOUNDRIES 22nm FDSOI technology. Transmission lines provide 50 Ω impedance both at the input and the output of the combiner. Figure 1 shows a micrograph of the die and the test structure used to verify insertion loss of the combiner. Impedance matching was accomplished using quarter-wavelength transformers. To fulfill low-characteristic impedance requirements, the signal and ground traces of the strip lines were designed on QA and M1 layers, respectively. As can be seen in Figure 2, a very good agreement was achieved between the simulation and measurement over the whole D-band frequency range.

Why EUROPRACTICE?

EUROPRACTICE provides access to various state-of-the-art technologies at affordable price. Furthermore, EUROPRACTICE staff provide a very good customer service and technical support. The variety of technologies and the frequency of runs create a platform for excellent research opportunities.

Fig. 1: Microphotograph of the test structure used to verify the D-band differential power combiner.

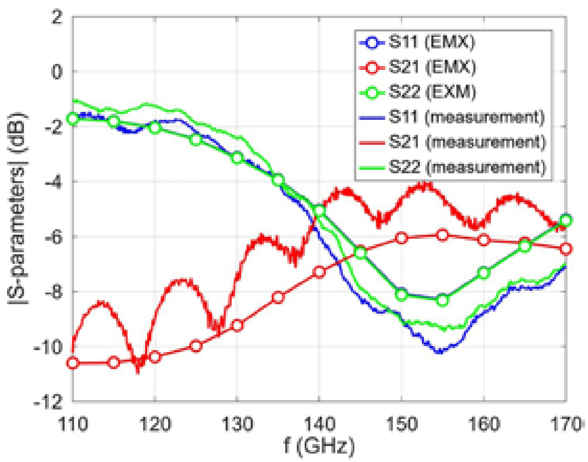


Fig. 2: Measured and simulated S-parameters of the D-band differential power combiner.

140 GHz Transmitter Chip for Pseudo Random Noise Radar in 22 nm FD-SOI CMOS Technology

Institute of Electrical and Optical Communication Engineering (INT) and Institute of Robust Power Semiconductor Systems (ILH), University of Stuttgart, Germany

Contacts: Daniel Widmann, Raphael Nägele, Athanasios Gatzastras
E-mail: daniel.widmann@int.uni-stuttgart.de
Technology: GLOBALFOUNDRIES 22nm FD-SOI 22FDX
Die size: 1.25mm × 1.25mm
Design tools: For designing and simulation Cadence Virtuoso and Spectre were used. For DRC/LVS/PEX Mentor Calibre and xACT were used. ADS-Momentum from Keysight to extract and model inductors.

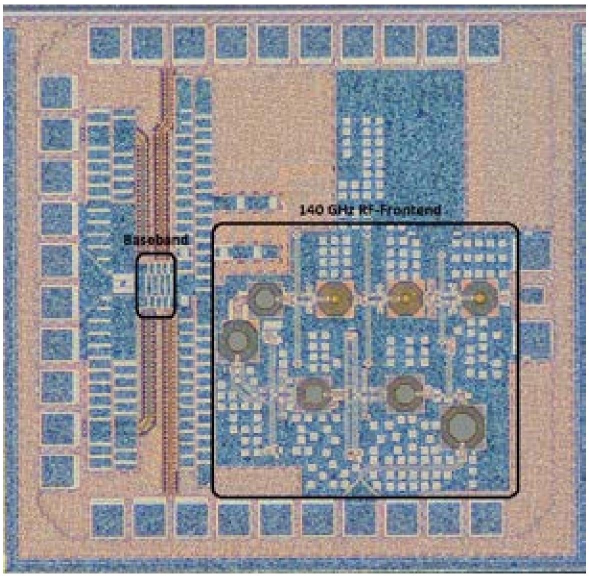


Fig.1: Photo of the PNRADAR Chip.

Description

Compact and inexpensive radar systems are an important prerequisite for advanced driver assistance systems (ADAS) and self-driving cars. Today's radar systems rely on the hybrid integration of RF circuits in SiGe technology with digital circuits in CMOS technology. The progress of technology now allows moving to pure CMOS single-chip solutions that include the digital baseband, A/D and D/A signal converters as well as millimeter-wave circuits beyond 100 GHz on a single IC. In this project a complete mixed signal transmitter integrated circuit in 22 nm FD-SOI CMOS was designed. The target application of the IC are broadband radar systems in which the carrier signal is modulated with a pseudo random noise signal.
The baseband circuitry consists of a digital pulse shaping circuit for binary pseudo random input sequences with a subsequent D/A converter. After digital pre-processing, the symbols are converted to an analog signal by a non-binary D/A converter approaching a raised-cosine shape at very low hardware effort. The method implemented here is an efficient way to perform spectral shaping at low power consumption without complex analog filters.
The RF front-end includes up-conversion and millimeter-wave amplification. The spectral shaped differential IF signal is up-converted by a double-balanced mixer driven by a 140 GHz LO signal. The LO signal is generated out of a 35 GHz source by frequency quadruplication. The up converted differential RF signal passes through an amplifier chain to achieve a sufficient high output power.

Why EUROPRACTICE?

As research institutes specialized in the design of integrated mixed-signal and millimeter-wave circuits, fast access to leading electronic automation tools and state-of-the-art semiconductor technologies is of utmost importance for us. At present, and over the past two decades, we rely on EUROPRACTICE for software licensing, design kit access and particularly IC fabrication in some of the most advanced semiconductor technologies. We deeply value the benefits of being part of the EUROPRACTICE program and are very thankful for the technical support provided by EUROPRACTICE.

On-Chip Millimeter-Wave Integrated Absorptive Bandstop Filter in (Bi)-CMOS Technology

University of Technology Sydney, Australia

Contact: Dr. Forest Xi Zhu
E-mail: xi.zhu@uts.edu.au
Technology: IHP 0.13µm SiGe BiCMOS SG13G2
Die size: 0.32mm × 0.12mm

Introduction

Most filters provide rejection by reflecting signals back outside of the passband. This can sometimes cause a problem, especially when the filter is cascaded with relatively high-power devices, such as power amplifiers. A classical way to solve this problem of RF-power-reflection mitigation is to use reflectionless or absorptive RF filters. This type of filter dissipates the non-transmitted RF-signal energy inside its lossy-circuit structure instead of reflecting it back to its input terminal. So far, most of reflection-less/absorptive filters are designed in expensive III/V technologies, such as GaAs p-HEMT.

Description

The design of an on-chip millimetre-wave (mm-wave) absorptive bandstop filter in Bi-CMOS technology is reported here. It consists of a symmetrical two-path transversal structure that is inspired by the absorptive bandstop filter concept. In this design, the lossy properties of silicon-based distributed-element resonators are conveniently exploited to attain the two-port reflectionless behaviour without additional resistors for the stopband RF-power absorption. This is done while achieving a second-order deep-notch bandstop response. For the purpose of proof-of-concept, a 24.5-GHz bandstop filter is designed and fabricated. Close agreement between simulated and measured results for the designed filter is achieved.

The main measured performance metrics of the designed filter are as follows: second-order notched band with center frequency of 24.54 GHz, 10-dB-attenuation-referred absolute bandwidth of 1.54 GHz (i.e., 6% in relative terms), and maximum attenuation equal to 23.1 dB. The minimum input-power-matching level in the proximities of the stopband is 16.3 dB and below 15.4 dB for the frequency range from DC to 60 GHz. The maximum power-attenuation level in the passband region is 0.95 dB as measured at 60 GHz. Moreover, the power-absorption ratio at the notch frequency is 98.6%, as a demonstration of its absorptive nature.

Why EUROPRACTICE?

The University of Technology Sydney has worked with EUROPRACTICE on IHP fabrication for a few years. We have benefitted from EUROPRACTICE's excellent technical support for dummy fill and GDS submission. The EUROPRACTICE's MPW service allows affordable access to state-of-the-art technology, such as the 0.13-µm SiGe Bi-CMOS technology used in this work. Without this service, this design would not have been possible.

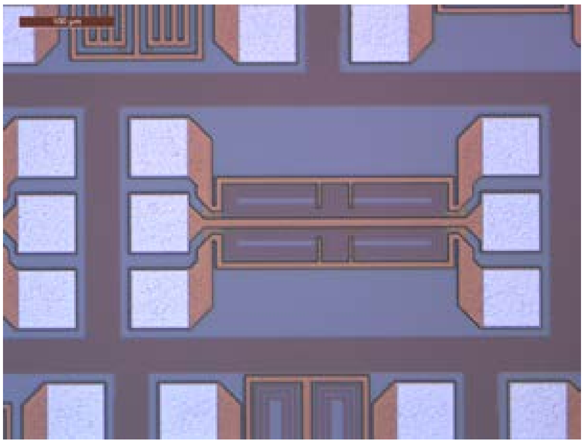


Fig.1: Die microphotograph of the designed filter.

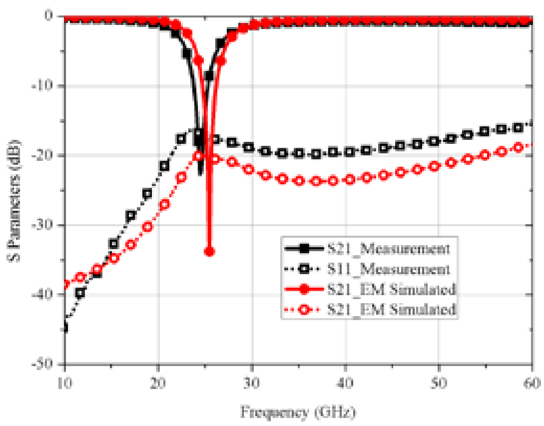


Fig.2: Measured and simulated S-parameters of the designed filter.

Silicon-Based IC-Waveguide Integration for High-Efficiency and Compact Millimeter-Wave Spatial Power Combiner

Integrated Circuits (IC) and Electromagnetics (EM) Group, Eindhoven University of Technology, The Netherlands

Contacts: Piyush Kaul, Alhassan Aljarosha
E-mail: p.kaul@tue.nl

Technology: IHP 0.13µm SiGe BiCMOS SG13S
Die size: 1.18mm × 0.86mm
Design Tools: Cadence: SPECTRE, IC and ASSURA

Description

Modern wireless systems operating at Millimeter-wave (mm-wave) frequencies require a low-loss packaging solution with a compact system-level integration. The research on such systems at mm-wave frequencies is focused on developing efficient power-generating systems based on III-V technology. However, in the past decade, silicon-based technology has rapidly gained significant interest as an alternative solution for the development of such systems. The high-level of integration of several transceiver blocks and size-scaling trend of the technology enable it to be more promising for high-volume commercial applications. In silicon-based wireless systems, the achievable output power is limited at mm-wave frequencies from a single amplifier. However, number of amplifiers that can be combined to achieve high output power is limited due to a trade-off between number of combiner ports and combiner insertion loss.

Packaging using RF interconnects such as flip-chip technology or bond-wires from MMICs to waveguides or high gain antennas introduces more insertion losses in addition to power-combiner loss, which is another challenge at Millimeter-wave frequencies. Moreover, the manufacturing and assembly process of waveguides at these frequencies is difficult in terms of accuracy and tolerances. Therefore, realization of a galvanic contact remains a challenge for transfer of signals between MMICs and waveguides at mm-wave frequencies.

The purpose of this IC-Waveguide system is to present a new packaging solution providing a contactless, and low-loss IC-to-waveguide connection [1]. The proposed solution considers a p-doped lossy substrate silicon-IC-to-waveguide connection for the first time. The silicon-IC comprising an array of coupling pads and microstrip lines is implemented in back-end-of-line (BEoL) of IHP Microelectronics SiGe BiCMOS process, SG13S. The RF-signals are directly coupled from the MMIC coupling-pads to a ridge waveguide via a cavity resonator, which enables a low-loss spatial power combiner in air.

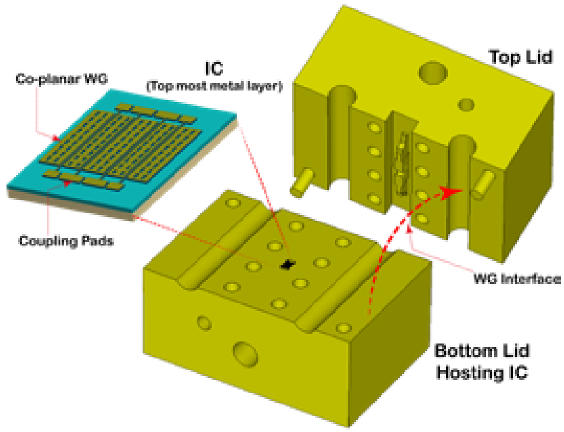


Fig.1: Schematic representation of the building blocks of the device.

Figure 1 presents the 3D model of the IC-Waveguide system.

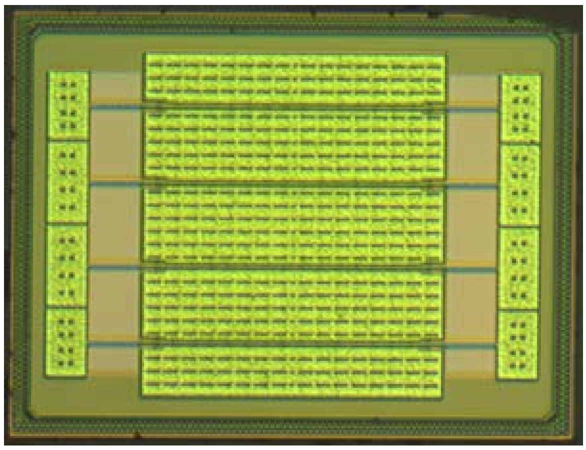


Fig.2: Photograph of the fabricated die.

Figure 2 presents the passive back-to-back IC structure consisting of coupling pads and microstrip lines. The IC structure also uses the TSV module for enhanced RF performance.

Why EUROPRACTICE?

Eindhoven University of Technology has been a frequent user of EUROPRACTICE's project runs. EUROPRACTICE services provide access to several advanced technology nodes. They also provide access to design support, process design kits, knowledge transfers, and design software (Cadence: SPECTRE, IC and ASSURA) in addition to design runs.

References

[1] P. Kaul, A. Aljarosha, A. B. Smolders, P.G.M. Baltus, M. Matters-Kammerer and R. Maaskant, "An E-Band Silicon-IC-to-Waveguide Contactless Transition Incorporating a Low-Loss Spatial Power Combiner," *2018 Asia-Pacific Microwave Conference (APMC)*, Kyoto, 2018, pp. 1528-1530, doi: 10.23919/APMC.2018.8617206.

STMicroelectronics 28FDSOI

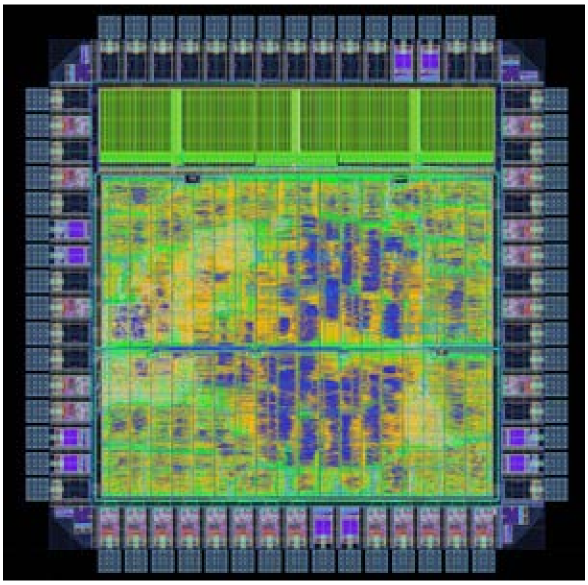


Fig.1: BrainWave layout.

BrainWave: Ultra-Low-Power Processor

Eindhoven University of Technology, Eindhoven, The Netherlands

Contact: Kamlesh Singh
E-mail: k.k.singh@tue.nl

Technology: ST 28nm FD-SOI CMOS
Die size: 1.49 mm^2

Introduction

The BrainWave processor aims for real-time epileptic seizure detection and classification. The chip is an ultra-low-power advanced digital signal processing SoC consisting of a RISC-V core and a coarse-grained reconfigurable accelerator (CGRA).

Description

The SoC implementation is a voltage converter free design based on three-level voltage stack operating using a single voltage source of 1.8V. The current consumption of SRAMs in the top stack is recycled to sustain the near/sub-threshold operation of logic circuits in the two lower stacks. The chip achieves up to 95% power delivery efficiency with a negligible area overhead. The energy efficiency achieved at near/sub-threshold operation (0.4V) is 35MMACs/mW with a peak performance of 4MMAC/s.

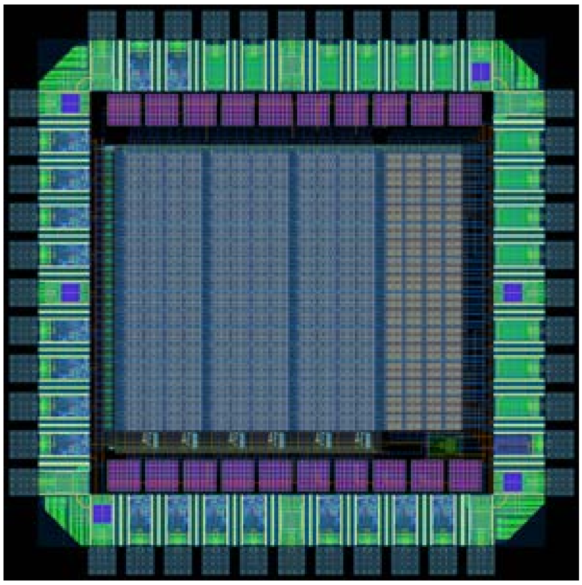


Fig.1: Layout of the circuit.

ROSQUILLAS: Ring Oscillators array to measure RTN

HiPICS research group, Electronic Engineering Dept., Universitat Politècnica de Catalunya-BarcelonaTech (UPC), Barcelona, Spain

Contact: Enrique Barajas
E-mail: enrique.barajas@upc.edu

Technology: ST 28nm FD-SOI CMOS
Die size: 1.16 mm^2

Introduction

This chip has been fabricated to analyze the effect of Random Telegraph Noise (RTN) in circuits fabricated with this technology and used in very low power supply environments.

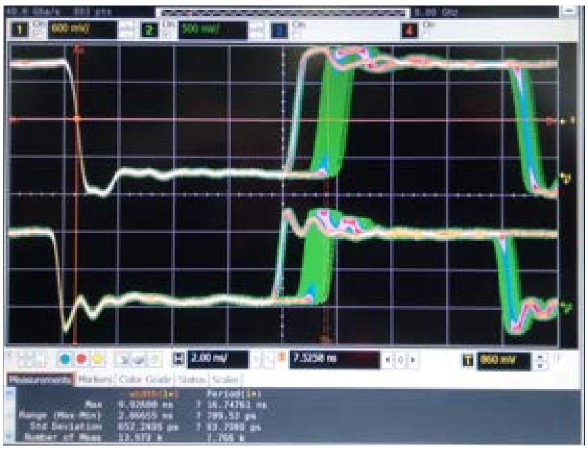


Fig.2: Voltage output as a function of time for one of the oscillators.

Description

In this chip, several thousand ring oscillators have been placed in a matrix-like structure. They are accessible individually. In addition, any two of them can be switched on and connected to the input of an odometer to measure the RTN by measuring the change in the phase between the two oscillations filtering at the same time the jitter. Figure 2 shows the output of one of the oscillators of the array.

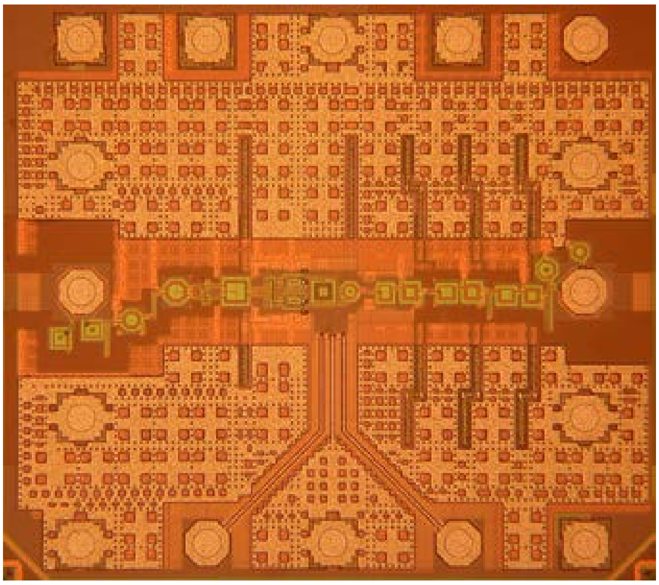


Fig1: Photograph of the fabricated die.

W-Band Active Mirror for OFDM Radar

University of Toronto, Canada

Contact: Sadegh Dadash
E-mail: dadashmo@ece.utoronto.ca
Technology: ST 55nm BiCMOS
Die size: 1.14 mm²

Introduction

The intended application is as an active mirror to improve the resolution of automotive radar networks using FMCW and OFDM modulation.

Description

The MMWTAGIQ tag is a transceiver with single-ended receiver input, a signal detector, an IQ-modulator, and a single-ended transmitter output driving the transmit antenna. The IQ modulation functionality is used to shift the carrier frequency by the modulation frequency. The gain and output power of the transmitter output can be adjusted with an off-chip control by about 30dB. The tag operates from 2.5V supply in the 77-82GHz range. It achieves: Small-signal gain: >40dB; Noise figure: <7dB; Receiver S_{11} <−20dB; Transmitter S_{22} <−15dB; Transmitter P_{sat} = -10dBm; IQ modulation frequency: <200MHz; IQ modulation amplitude: 150mV; Detector range: −60dBm < Pin <−30dBm; Power dissipation: <77mW.

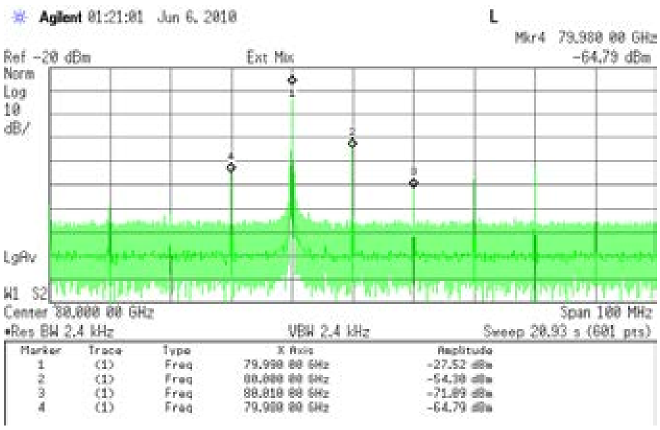


Fig2: Test results of the MMWTAGIQ device.

Multiband 5G New-Radio Digitally Controlled Power Amplifier, Voltage Controlled Oscillator, and Energy Harvester in Single CMOS Chip

Collaborative Microelectronic Design Excellence Centre Universiti Sains Malaysia

Contact: Jagadheswaran Rajendran
E-mail: jaga.rajendran@usm.my
Technology: ST 65nm CMOS RF
Die size: 1.2317 mm^2

Introduction

As wireless communication system keeps on evolving, 5G application is highly demanded as it provides low latency, ultra-high-speed connectivity between devices, and higher data rates. The 5G deployments spectrum has been classified into low-frequency bands (Sub-6 GHz) and high-frequency bands (mm-wave). The sub-6 GHz application is also referred to as 5G New-Radio (5GNR) which is a unified, flexible air interface that supports the three main categories for 5G communications. The categories defined by the International Telecommunication Union (ITU) are enhanced mobile broadband, ultra-reliable low-latency communication, and massive internet of things. 5GNR can also support various 5G vertical applications including automotive and health care industries.

Description

A CMOS power amplifier (PA) comprises a pre-driver, a driver and a main stage that has been designed with integrated Digital Controller which is utilized to vary the operating point of the main PA stage. A voltage-controlled oscillator (VCO) has also been designed and integrated into the main PA. The VCO functions independently and also as a linearizer for the PA. In addition, an Energy Harvester (EH) has been integrated at the output of the PA. The EH converts the RF signal obtained at the output of the PA into a DC power which is utilized to supply other circuits and thus enhances the overall efficiency of the system. The S-Parameter response shows that the designed circuit has a wide operating bandwidth from 4.5-5.7 GHz. A peak gain of 22 dB is achieved at 4.5 GHz. The power amplifier delivers a maximum output power of 18 dBm. At 5 GHz, the VCO delivers an output power of 6.8 dBm and achieves a phase noise of 102 dBc/Hz at 1 MHz. The EH is capable of delivering a maximum DC output voltage of 2.5 V.

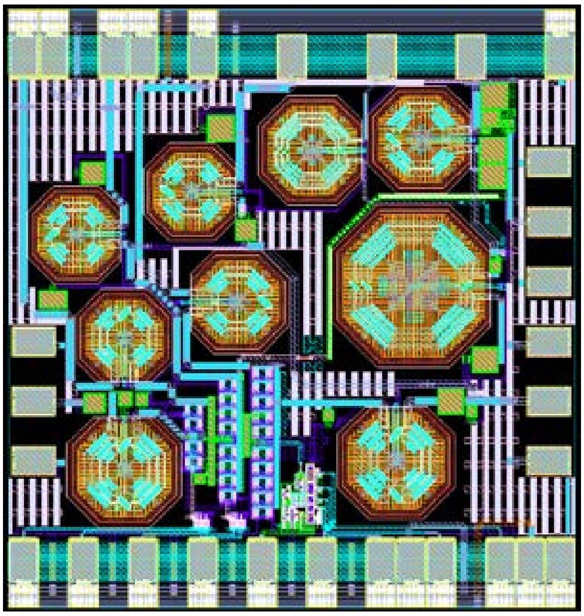


Fig.1: Layout of the circuit.

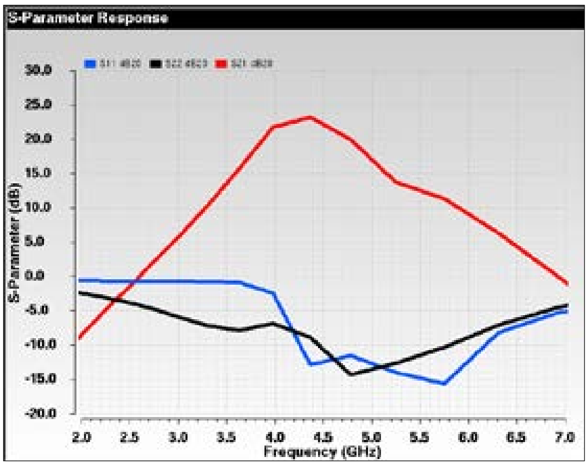


Fig.2: S-Parameter response (dB) as a function of Frequency.

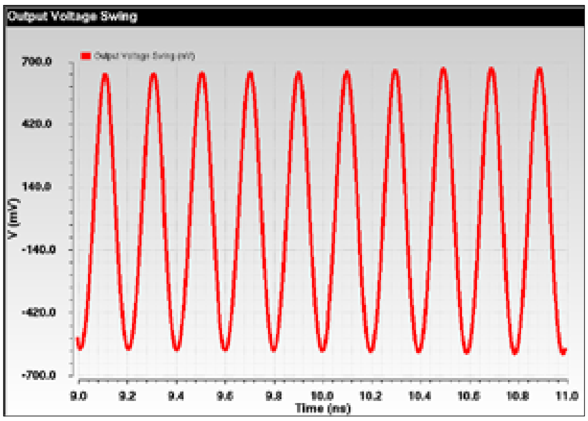


Fig.3: Output voltage swing.

Electronic-Photonic Convergence for Silicon Photonics Transmitters Beyond 100Gbit/s On-Off Keying

University of Southampton, UK

Contacts: Dr Ke Li, Prof. David Thomson, Prof. Graham Reed
E-mail: kl@ecs.soton.ac.uk
Technology: TSMC 28nm HPC & CORNERSTONE Si-Photonics 220nm Active
Die size: TSMC 28nm: 610μm × 1000μm (Microblock)
Design tools: Cadence Virtuoso, Mentor Calibre

Description

The optical modulator is the critical component in systems serving modern information and communication technologies, not only in traditional data communication links but also in microwave photonics or chip-scale computing networks. In contrast to previous work in the field where electronic–photonic integration was mostly limited to the physical coupling approach between photonic and electronic devices, we have introduced a new design philosophy, where photonics and electronics must be considered as a single integrated system, in order to tackle the demanding technical challenges of this field.

By designing the silicon photonics modulator and CMOS driver amplifier as a single integrated system, we have demonstrated the world-wide first all-silicon optical transmitter at 100GBaud/s and beyond, without the use of digital signal processing to recover the signal. Compared to the recently reported lithium niobate modulators and electronic-plasmonic modulators integrated with Silicon Photonics, for example, in Nature (2018), Nature Photonics (2019), and Nature Electronics (2020), this work demonstrates great potential for a low power, low-cost, all-silicon solution, without the need to dramatically complicate fabrication processes by bringing in new materials that are not necessarily CMOS compatible. The technical details of this work can be found from the Optical Society of America (OSA) journal Optica. [1]

The silicon modulator was fabricated through Southampton's CORNERSTONE research fabrication foundry service (available from EUROPRACTICE), and integrated with a TSMC28nm CMOS drivers that are designed in-house, and fabricated at the electronics foundry TSMC, Taiwan. The modulator fabrication and integration work were carried out at the University of Southampton's Mountbatten cleanroom complex.

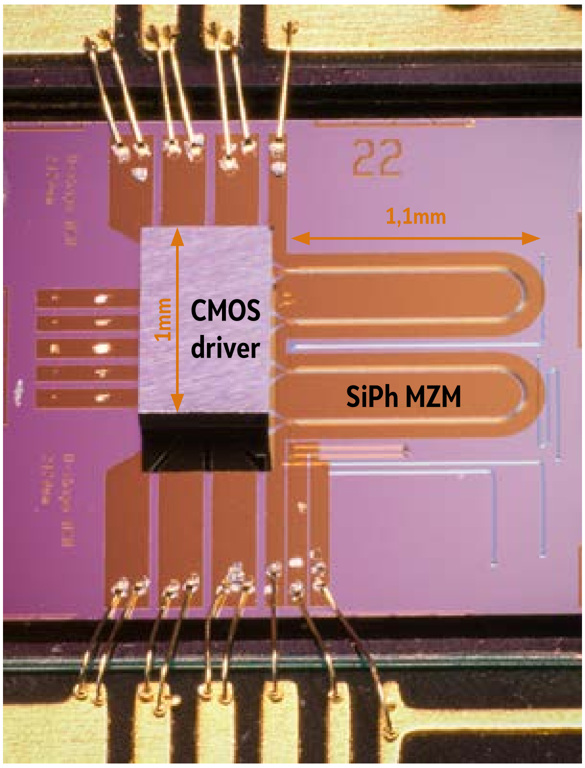


Fig.1: Microscope view of the packaged silicon photonics transmitter.

Why EUROPRACTICE?

The University of Southampton has worked with EUROPRACTICE for TSMC fabrication for many years. We have benefitted from EUROPRACTICE's excellent technical support for CMOS chip submission. EUROPRACTICE has given us affordable access to frequent multi-project wafer fabrication runs.

Acknowledgement

This work was supported through the Engineering and Physical Sciences Research Council (EPSRC) EP/L00044X/1, EP/L021129/1, EP/N013247/1, EP/T019697/1, D. J. Thomson acknowledges funding from the Royal Society for his University Research Fellowship.

Reference

[1] Ke Li, Shenghao Liu, David J. Thomson, Weiwei Zhang, Xingzhao Yan, Fanfan Meng, Callum G. Littlejohns, Han Du, Mehdi Banakar, Martin Ebert, Wei Cao, Dehn Tran, Bigeng Chen, Abdul Shakoor, Periklis Petropoulos, and Graham T. Reed, "Electronic–photonic convergence for silicon photonics transmitters beyond 100 Gbps on–off keying," Optica 7, 1514-1516 (2020) https://doi.org/10.1364/OPTICA.411122

Error-detection and Correction Through Completion Detection Applied in a Dual Core DSP Processor Operated at Near-threshold Supply Voltage

KU Leuven – ESAT – MICAS, Belgium

Contacts: Roel Uytterhoeven, Wim Dehaene
E-mail: roel.uytterhoeven@esat.kuleuven.be
Technology: TSMC 28nm HPC+
Die size: 1.5mm × 1.5mm
Design tools: Cadence Xcelium, Innovus, Virtuoso, Spectre; Mentor Calibre

Description

Today, the wide application spectrum of battery-powered electronic devices demands energy-efficient microprocessors across a wide performance range. To that end, we focus on the implementation of these devices at ultra-low supply voltage in the sub/near-threshold domain. In this domain, the energy benefits associated with voltage-scaling reach their optimum in the minimum energy point or MEP.

However, low voltage operation increases the system's sensitivity to PVT variations and therefore enforces large and inefficient safety margins to ensure reliability as illustrated in Fig. 1. To counteract the energy losses caused by these margins, a novel timing-error detection and correction (EDaC) technique is applied. In contrast to most conventional EDaC systems, this technique avoids the need for additional hold-constraints to detect timing-errors. Furthermore, the proposed system corrects timing-errors through last-minute error-prevention. This allows the host processor to remain unaware (i.e. make abstraction) of the EDaC system and thus significantly eases the integration between both.

In this Silicon prototype shown in Fig. 2, our EDaC system is applied to the CoolFlux DSP audio processor from NXP. This is a dual-core processor optimized for low power consumption. To explore and benchmark the gains from the EDaC system, only one of the two identical cores is equipped with EDaC. The core without EDaC acts as a baseline that has to operate with the conventional signoff margins to guarantee reliability. On the other hand, the core with EDaC can safely operate at its most critical point without any margins.

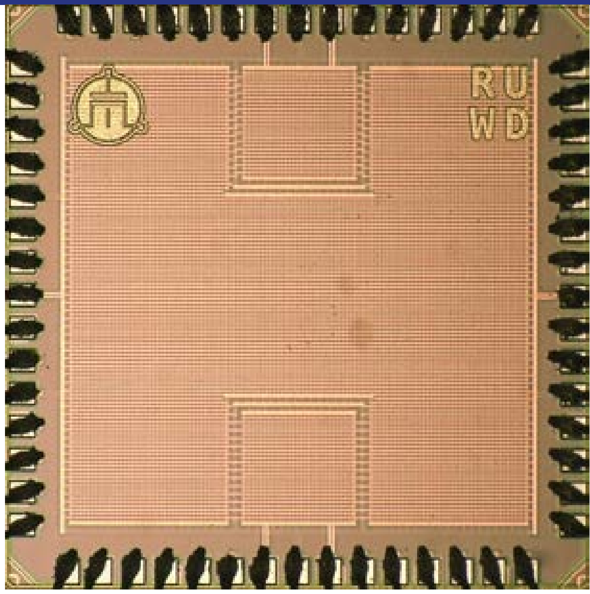


Fig.2: Die photograph of the Silicon prototype in 28nm HPC+ from TSMC.

Why EUROPRACTICE?

At MICAS, EUROPRACTICE is the default gateway to silicon prototypes. Their well-packed technology and CAD tools portfolio provides us with all the ingredients we need to design innovation and cutting-edge electronics. This whilst their well populated run schedule allows for flexible tape-out planning.

Acknowledgements

This design is made possible thanks to a collaboration with NXP semiconductors Haasrode and the support of an FWO-SB scholarship (1S31817N)

Reference

[1] R. Uytterhoeven and W. Dehaene, "Completion Detection-Based Timing Error Detection and Correction in a Near-Threshold RISC-V Microprocessor in FDSOI 28 nm," in IEEE Solid-State Circuits Letters, vol. 3, pp. 230-233, 2020.

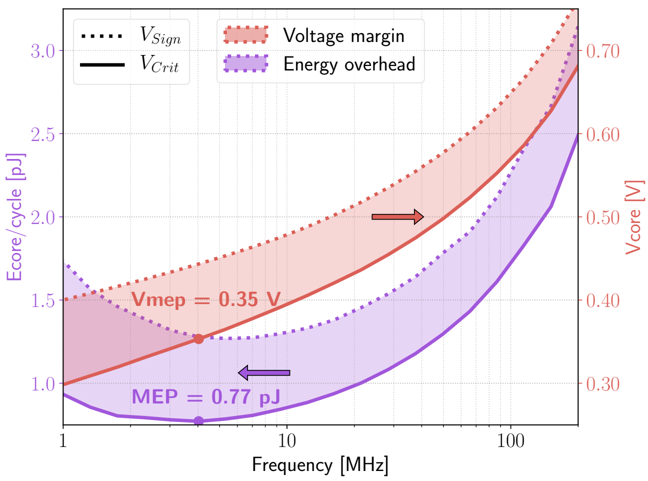


Fig.1: Illustration of the energy overhead caused by voltage margins based on measurements from [1].

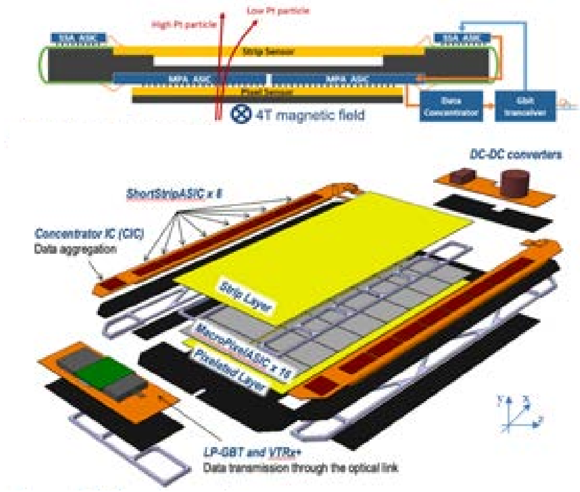


Fig. 1: Hybrid Tracking Module Architecture

A novel particle tracking detection module featuring real-time, on-chip, prompt momentum discrimination for the CMS LHC experiment

CERN - The European Laboratory for Particle Physics, Geneva, Switzerland

Contacts: Kostas Kloukinas, Davide Ceresa, Alessandro Caratelli
E-mail: kostas.kloukinas@cern.ch
Technology: TSMC 65nm CMOS
Die sizes: 25mm × 11.9mm (MPA), 6.5mm × 11.8mm (SSA)
Design tools: Cadence Virtuoso, Genus, Innovus

Introduction

The Large Hadron Collider (LHC) experiments ATLAS, CMS, ALICE and LHCb at CERN are currently some of the most prominent detectors because of their size, complexity and rate capability. Huge magnet systems, which are used to bend the charged particles in order to measure their momenta, dominate the mechanical structures of these experiments. The fact that only about 100 of the 10^9 events per second can be written to disk necessitates highly complex online event selection, called 'triggering'.

CERN has planned upgrades of the LHC accelerator that are expected to allow operation at luminosities around or above $5{\times}10^{34}cm^{-2}s^{-1}$ after 2025, to eventually reach an integrated luminosity of 3000 fb^{-1}. In order to fully exploit such operating conditions and the delivered luminosity, the CMS experiment needs to upgrade its tracking detectors and substantially improve its trigger capabilities. The capability of performing quick recognition of particles with high transverse momentum (more than 2 GeV/c) in the tracker is deemed essential to keep the CMS trigger rate at an acceptable level.

Description

This work presents a novel tracking module based on a combination of a pixelated sensor with a short strip sensor that would offer, for the first time, real-time, on-detector, prompt momentum discrimination. This module is part of the CMS Outer Tracker upgrade for the High Luminosity LHC (HL-LHC)[1]. As shown in Figure 1, a module is composed by two closely spaced silicon sensors (a pixelated layer and a strip layer sensor) in a strong magnetic field providing sufficient sensitivity to measure the particles' transverse momentum over the small sensor separation of a few millimeters. The correlation of the coordinates measured by the two sensors in the x–y plane enables the pT discrimination, while the segmentation of the pixelated sensor along the z direction (R direction in end-cap configuration), provides a precision coordinate that contributes to the required z_0 resolution for the reconstructed track.

The Macro-Pixel ASIC (MPA) is a 65nm CMOS technology pixel readout chip featuring on-chip real-time particle discrimination with trigger-less and zero suppressed readout. The Short Strip ASIC (SSA) is a strip readout chip, designed in the same technology, which provides real-time particle hit coordinates from a strip sensor to the MPA for the particle discrimination.

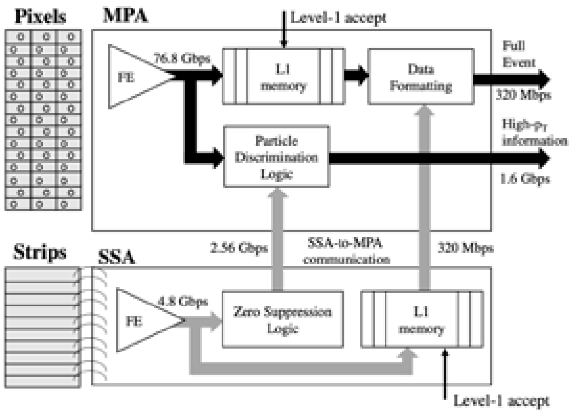


Fig. 2: Block Diagram of the MPA Macro Pixel ASIC and SSA Short-Strip ASIC readout architecture.

Fig. 2. depicts the block diagram of the MPA and SSA readout architecture. The trigger-less readout is based on transverse momentum (p_T) particle discrimination and it works in parallel with a triggered and zero suppressed readout with a programmable latency (up to 12.8μs at 40MHz event rate), which provides the entire event with a maximum trigger rate of 1 MHz[2]. The high complexity of the digital logic for particle selection and the very low power requirement of < 100 mW/cm^2 drive the choice of a 65 nm CMOS technology. The harsh environment, characterized by a high ionizing radiation dose of 100 Mrad and a low temperature of around -30° C, requires additional stud-

ies and technology characterization. Several architectures for particle tracking have been studied and evaluated with physics events from Monte Carlo simulations. The chosen architecture reaches an efficiency of > 95% in particle selection and a data reduction from ~30 $Gbps/cm^2$ to ~0.7 $Gbps/cm^2$.

Results

Due to the large die sizes, the MPA and SSA ASICs have been prototyped on a full mask set dedicated engineering run on the TSMC 65nm MS/RF process. Testing of the MPA and SSA ASICs consisted of functional verification of the digital circuitry and performance characterization of the analog front-end circuitry using embedded charge injection capacitor circuits. ASICs with connected sensors were tested using radioactive sources and interest beam experiments. As extensively reported in [3], the MPA front-end characterization with internal capacitance pulse injection matched simulations closely, with a pixel-to-pixel threshold spread of 171 e−r.m.s. after equalization, an Equivalent Noise Charge (ENC) of 188 e−r.m.s., a peaking time of 24ns and a time walk of < 15 ns. The power consumption is lower than 200 mW per chip and fulfills the very strict CMS Tracker requirements. The same tests, as reported in Ref. [4], were carried out on the SSA obtaining a strip-to-strip threshold spread of 55 e−r.m.s. after equalization, a noise without sensor connected of 330 e−r.m.s. and a peaking time of 19.3 ns. A special board was developed to test the MPA-SSA high-speed communication links. Measurements show a robust communication with a Bit Error Rate (BER) lower than 1×10−9 with the lower I/O bias current setting (BER limited by the test system, new measurement campaign on-going). During this test, a total consumption of 250 mW for the two ASICs has been measured.

The ASICs' irradiation with X-rays up to 200 Mrad did not show

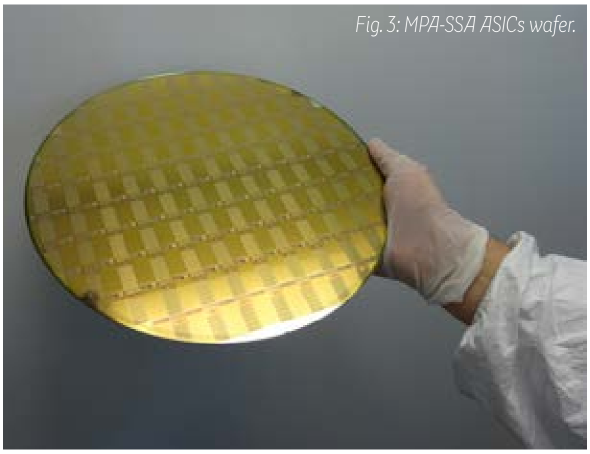


Fig. 3: MPA-SSA ASICs wafer.

any performance degradation. In addition, a Single Event Upset (SEU) test with Heavy Ions proved SEU tolerance up to an effective Linear Energy Transfer (LET) of ~70 MeV / (mg/cm^3). Finally, a data error rate evaluation provided an SEU related data error probability lower than 5×10−11.

Why EUROPRACTICE?

Within the framework of ASIC design for Particle Physics Instrumentation CERN and its collaborating institutes and universities tape out through the EUROPRACTICE service more than 50 ASICs per year. EUROPRACTICE services gives access to modern semiconductor processes of the worlds largest dedicated independent foundry, TSMC. Projects, such as the CMS Outer Tracker ASICs, with relatively small volume production requirements would not have otherwise the possibility to access and benefit from the use of such advanced process. Of equal importance is the technical support that the project receives from EUROPRACTICE engineers throughout the design the tape-out phases.

The development of such complex ASICs requires the use of state-of-the-art EDA software tools for the design, the implementation and verification both at the component level as well as at the system level. EUROPRACTICE software service is an indispensable element for the ASIC developments at CERN and its collaborating institutes, supporting the use of a multitude of state-of-the-art EDA tools facilitating coherency in the collaborating design framework of distributed design teams.

Custom microelectronics components implemented in advanced technologies are vital parts of today's complex scientific instruments. The services provided by EUROPRACTICE are allowing a large community of physicists and engineers at CERN and in tens of collaborating Institutes working for these projects to use state of the art EDA software tools and access advanced CMOS process for the construction of unique scientific instruments with a centralized high-quality technical support.

References

[1] CMS Collaboration, The Phase-2 Upgrade of the CMS Tracker, CERN-LHCC-2017-009; CMS-TDR-014.

[2] D. Ceresa, MPA-SSA, design and test of a 65nm ASIC-based system for particle tracking at HL-LHC featuring on-chip particle discrimination. https://ieeexplore.ieee.org/abstract/document/905 9989

[3] D. Ceresa, Characterization of the MPA, PoS(TWEPP2018)166. https://pos.sissa.it/343/166/

[4] A. Caratelli, Characterization of the SSA, PoS(TWEPP2018)159. https://pos.sissa.it/343/159

Mixed-Signal Neuromorphic Device HICANN-X

Electronic Vision(s) Group, Kirchhoff Institute for Physics, Heidelberg University, Germany

Contact: Dr. Johannes Schemmel
E-mail: schemmel@kip.uni-heidelberg.de
Technology: TSMC 65nm
Die size: 8mm × 4mm
Design tools: Cadence Virtuoso, Mentor ModelSim/Questa, Cadence Xcelium, Synopsys Design Compiler, Cadence Innovus, Synopsys Primetime, Mentor Calibre

Description

Heidelberg University has a more than 20-year history of neuromorphic circuit design. The most recent generation is the BrainScaleS-2 system. This tapeout comprised the current revision of the BrainScaleS-2 system ASIC: a complex mixed-signal system-on-a-chip supporting all aspects of neuromorphic processing. It contains at its heart an analog neural network core, consisting of 256k synapse circuits and 512 neuronal compartments. They operate 1000 times faster than biological real-time, resulting in a maximum connection rate of $32*10^{15}$ cps. The analog core simultaneously supports spike or rate based neural modeling, making it suitable for deep convolutional neural networks as well as event-based processing after the biological example. The synapses include temporal correlation sensors for online learning, which is further supported by two on-die embedded Power-PC CPU cores with 128-wide SIMD-processing extensions each. They can access the analog correlation measurements as well as the membrane voltages of all neuronal compartments with two parallel ADC converters providing a total number of 1024 channels.

External communication is realized by eight source-synchronous serial links with an aggregated bandwidth of 32 Gb/s.

The applications of the HICANN-X system are twofold: low-power analog inference and modeling of biologically-inspired online learning algorithms. For inference two operation modes are available. Either a rate-based one, which allows the direct implementation of DCNN models, or spike-based coding, which is especially suited for extreme low-latency inference. MNIST classification has been demonstrated with an effective rate of 70k frames per second at 4 µJ per frame while powering the full ASIC.

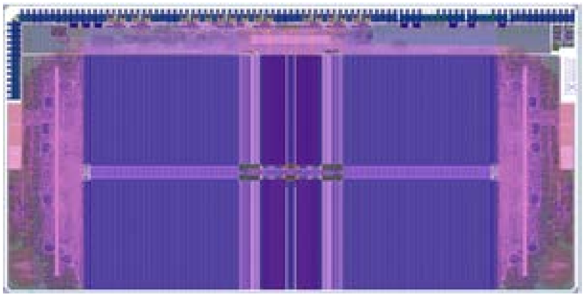


Fig.1: Layout view of HICANN-X.

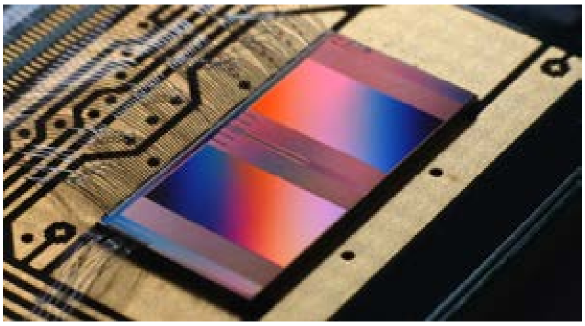


Fig.2: Photograph of the fabricated chip.

As a modeling platform for biology, the BrainScaleS-2 architecture supports the Adaptive-Exponential-Integrate-and-Fire neuron model with additional support for active dendrites and structured neurons. Support circuits for synaptic as well as structural plasticity are closely coupled to the on-die SIMD cores, providing “hybrid plasticity”: plasticity algorithms with most of the flexibility of software solutions while still maintaining the speed and power-efficiency of a fully parallel mixed-signal hardware implementation.

Why EUROPRACTICE?

Heidelberg University has worked with EUROPRACTICE on TSMC and other ICM fabrication on a multitude of successful tapeouts since 1994. EUROPRACTICE has been a reliable partner for all aspects of multi-project and full maskset prototypes. The affordable access to multi-project wafer and mini@sic fabrication has been an enabling factor for our research in neuromorphic hardware.

Acknowledgement

The research has received funding from the Bundesministeriums für Bildung und Forschung under the funding no. 16ES1127 (HD-BIO-AI) and from the European Union’s Horizon 2020 Framework Programme for Research and Innovation under the Specific Grant Agreement Nos. 720270, 785907 and 945539 (Human Brain Project, HBP).

LEO-I rapid integration research platform

Emerging Nanoscaled Integrated Circuits & Systems (EnICS) Labs, Faculty of Engineering, Bar-Ilan University, Israel

Contacts: Adam Teman, Shawn Ruby, Roman Golman
E-mail: adam.teman@biu.ac.il

Technology: TSMC 65nm CMOS LP
Die size: 4000µm × 2000µm

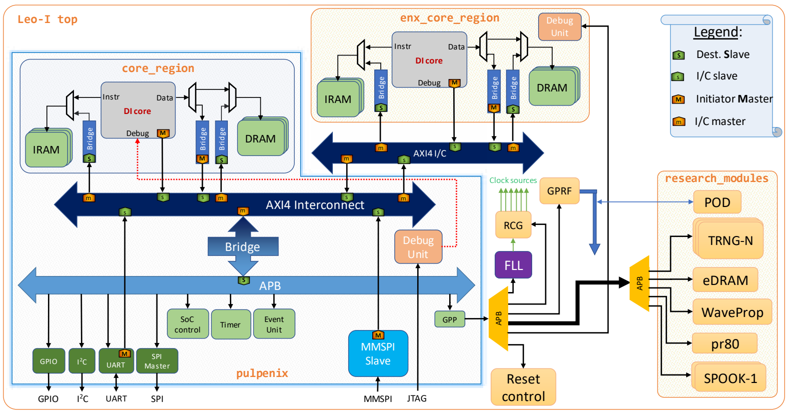


Fig. 1: Leo-I architecture.

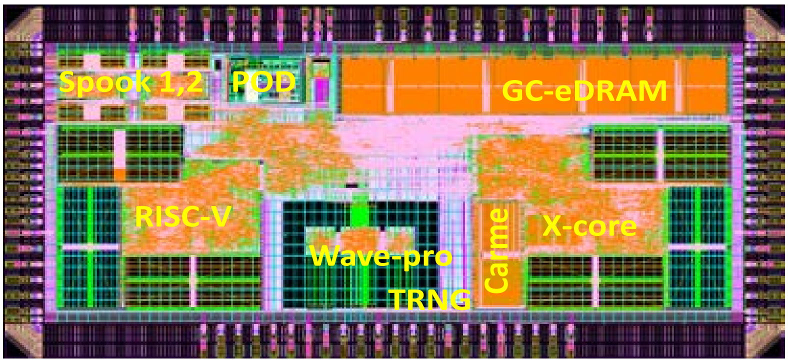


Fig. 2: LEO-I Layout.

Background – The EnICS Labs Research Center

The Emerging Nanoscaled Integrated Circuits & Systems (EnICS) Labs in the Faculty of Engineering at Bar-Ilan University combines an academic research center with an industrial team of engineers ("SoC lab"), allowing to implement very complex projects, which are used for a demonstration of the ability of the research groups and the Israeli industry alike. This tapeout is a research-driven design, that was implemented using both the capabilities of the researchers and the industrial experience of the SoC lab.

Description

This chip nicknamed "LEO-I" is the first tapeout of an experimental platform design allowing to integrate several diverse research modules coming from different research groups into one chip with a standard interface. In this project researchers and research students have been working with the SoC Lab engineers, to develop the proposed platform.

The platform is aimed to allow very fast design cycles for bringing a project from the idea to the tapeout stage, where the researcher only needs to integrate his module via a dedicated advanced peripheral bus (APB) interface, while the rest of the chip is already implemented. The platform also includes two general purpose cores, built on the open-source and extendable RISC-V architecture. The cores are the first tapeout of our small footprint "HAMSA-DI" core – a dual-issue version of the RI5CY core, developed by the PULP team at ETH-Zurich. One of the integrated cores is a standard core made for reference comparison and backup, while the other is called the "experimental core", as it allows integration of research modules directly into the microprocessor datapath and enabling microarchitecture level innovations. The chip architecture is illustrated in Fig. 1, showing both the hardened area that is the heart of the platform, which allows fast tapeout cycles, and the research modules integrated into the chip. The first tapeout of the chip, that includes more than ten different research modules integrated both as standalone modules and inside the research core, both from our research group, and from other groups. The layout of the chip is shown in Fig. 2.

Why EUROPRACTICE?

EUROPRACTICE allows us to prototype research designs in state-of-the-art technologies at affordable prices. The frequent scheduling of tapeout shuttles is extremely convenient allowing us to build an appropriate timeline for the project. Furthermore, the design submission process is very friendly, and accompanied by very good communication with EUROPRACTICE staff that is always open to questions and ready to help.

Acknowledgements

We acknowledge the support of Prof. Luca Benini's group at ETH-Zurich for sharing their FLL IP with us, as well as providing the RI5CY core and PULPino SoC platform, from which our cores and platform were forked. We acknowledge the Israel Innovation Authority under the Kamin program and the Israel Ministry of Science and Technology for providing the funding for the tapeout, as well as a large portion of the research modules. Additional research modules are also supported by the Israel Science Foundation.

Rosetta: PULP-based in-memory computing research vehicle

ETH Zürich, EPFL, Switzerland

Contacts: Manuel Eggimann, Alexandre Levisse, Robert Giterman
E-mail: meggimann@iis.ee.ethz.ch
Technology: TSMC 65nm CMOS
Die size: 2940µm × 4080µm
Design tools: Synopsys: Design Compiler; Cadence Design Systems: Innovus; Mentor: Questasim, Calibre

Fig.1: Rosetta dies in a waffle pack.

Description

Rosetta is a research SoC designed around the PULPissimo architecture part of the open-source PULP platform (https://pulp-platform.org/). The basis is a RISC-V based microcontroller system running at 200MHz including 512kBytes of on-chip SRAM and a wide set of common peripherals such as QSPI, I2C, I2S, Camera Interface, UART and a JTAG-based RISC-V debug specification compliant debug unit with full access to the main memory bus of the system.

The most interesting aspect of the PULPissimo system is that it allows the addition of hardware accelerators that have direct access to the processor memory with relative ease. In Rosetta, the independent work of three different research groups was combined in one SoC. By sharing a common processing infrastructure and memory, the research groups were able to focus their work on their research and develop their own accelerators. The flexibility of the PULPissimo allowed these independent systems to be manufactured within the same SoC without interfering with each other while allowing greater flexibility for testing and evaluation.

The contribution of the Integrated Circuits Laboratory of ETH Zurich is a programmable autonomous accelerator for Hyper-Dimensional Computing Algorithms with binary-spatter-code based hypervectors of dimensionality of up to 2048 bits.

The Embedded Systems Laboratory of EPFL, Lausanne has contributed a 32KiB in-sram computing architecture and an innovative memory controller enabling in-situ bitwise operations, addition and multiplications. These features will be used to accelerate data-intensive applications running on the PULPissimo platform.

Finally, the Telecommunication Circuits Laboratory of EPFL developed a 64 KiB (in 16 memory cuts) of Gain-Cell eDRAM, based on conventional logic design rules, which can offer higher density than SRAM. The eDRAM in this implementation has a built-in refresh support and a new option to ease folding of the memory. By adjusting the refresh period, it will be used to explore approximate-computing concepts.

While these systems are designed to operate independently, the PULPissimo system also allows these systems to work concurrently, for example the hyper-dimensional computing accelerator is able to use both its own standard cell based memories operating at low voltages or the eDRAM operating with long refresh periods to explore energy reliability trade-offs in such configurations.

The chip is named after the Rosetta Stone that contains the same script in three alphabets and was instrumental in deciphering hieroglyphs. This chip contains the work of three different research groups and the high dimensional computing accelerator has applications in language recognition.

Why EUROPRACTICE?

Over the years, the Integrated Systems Laboratory of ETH Zurich has been able to design and get more than 200 ASICs manufactured through the active and invaluable support of both the EUROPRACTICE Design Tool Service which allows us to have access to state of the art IC Design software not only for research but also for in-class use and of course the EUROPRACTICE IC manufacturing service that has been instrumental in our ability to be engaged in IC Design at this level.

EUROPRACTICE is not only a service for us, but a partner that helps us with the correct choice of technology, packaging as well as supporting us in all aspects of the design process.

Acknowledgements

Part of the work was supported by the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215, Mnemosene.

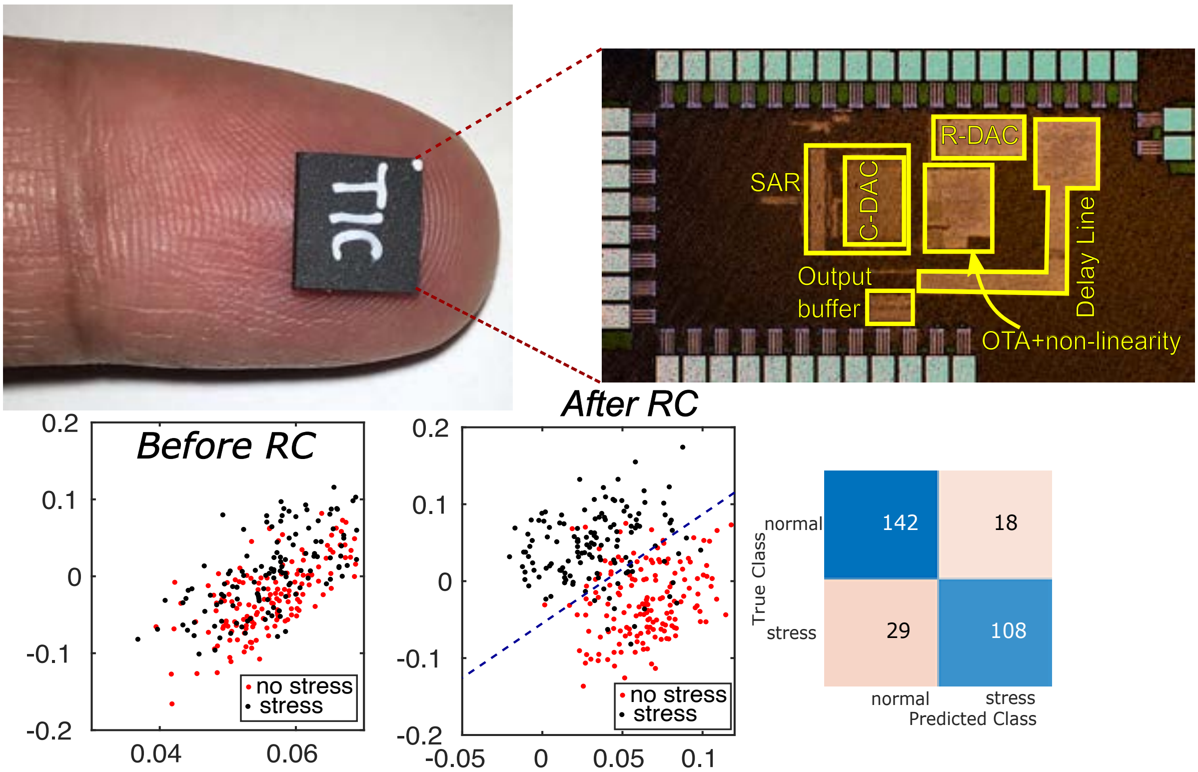


Fig.1: RCNN chip for stress detection from ECG.

CMOS reservoir computer for intelligent wearable health monitors

Electrical Engineering, University at Buffalo, State University of New York, NY, USA

Contacts: Arindam Sanyal, Sanjeev Tannirkulam Chandrasekaran
E-mail: arindams@buffalo.edu
Technology: TSMC 65nm 1p9M
Die size: 1.2mm × 0.7mm

Description

Early detection of stress and heart diseases can prevent one-third of global deaths. Advances in machine learning (ML) has the potential for automating risk prediction of heart diseases by analyzing patient vitals in combination with electronic healthcare record (EHR). Embedding ML algorithms on wearable devices can lead to continuous intelligent health monitoring of patients. However, conventional ML algorithms are computationally intensive and consume significant energy during a memory access, which makes their integration on resource-constrained wearables challenging. Prior attempts have addressed this issue through reduced bit-precision, in-memory computation, and reduced number of multipliers. However, they consume energy in the range of hundreds of nJ to tens of µJ for each inference.

Instead of optimizing existing ML architectures, we demonstrate the first reservoir-computing based RCML architecture that consumes factors-of-magnitude lower energy than conventional ML algorithms without sacrificing accuracy. The RC mimics a non-linear kernel and projects the input to a higher-dimensional space, thereby enabling classification of the data with simple logistic regression (LR) output layer. We demonstrate the RC chip for detecting stress and heart diseases from electrocardiogram (ECG) signal and electronic healthcare record (EHR). Operating from a 1.2V supply, the RC can detect stress from ECG signals in real-time with 93% accuracy, while consuming 27.5nJ/inference, which is 7x better than existing state-of-the-art ECG processors. The RC is capable of early prediction of heart diseases with 84% accuracy while consuming 7.5nJ/inference, which is 44x better than existing state-of-the-art neural networks ICs employed for medical event classification.

Why EUROPRACTICE?

EUROPRACTICE offers affordable prototyping for research and it is much simpler to use their PDK and services compared to competitors in the USA. The EUROPRACTICE and imec staff are also easily accessible and have always answered all our questions patiently and helped us with all our prototypes.

Acknowledgement

This material is based on research sponsored by US Air Force Research Laboratory under agreement number FA8650-18-2-5402.

ALTIROC1, a 25 ps jitter ASIC for the ATLAS High Granularity Timing Detector (HGTD)

OMEGA (CNRS/IN2P3), Ecole Polytechnique, Palaiseau, France
SLAC National Accelerator Laboratory, Stanford University, Menlo Park, California

Contacts: Nathalie Seguin-Moreau, Bojan Markovic
E-mails: nsmoreau@in2p3.fr, markovic@slac.stanford.edu
Technology: TSMC 0.13µm CMOS MS/RF (8-inch)
Die size: 7600µm × 7700µm

Description

ALTIROC1 is a 25-channel ASIC prototype designed in TSMC 130 nm to read out a 5 × 5 channel matrix of 1.3mm × 1.3mm Low Gain Avalanche Diodes (LGAD) of the new ATLAS HGTD detector foreseen for the High Luminosity-LHC upgrade, where high radiation levels are expected (200 Mrad and 2.5 10^{15} MeV neq/cm^2 fluence). The dies will be bump-bonded onto sensors. The targeted combined time resolution of the system {sensor + readout electronics} is 25 ps for 10 fC input charges.
The ASIC noise must be small enough to detect charges as small as 4 fC with a 95 % efficiency.
This ASIC comprises several analog and digital blocks. Each channel integrates a RF preamplifier (1 GHz bandwidth) followed by a large gain leading edge discriminator and two Time to Digital Converters (TDC) for Time-of-Arrival (TOA) and Time-Over-Threshold (TOT) measurements. The timing data are stored in a local memory. The TOA and TOT TDCs achieve a 20 ps time resolution over a 2.5 ns range and 40 ps over a 20 ns range respectively. Measurements gave a DNL of about 6 ps rms and time resolution dispersion between channels of 0.35 rms after individual tunings. This frontend exhibits a 20 ps jitter noise for a detector capacitance of 5 pF and an input charge of 5 fC while keeping a challenging power consumption of less than 4.5 mW per channel. Furthermore, the ASIC has out-of-pixel analog and digital blocks. In particular, it includes a 1.28 GHz PLL providing multiples of 40 MHz clocks and a phase shifter with 100 ps phase shift resolution over a 25 ns range.

Why EUROPRACTICE?

The EUROPRACTICE service offers the ability to reduce manufacturing costs thanks to large multi-project wafers.

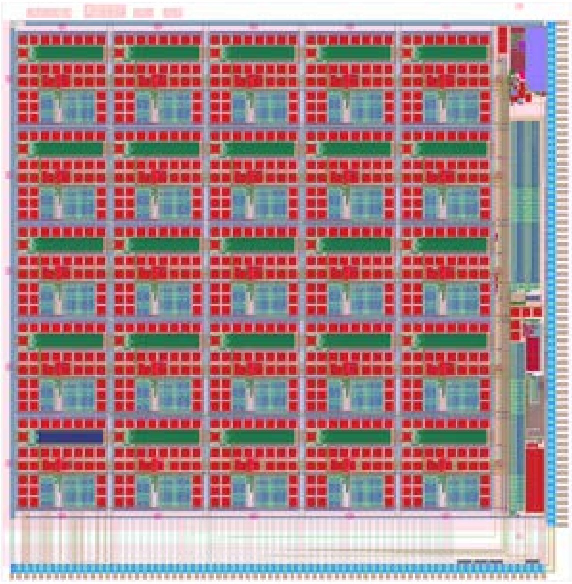


Fig.1: ASIC layout

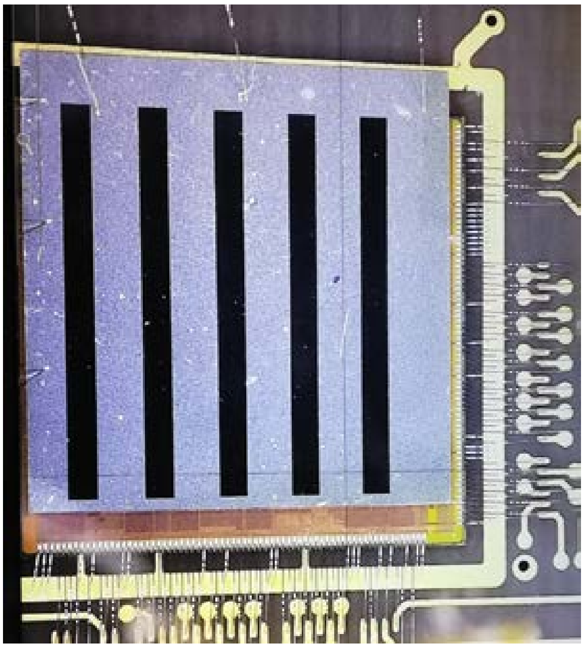
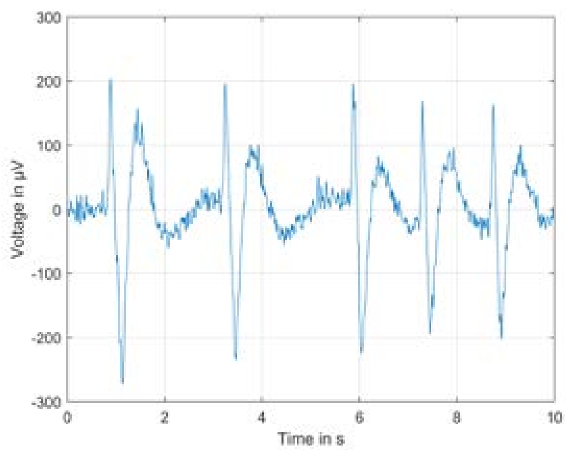


Fig.2: ASIC bump bonded onto a sensor



GAMMA2 *Fig.3: Measured EEG-signal, showing blinking eyes.*

Fig.1: GAMMA2 prototype

GAMMA2: Bio-sensing SoC for wireless battery-less EEG-electrodes

Institute for Integrated Circuits, Johannes Kepler University Linz, Austria

Contacts: Prof. Harald Pretl, Stefan Schmickl
E-mail: harald.pretl@jku.at
Technology: TSMC 0.18µm CMOS Log/MS/RF (G)
Die size: 1.6mm × 1.6mm
Design tools: Cadence Virtuoso, Cadence Innovus, Mentor QuestaSim, Synopsys Design Vision, Synopsys PrimeTime

Description

Trends show that electroencephalography (EEG) systems, used for either patient therapies or brain-computer-interfaces (BCI), tend to use more and more electrodes due to increased spatial resolution. With growing electrode count, the cabling process becomes a very time-consuming task on the one hand, and on the other hand it becomes practically impossible for the user to move because of the bulky cabling. Here the presented bio-sensing SoC GAMMA2 comes into play as replacement of a cabled solution. Fig.1 shows a picture of GAMMA 2 prototype. The wireless BCI system was demonstrated at ARS Electronica 2020: Pangolin Scales.

The SoC consists of a power-management unit, which consists of an RF-energy-harvester working in the 868 MHz UHF-band for wireless powering of the SoC [1, 2], and a low-power LDO providing a constant voltage of 1 V to the subsequent units, providing a power budget of 5 µW for the total SoC. For the acquisition of the bio-signals, which are in the order of 10 µV and 0.5 Hz to 100 Hz, a 350-nW ac-coupled low-noise amplifier with reduced flicker-noise [3] and an untrimmed 14-bit non-binary SAR-ADC with 0.37 fF-capacitors using 1.1 µW at 4 kS/s [4] are responsible. The digitized samples of the bio-signal get wirelessly transmitted with an ultra-wide-band (UWB) impulse-radio (IR) transmitter (TX) [1, 2]. The UWB-IR-TX works at 7 GHz, sending with a data rate of 5.12 kbps using a double-pulse-interval coded alphabet, consuming only 1.89 µW. The used transmission scheme allows up to 64 sensor nodes to work at the same time, enabling a high amount of wireless sensing channels. Indoor wireless transmission experiments showed a range of over 12 m, in companion with a custom made UWB-receiver.

Why EUROPRACTICE?

The EUROPRACTICE services allow affordable access and reasonable prices to leading-edge IC technologies, frequent MPW-fabrication runs, attractive mini@sic runs, CAD tools and packaging services. Our research projects would simply not be possible without the services EUROPRACTICE provides.

References

[1] S. Schmickl, T. Faseth, and H. Pretl, “A 1.9-µW 7-GHz IR-UWB transmitter with RF-energy-harvester in 180-nm CMOS for battery-less bio-sensors,” in 2019 17th IEEE International New Circuits and Systems Conference (NEWCAS), June 2019, pp. 1–4.

[2] S. Schmickl, T. Faseth, H. Pretl, “An RF-Energy Harvester and IR-UWB Transmitter for Ultra-Low-Power Battery-Less Biosensors,” in IEEE Transactions on Circuits and Systems I: Regular Papers 67(5), 2020, 1459–1468.

[3] S. Schmickl, T. Faseth, H. Pretl, “An Untrimmed 14-bit Non-Binary SAR-ADC Using 0.37 fF-Capacitors in 180 nm for 1.1 µWat 4 kS/s,” in: 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2020, to be published.

[4] S. Schmickl, T. Schumacher, P. Fath, T. Faseth, H. Pretl, “A 350-nW Low-Noise Amplifier With Reduced Flicker-Noise for Bio-Signal Acquisition,” in: 2020 Austrochip Workshop on Microelectronics (Austrochip), pp. 9-12, 2020.

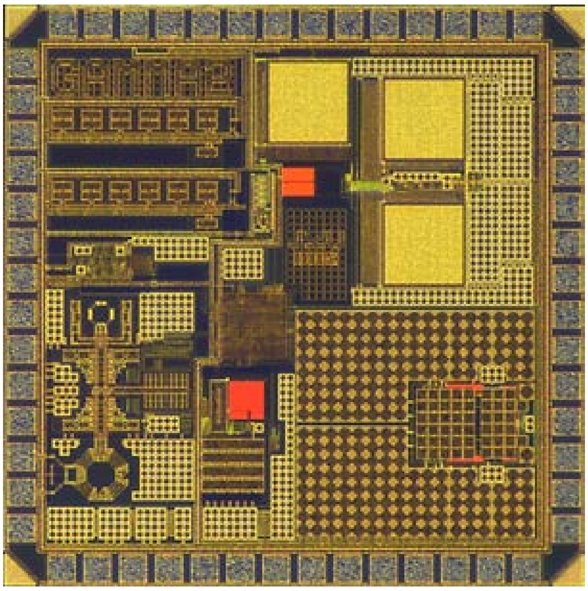


Fig.2: Micrograph of GAMMA2 SoC.

Circuit for fast and wide-band BioImpedance Spectroscopy

National Center of Scientific Research - Laboratory of Computer Science, Robotics and Microelectronics of Montpellier (CNRS-LIRMM), France

Contact: Serge Bernard
E-mail: serge.bernard@lirmm.fr

Technology: TSMC 0.18µm CMOS MS/RF
Die size: 4160µm × 3695.01µm

Description

In the context of marine animal monitoring, teams from CNRS (LIRMM) and IFREMER are developing new technological and operational biologging solutions.
The objective is to propose electronic systems, called electronic tags, which will be hooked onto the targeted marine species and will be capable of collecting information on individuals and their environment, then transmitting it via satellites. In addition to developing low-cost, low-disturbance solutions for the tracked animals, the originality is to supplement environmental and geolocation information with physiological information about the animal to link geolocation with the state and activity of the animal (feeding, reproduction, growth...).
This information is obviously crucial to understand the species and subsequently take effective management and protection actions. In particular, in the context of the FishNchip project (EMFF EU funding), the objective is to develop an implantable device to measure the composition of bluefin tuna flesh based on bioimpedance measurements, to observe the reproduction events and thus identify and characterize the tuna breeding areas.
To perform the impedance spectroscopy, we have designed a circuit in TSMC0.18µm technology by EUROPRACTICE. At the end of the project, the integrated circuit will perform an impedance spectroscopy on 22 frequencies in less than 200ms over a frequency range from 4Hz to 8MHz. The measurement can be configured in 2-points or 4-points. After manufacturing, the circuit has been compared with measuring instruments. A new version of the circuit is planned in 2021 to correct some bugs and improve the performances.

Why EUROPRACTICE?

We use EUROPRACTICE for the technology they offer and the associated services.

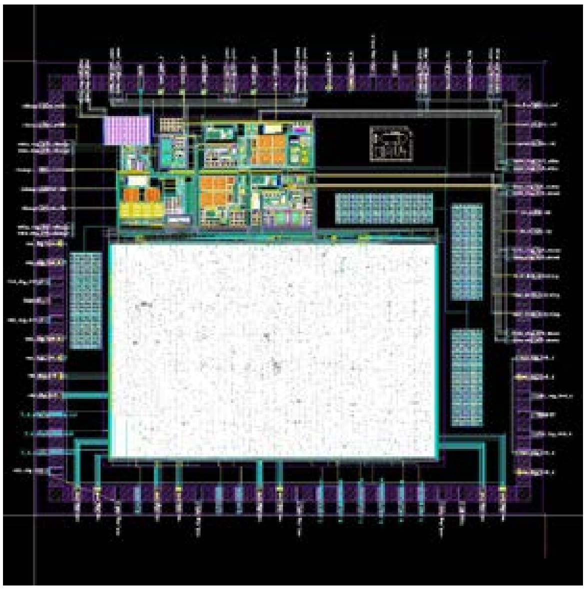


Fig1: Layout of the designed circuit.

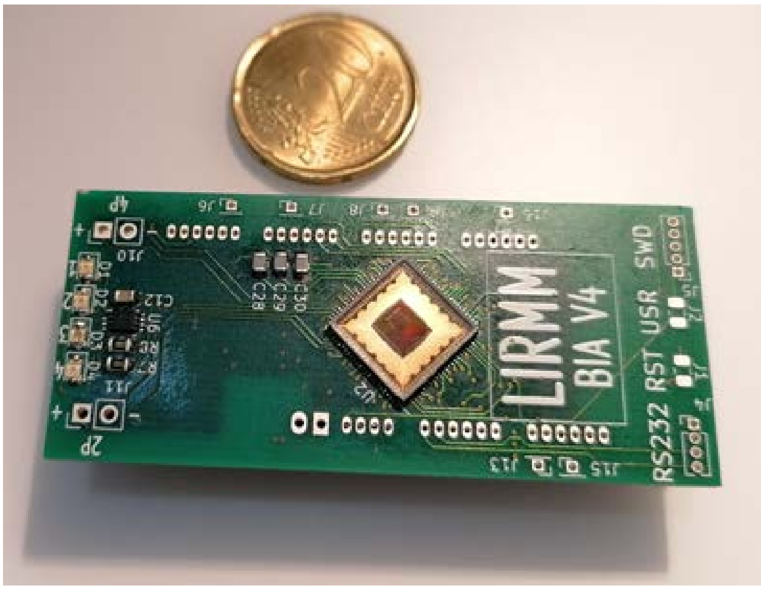


Fig.2: Test board with a fabricated die, mounted in the center.

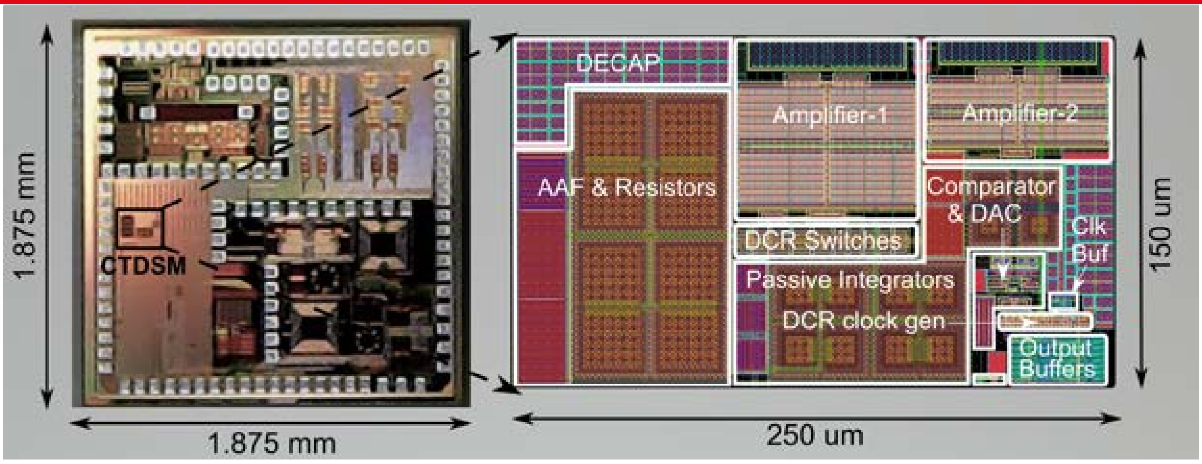


Fig.1: (left) Complete micrograph of the test chip, highlighted inside is the designed CTDSM for the application and (right) the detailed layout of the designed CTDSM.

Test chip module: A 400 mV Continuous-Time Delta Sigma Modulator for Multichannel Biomedical Applications

Mixed-signal group,
Department of Electrical Engineering,
Indian Institute of Technology Bombay, India

Designers: Laxmeesha S, Maryam Shojaei Baghini
Supervisor: Prof. Maryam Shojaei Baghini
E-mail: mshojaei@ee.iitb.ac.in
Technology: UMC 65nm Logic/MM/RF-LL (mini@sic)
Die size: 1875µm × 1875µm

Description

Demands for monitoring and recording of various bio-potential signals have been increased for the implementation of numerous multichannel, portable and implantable electronic medical systems. Implantable recording systems with parallel recording channels present challenges in the form of high-density and very low power consumption. The systems generally exhibit very low power consumption characteristics since they must operate for months or years without battery replacement and help reduce the risk of damaging surrounding tissues due to the dissipated heat. Reducing the operating voltage is one of the most effective ways to reduce the dynamic power consumption. Monitoring and recording biomedical signals of the human body require the conversion of multi-channel analog bio-potential signals into digital signals through ADCs. Compact, very low power (operating at a low voltage) and energy efficient ADCs are hence very essential for the longevity of portable and implantable medical systems.

The continuous time delta sigma modulator (CTDSM) based ADC designed in this work operates at a low supply voltage of 400 mV for low power operation. For further power saving, a low oversampling ratio (OSR) CTDSM is realized by means of duty cycled integrators. The duty cycled integrators are realized using passive components leading to additional power saving. A novel differential amplifier with an inherent bulk based common mode feedback is utilized to isolate the passive integrator stages and provide the loop-filter gain of the CTDSM. An auto-shutdown comparator was designed to operate at a 400 mV supply voltage while still maintaining sub-µW power consumption. The auto-shutdown feature is essential since the reduced MOSFET stacking in the comparator leads to large power dissipation.

Measurement Results

The ASIC is realized in a 65 nm low-leakage CMOS process as shown in Fig.1. For a biomedical bandwidth of 10 kHz, at an OSR of 32 (clock frequency of 640 kHz), the CTDSM achieved a measured SNDR of 56.3 dB while consuming 160nW power, operating at 400 mV. Further, at an OSR of 128 (clock frequency of 2.56 MHz), the CTDSM achieved an SNDR of 64.7dB with a power consumption of 560 nW at 400 mV supply voltage. The CTDSM occupies an extremely small area of only 0.035mm^2 and exhibits an energy efficiency of 15 fJ/conversion at an OSR of 32, making it an ideal candidate for multichannel bio-potential acquisition systems.

Why EUROPRACTICE?

EUROPRACTICE provides students and research scholars access to the various semiconductor ASIC fabrication technologies to test and prototype their designs at affordable academic prices. EUROPRACTICE gave us excellent technical support during the entire design cycle from the GDSII preparation to the submission stage and finally to the packaging stage. The entire procedure is well planned by the EUROPRACTICE team.

Acknowledgments

- Department of Science and Technology (DST), SMDP-C2SD program of MeitY, Govt. of India.
- VLSI lab and Embedded Systems lab of the Department of Electrical Engineering, IIT Bombay

Programmable Readout IC for Photodiodes Array

Łukasiewicz Research Network - Institute of Microelectronics and Photonics, Warsaw, Poland

Contacts: Cezary Kolacinski*, Pawel Pienczuk, Andrzej Szymanski and Dariusz Obrebski
E-mail: ckolacin@ite.waw.pl

Technology: UMC L180 MM/RF
Die size: 4960μm × 1525μm
Design tool: Cadence Design Systems

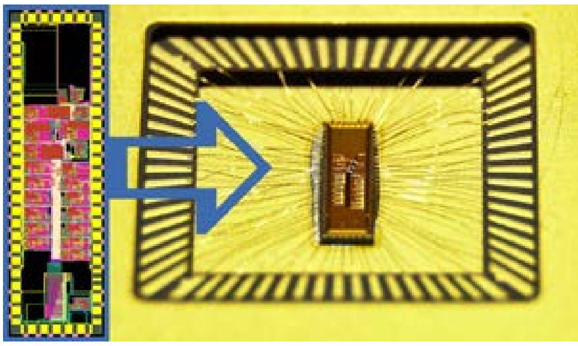


Fig.1: Layout of the designed structure (left) and fabricated chip mounted in PLCC package (right).

Description

Under the ParCour project, the established consortium develops a new particle counting technique, with an aim of cost and mobility. A new measurement apparatus will be based on a LED light source, additional optical systems, a unique photodiodes (PDs) array and a designed integrated circuit for readout. The PDs array is organized as a half ring structure consisting of 17 sections with different sizes and position - this structure has been manufactured using proprietary CMOS process of the Institute of Microelectronics and Photonics.

Dedicated readout chip – designed in UMC L180 MM/RF process - features 17 analog input ports, 17 analog output ports, SPI bus and several diagnostic and auxiliary ports.

Designed analog block consists of 17 separate channels, one for each photodiode forming the detection array. Signal path of each channel is composed of two amplification blocks: a transimpedance amplifier (TIA) and a voltage amplifier (buffer). Parameters of the particular channel has been suited to the expected characteristic of corresponding PD but the values of offset and current-to-voltage ratio (transconductance) can be controlled (within the limited range) by the 4-bit digital signals, independently for each channel.

Digital interface configures the analog block parameters – it consists of several calibration registers, accessible via the Serial Peripheral Interface (SPI). Power-on Reset (PoR) block resets registers at every power-up event.

Every time the power supply is switched on, the configuration process must be performed. It is realized with the mentioned SPI protocol and 2-byte data frame. Each configuration word addresses particular register in specific channel and passes 4-bit value in 11 least-significant bits. Last 5 bits are ignored. The channel to be controlled is addressed by 5 LSBs within the frame, while the register – by subsequent two bits.

Total current consumption has been estimated at 10mA for the complete chip (at 3.3V power supply). The structure fabricated in UMC CMOS 180nm technology occupies area of 4960μm x 1525μm and is equipped with 57 I/O pads.

Why EUROPRACTICE?

Łukasiewicz Research Network - Institute of Microelectronics and Photonics (formerly Institute of Electron Technology) is a longstanding member of EUROPRACTICE, with many ICs designed and fabricated over the last twenty years. The EUROPRACTICE MPW service offers an excellent opportunity for the prospective access to many mature technologies. EUROPRACTICE staff always provides superb assistance and knowledgeable feedback, which is a huge support for our design and prototyping processes.

Acknowledgement

This work has been supported by Poland Berlin-Brandenburg Project no. 2/POLBER-3/2018 Parcour – "Particle counter".

ReSCU-V2: SIL3 Safe-SoC according to IEC 61508

Institute for Computer Architecture and System Programming (ICAS), University of Kassel, Germany

Contacts: Prof. Dr.-Ing. Josef Börcsök, M. Sc. Waldemar Müller, M. Sc. Eike Hahn
E-mail: j.boercsoek@uni-kassel.de
Technology: UMC L180 MM/RF 1.8V/3.3V 1P6M
Die size: 5mm × 5mm
Design tools: Cadence digital design flow

Introduction

Today, in addition to system size, reduced system costs, optimized energy consumption and high reliability or safety, the aspects of functional safety are increasingly in the focus of many applications.

Description

The ReSCU-V2 safety chip consists of a 1oo2D safety architecture model (Fig.1) based on an asynchronous software comparator architecture. The design of the safety SoC is realized according to IEC 61508 standard. Internally the architecture has two redundant 32-bit microcontrollers of type ColdFireV2. Each side consists of 16KiB Cache and 32KiB SRAM, both enhanced with SECDED, as well as ethernet, QSPI, I2C, UART and CAN as peripherals. The complete SoC also features 78 FlexIO and 20 PWM, multiplexed with peripheral functions, as well as 8 ADC and 4 DAC channels. All FlexIO are equipped with real-time hardware on-chip diagnosis for every single IO, including self-test, that detects multiplexer status and correct function of the IO up to the bond pad without software intervention. ADC and DAC are also redundant, as well as isolated and provide diagnosis features. On top, there is a physically isolated watchdog on chip.

Both microprocessor systems are independent from clock, power and memory, called by standard free from interference. For crosschecking the safety-relevant results of both processors, they can communicate on-chip by two fast asynchronous interfaces.

Freedom from interference is also concerned for the back-end design, so both microprocessor systems are physically isolated by a 100µm wide gap. Additionally, all supply voltages need to be independent, which leads to eight power domains on chip for I/O, core, PLL and analog parts on both channels.

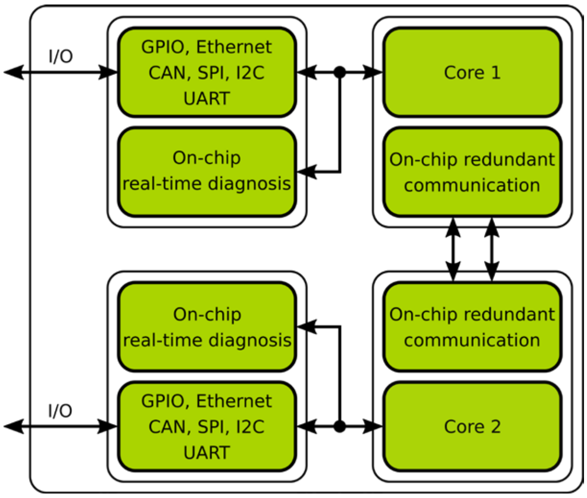


Fig.1: 1oo2D safety concept.

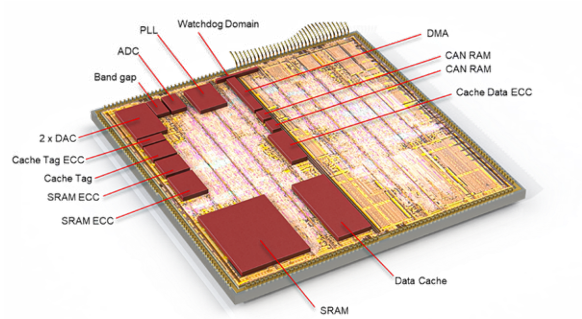


Fig.2: Physical layout of the safety SoC.

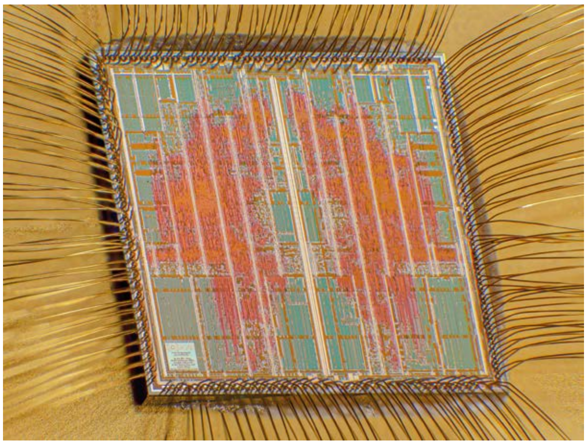


Fig.3: Photo of the ReSCU-V2 die.

The SoC was packaged into a CPGA256 package. It consumes < 500mW and runs stable at 100MHz from -40°C to +125°C.

Why EUROPRACTICE?

EUROPRACTICE gives the possibility to realize small research projects with limited funding. Additionally, the support by EUROPRACTICE for software and design issues is of big importance for small research groups.

References

http://www.uni-kassel.de/eecs/fachgebiete/icas/forschung/system-on-a-chip-soc/rescu-v2.html

NIRCA MkII - Control ASIC for IR image sensors

Integrated Detector Electronics AS (IDEAS), Oslo, Norway

Contacts: Amir Hasanbegovic, Gunnar Maehlum
E-mail: amir.hasanbegovic@ideas.no

Technology: UMC L180 Logic GII, Mixed-Mode/RF
Die size: 10mm × 10mm

Description

NIRCA MkII is the second-generation ASIC from IDEAS for readout from infrared (IR) image sensors, e.g., HgCdTe/MCT-based focal plane arrays (FPA). The ASIC aims at reducing the size, weight, power and cost (SWaP-C) of infrared sensor readout systems by integrating the necessary functions and performance on a single ASIC. The NIRCA MkII is a radiation-tolerant integrated circuit (IC) system-on-chip with operating temperature between -40°C and +85°C. This makes the ASIC highly suitable for meeting the requirements in Earth observation payloads on satellites. The illustration shows the die photo of the ASIC (with annotations). The ASIC includes 16 video channels (VADCs) and 1 auxiliary ADC (AADC), each with a 1x to 8x programmable gain amplifier and a pipeline ADC with 14-bit and 16-bit output options running at 12 Msps. Analog input offset is adjustable in the analog domain (SREF) with fine-tuning of gain and offset is possible in the digital domain. Digitized sensor data is output on a 9x480-Mbps high-speed serial LVDS interface. The ASIC provides a digital interface (DIN/DOUT) for controlling the sensor, and analog reference voltages (ODAC) for biasing the sensor. NIRCA MkII is programmed via an SPI interface. After a program has been loaded into the internal ECC RAM the internal sequencer can execute a variety of tasks, e.g., waveform generation, ADC sampling control, configuration and control of both internal analog and digital modules. The validation campaign is currently ongoing, and the results so far have been satisfactory.

Why EUROPRACTICE?

To make this design, we worked closely with imec, who provided IP and chip verification services. The design was submitted for fabrication by using EUROPRACTICE MPW services.

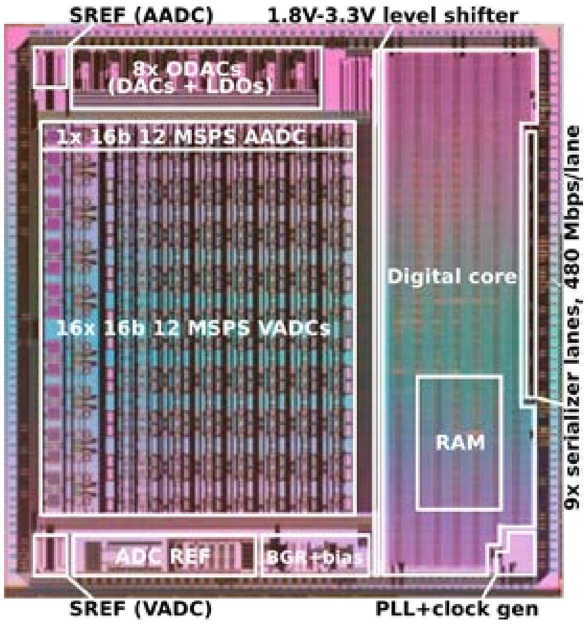


Fig.1: Bare die of NIRCA MkII.

Acknowledgements

The NIRCA MkII ASIC is developed under the ESA project Control ASIC for Earth Observation Infrared Detector (ESA Contract No. 4000119554/17/NL/BJ). The project has been funded by the European Space Agency (ESA), the Norwegian Space Agency (NSA) and IDEAS.

Read-out ASIC for GEM detectors

ASIC Lab, National Research Nuclear University «MEPhI», Moscow, Russia

Contacts: Eduard V. Atkin, Vitaly Shumikhin
E-mail: vvshumikhin@mephi.ru
Technology: UMC L180 Mixed-Mode/RF
Die size: 3240µm × 1525µm

Description

Nowadays gas electron multiplier (GEM) detectors are widely used in large-scale physical experiments, such as MPD (NICA), CBM (FAIR). During last few years a multichannel readout ASIC for GEM detectors with an asynchronous (self-triggered) architecture has been developed.

The developed ASIC is intended for read-out signals coming from GEM detectors. The prototype version of the ASIC contains 8 analog front-end channels for processing signals of both polarities up to 100 fC at maximum detector capacitance of 100 pF, followed by a 10-bit ADC in each channel and a digital signal processing system. After amplification and filtering of the detector signal in the analog channel, the ADC converts it at a maximum sampling rate of 25 MHz.

The chip has two modes of operation. In test mode, digital data from the ADC is serialized and directly buffered by mean of differential SLVS transmitters, working at a maximum frequency of 320 MHz. In operating mode, the data from the ADC of each channel is additionally processed by the interpolator. A slow serial interface is used to control the operation modes of the ASIC. To generate the clock signals in the chip the phase-locked loop unit (PLL) is used.

A specific feature of the chip is a usage of the digital domain interpolator for amplitude measurements. Using of the interpolator allows determining signal maximum in ASIC at high accuracy: 1 LSB for 10 bits ADC (simulation results).

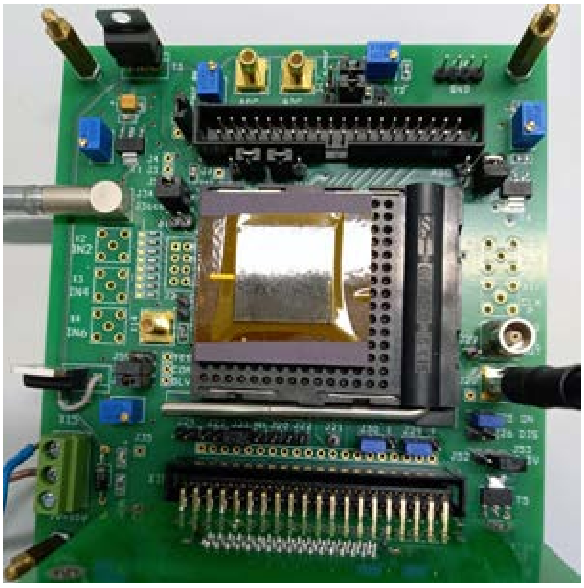


Fig.2: Lab measurement setup.

Results

The ASIC has been implemented in 0.18 µm UMC L180 Mixed-Mode/RF CMOS process and packaged into CPGA 120 case. The layout and die photo are shown in Fig. 1. The lab measurement setup, shown in Fig. 2, has confirmed the expected ASIC functionality.

Why EUROPRACTICE?

EUROPRACTICE provides a unique opportunity for our University to have a well-scheduled access to a wide range of advanced technological processes. It is also important, that the approach is cost-effective. This allows making a simple choice of right technology for each R&D project, keeping in mind possibility of further engineering runs for a small volume reproduction of chips. An expert support on installation and usage of PDKs jointly with advanced EDA tools gives additional benefit to our designers.

Acknowledgement

This work was supported by Grant No. 18-79-10259 of the Russian Science Foundation.

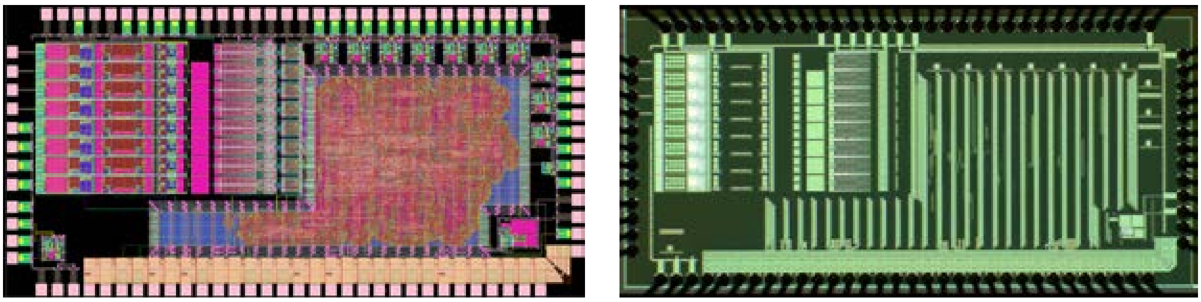


Fig.1: ASIC layout versus die photo.

Servo Drive Controller ASIC

Faculty of Engineering, Technical University of Applied Sciences Rosenheim, Germany

Contact: Dr. Martin Versen
E-mail: martin.versen@th-rosenheim.de
Technology: X-FAB XH018 0.18µm E-FLASH MET3/4/MID/THK
Die size: 3226µm × 2962µm
Design tools: Cadence: Virtuoso, Genus, Innovus

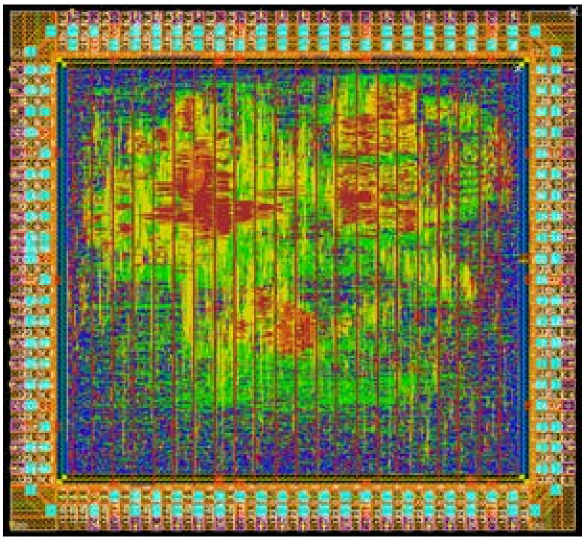


Fig.1: Layout view of the servo drive controller

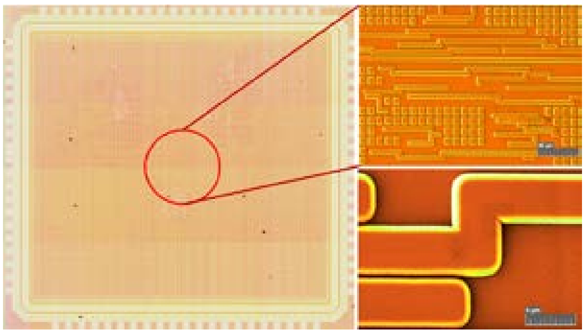


Fig.2: Microscope views of the fabricated chip

Description

Position-controlled servo drives are widely used in automation systems. A cascaded control structure with a current controller as innermost control loop is used. As controller usually consists of proportional, integral and differential (PID) elements, the motor control ASIC is a configurable PID controller. The configuration is achieved by a serial peripheral interface (SPI). The motor controller acts a SPI slave. Digital inputs connect to three delta-sigma modulators which sample at an input frequency of 16MHz. One analog input receives a current input signal, while the other two interface to the A/B signal of a rotary or a linear encoder. Three $sinc^3$ decimation filters are implemented with variable filter lengths between 16 and 256 to reduce the noise of the serial 1-bit input data streams. For the motor control, the output signal switches a full bridge assembly with an adjustable resolution of up to 16bit with a device frequency of 100MHz. The project includes a digital output interface for two 16bit digital-analog converters (DAC) so that we can visualize control loop variables with an oscilloscope on-line.
The servo drive controller is going to be used in lab practices for mixed-signal systems in the master program of the university.

Why EUROPRACTICE?

The Technical University of Applied Sciences Rosenheim has licensed Cadence Tools through EUROPRACTICE for several years. We have benefitted from EUROPRACTICE's excellent technical support for dummy fill, chip submission and chip packaging. EUROPRACTICE has given us an affordable access to a multi-project wafer fabrication run.

Calibration pulser for high energy physics ATLAS detector at CERN

Centre de Microélectronique OMEGA – CNRS/ IN2P3-Ecole Polytechnique, Palaiseau, France

Contact: Gisele Martin-Chassard
E-mail: gisele.martin-chassard@in2p3.fr
Technology: XFAB XT018 0.18µm
Die size: 4.2mm × 2mm
Design tool: Mentor Calibre

Introduction

The ASIC calib_atlas will provide the calibration of the electromagnetic calorimeter for ATLAS experiment at CERN. The goal of the circuit is to generate variable high precision test pulses in each measurement channel of the detector over the whole energy range (16bits).

Description

The chip embeds a 16bit-DAC current followed by four high-frequency switches to provide four calibration channels as shown in the figure of the chip layout.

The 16bits DAC provides a current from 5µA (LSB) to 320mA with an integral non-linearity less than 0.1% in the 10-bits DAC range. Thanks to XFAB 10V transistors, we could make the high-frequency switches so that the output pulse could reach 7.5V on 25 Ohms load. The 6 metal levels are very efficient to drive properly a relatively high current.

Results

The dies are packed in QFN64 case. The tests show good results in term of dynamic range and linearity for the switch part, but more mitigated results for the 13-bit and 16-bit DAC parts. The chip, which will be used in high energy physics experiment, must be characterized in irradiation environment. Irradiation tests were performed in X-ray beam up to 3Mrad at CERN and in proton beam until 4 Mrad using Proton Irradiation Facility (PIF) of Paul Scherrer Institut (PSI). These tests show too big leakage current increase and Vt shift for standard 5V MOS to be able to keep the chip performances in CERN experiments. However, the results are acceptable for 10V MOS transistors. Seeing these results, we decided to redo a 13bit-DAC in another more rad-hard technology and keep in XT018 the high frequency switches and the 3 MSB DAC (as PMOS current mirrors). The new chip was submitted in August 2020 run.

Why EUROPRACTICE?

EUROPRACTICE MPW program offers designers and researchers the opportunity to prototype their designs at an affordable price. EUROPRACTICE staff provide excellent technical support through the different stages of the tape-out.

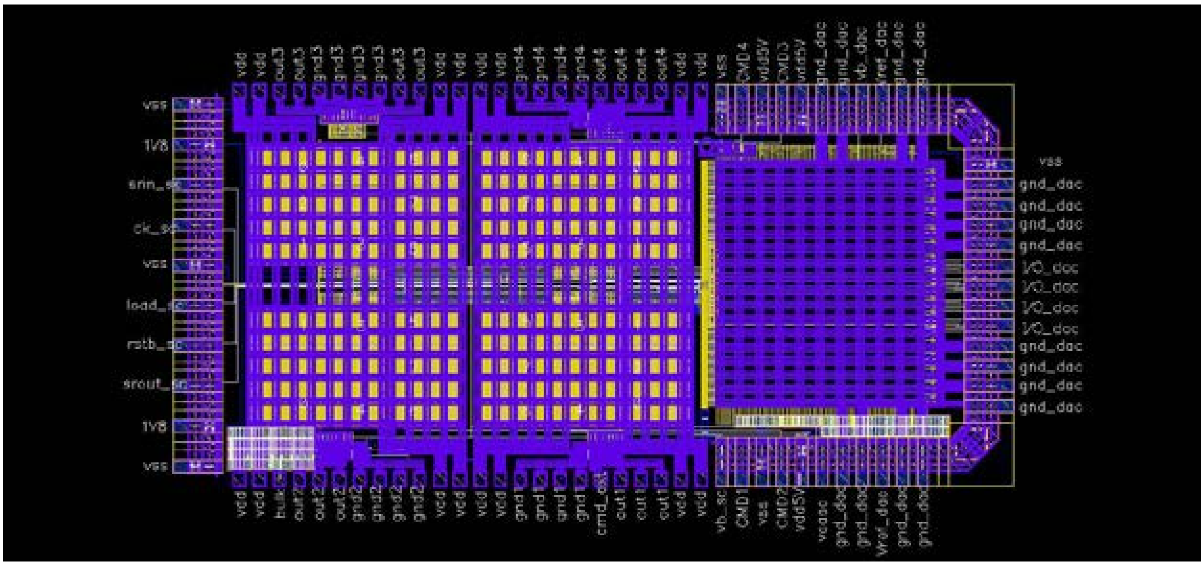


Fig.1: Layout of the designed chip.

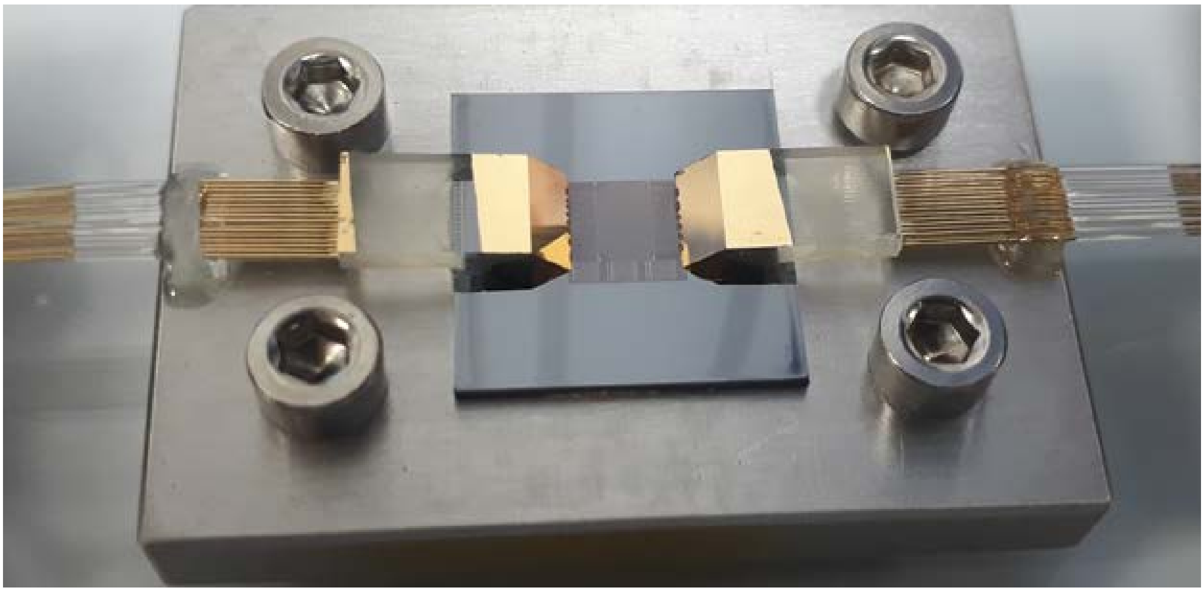


Fig.1: A Silicon-photonics chip fabricated at imec with specialized assembly at Tyndall of two fiber array attaches with gold coating.

Silicon-Photonics Array for Ultrasound Detection

Technion - Israel Institute of Technology, Haifa, Israel

Contacts: Y. Hazan, A. Rosenthal
E-mail: yoav.hazan@campus.technion.ac.il

Technology: Tyndall packaging & imec Si-Photonics Passives+
Die size: 5mm × 5mm (Full wafer to allow for post-processing)
Design tools: Synopsys OptoDesigner

Description

In biomedical application, the detection of ultrasound is commonly performed using piezo-electric transducers due to their ability to transmit and receive. Nevertheless, in new emerging hybrid imaging modalities, where only detection of ultrasound is required, piezo-electric technology does not provide the required bandwidth without compromising sensitivity. Ultrasound detection via optical resonators can perform with the required broad-bandwidth and sensitivity.
In this work, optical micro-resonators designed with OptoDesigner software and fabricated in Silicon-on-insulator technology at imec, scaling down to a few tens of microns with broad-bandwidth over 100MHz. In post-processing, polymer over-coating increases the sensitivity to few tens of Pascals, achieving sensitivity that enables bio-medical imaging. Finally, the Silicon resonators were fiber-coupled at Tyndall to allow interrogation and readout.

Why EUROPRACTICE?

EUROPRACTICE provides accessible, layout and simulation software, state-of-the-art fabrication and packaging technologies to small research institutes for rapid prototype manufacturing, which otherwise would be inaccessible or would take excessive time and money. The process design kit (PDK) provided by imec and used in Synopsys OptoDesigner layout software provided by STFC, made the design and layout process easy, using the well developed photonic integrated circuits (PIC) elements, then assembled and packaged by Tyndall National Institute. The professional technical support and humanly attention of STFC, imec and Tyndall was exquisite and greatly appreciated.

Design of High-speed Multi-lane Silicon Photonics MZM array

Department of Micro/Niao Electronics, Shanghai Jiao Tong University, China

Contact: Prof. Sun Yanan
E-mail: sunyanan@sjtu.edu.cn
Technology: imec Si-Photonics IsiPP50G
Die size: 5150µm × 5150µm

Introduction

Silicon photonics is becoming the technology of choice for optical transceivers in short reach optical interconnect systems. It leverages the existing microelectronic fabrication infrastructures, promising lower fabrication cost and larger scale integration than III-V photonics. To meet the performance requirement in bandwidth density and cost in next-generation high-performance computers and data centers, it is critical to achieve high-density integration of optical transceivers. However, using the principle of parallelism and scale-out the channel count, the large footprint and spacing of driving electrodes limit the bandwidth density. To overcome this limitation, a more compact device footprint and greater flexibility design is quite necessary.

Description

This work implemented a high-density and high-speed multi-lane traveling wave MZM array based on imec silicon photonics technology. We proposed a novel compact traveling-wave electrode structure for the MZM, and shared the ground pad between two neighboring MZMs to reduce the device size. Two MZM arrays with different lengths are designed in this chip. The optical eye-diagram measurement results show that MZM array can work at 25Gbps simultaneously with low crosstalk.

Why EUROPRACTICE?

The EUROPRACTICE provides accessible access to foundry services to research institutions that could otherwise not easily support regular fabrication costs. We have been working with EUROPRACTICE many years. In this work, we used imec silicon photonics technology ISiPP50G offered by the MPW service of EUROPRACTICE. We really appreciated EUROPRACTICE and imec technical support at every step of the chip design process, which significantly speeded up the development of the chip.

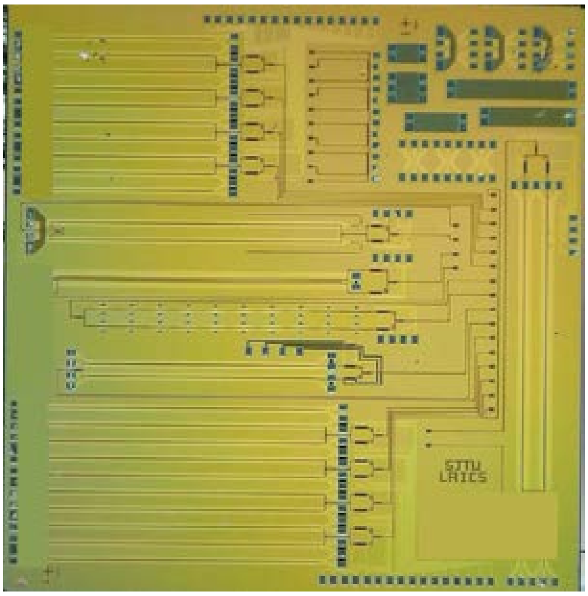


Fig.1: Photograph of the fabricated die.

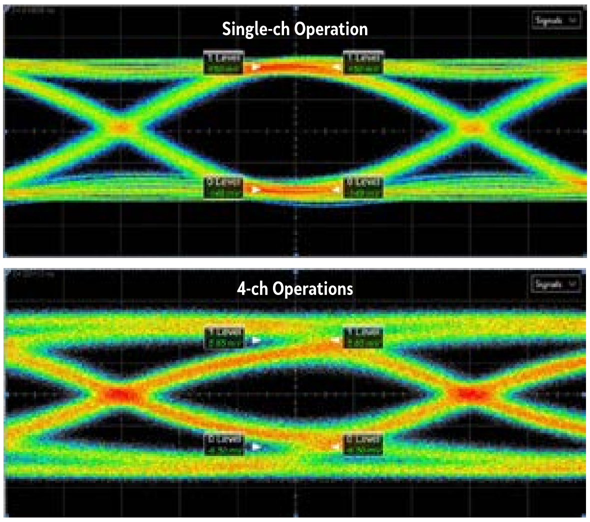


Fig.2 Optical eye diagrams of Tx channels at single-ch operation and simultaneously at all 4-ch operations.

Compact arrayed waveguide grating spectrometer for spectral-domain optical coherence tomography at 860 nm center wavelength on silicon nitride platform

Center for Advanced Research in Photonics, Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong

Contact: Hon Ki Tsang
E-mail: hktsang@ee.cuhk.edu.hk
Technology: imec SiN-Photonics BioPIX300
Die size: 10.75mm × 4.75mm

Description

The spectral domain optical coherence tomography (SD-OCT) is a three-dimensional (3D) imaging technique which obtain the information of the sample in depth direction by measuring the interference signal in spectral domain. A broadband and high-resolution spectrometer is the key component in SD-OCT system, which guarantees the large imaging depth and high imaging resolution in depth direction. Silicon nitride platform, with wide transparent spectral range, enables the operation of the spectrometer at the 860 nm center wavelength, which is often the spectral region of choice for in-vivo bio-imaging. We designed a 40-channel arrayed waveguide grating (AWG) spectrometer with 60 nm operating bandwidth and 1.5 nm spectral resolution.

Enabled by the high professional MPW service from imec under the PIX4life silicon nitride MPW, and especially with the high-quality devices fabricated, the AWG spectrometer we designed showed 1.3 dB experimental insertion loss and about -20 dB inter-channel crosstalk with experimental spectral resolution and optical bandwidth exactly matching with the design value. The total footprint of the AWG spectrometer is 910µm × 680µm. This AWG spectrometer with relatively good performance on silicon nitride also enabled our publication “Ultracompact 40-Channel Arrayed Waveguide Grating on Silicon Nitride Platform at 860 nm,” IEEE Journal of Quantum Electronics 56, 8400308 (2020).

Another paper has been submitted discussing the limitations on crosstalk performance in large-scale arrayed waveguides from the phase variations caused by nitride thickness nonuniformity and how alternative approaches can alleviate this problem for high resolution and wide optical bandwidth spectrometers.

The MPW service has also helped us to gain further research grant funding from Hong Kong government for developing integrated spectrometers for advanced dynamic optical coherence tomography.

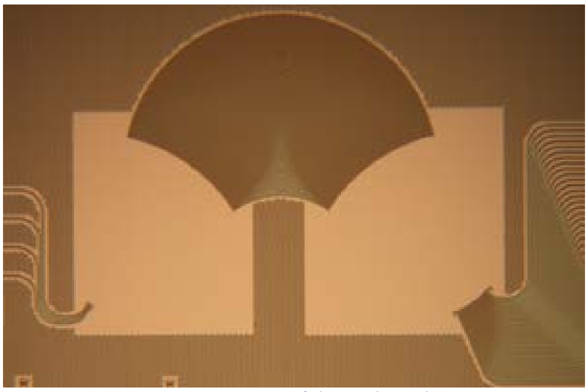


Fig.1: Microscope image of the 40-channel AWG spectrometer.

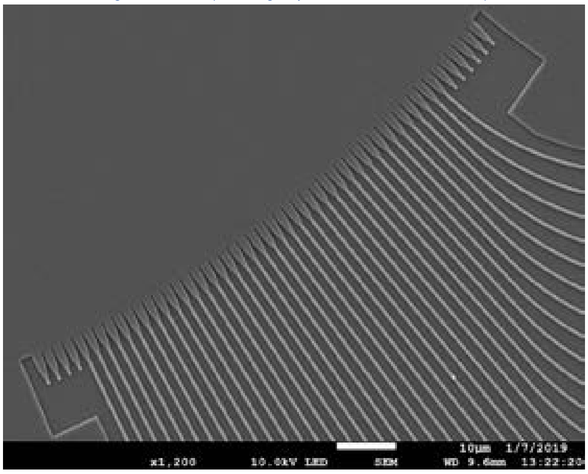


Fig.2: SEM image of parabolic tapers in the AWG spectrometer.

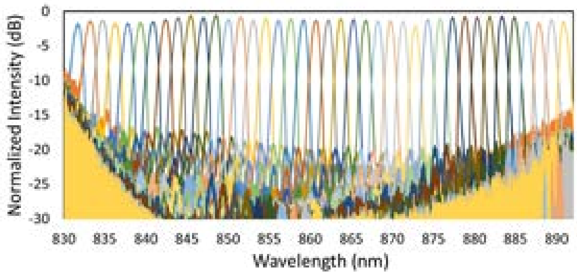


Fig.3: Experimental transmission spectrum of the AWG spectrometer.

PIX4life and EUROPRACTICE

Imec SiN-Photonics was developed within PIX4life, a European open-access pilot line for Photonic Integrated Circuits (PICs) targeting life science applications in the visible range. PIX4life services are available through EUROPRACTICE.

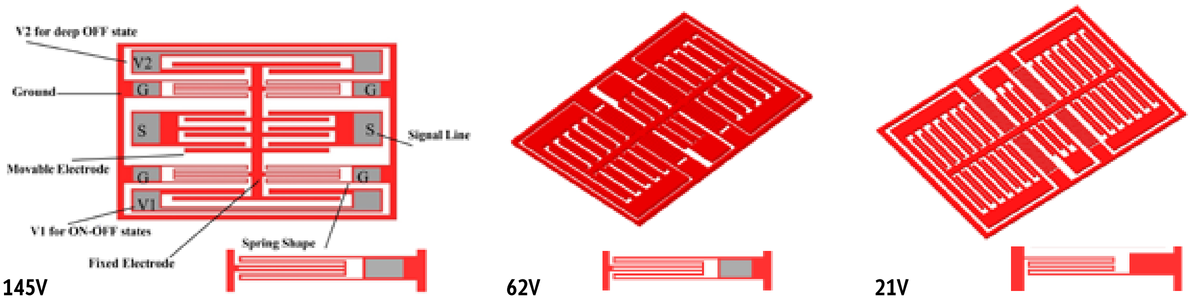


Fig.1: Design layouts for different 3-state non-contact Switches with varying comb lengths, including Spring details and pull-in Voltage simulated by Finite Element Analysis (FEA).

A Primary Study of Electrostatic Actuated Switch using the Technology of PiezoMUMPs

Department of Microelectronics and Nanoelectronics, University of Malta, Malta

Contact: Mounira Bengashier
E-mail: mounira.bengashier.15@um.edu.mt
Technology: PiezoMUMPs
Die size: 11.15mm × 11.15mm
Design tools: CoventorWare

Description

A number of non-contact electrostatic actuated switches were designed using the PiezoMUMPs technology and submitted to EUROPRACTICE for fabrication. These switches are of different designs and having various geometries in order to analyse and minimise the Pullin voltage. This work is part of a Ph.D. research study on the design of piezoelectric tuneable MEMS lateral bulk acoustic wave resonators originally based on the thermal effect on the resonant frequency in order to explore the feasibility of fine frequency tuning. The possibility of fine tuning can be applied to high precision timing circuits such as frequency counters. The possibility of having a switchable array of different resonators in the same chip results in a cost-effective wider frequency range. These non-contact electrostatic switches were analytically studied and simulated using CoventorWare FEM.

Proposed Design Geometry

The switch was fabricated using MEMSCAP's PiezoMUMPs Process. Figure 1 shows the first designed switch including the shape of one of the 4 springs having the following dimensions: Signal line, movable electrode gaps are 3,9 µm, Signal line, movable electrode Overlap is 110 µm, Gap between two actuation electrodes is 11.5 µm, Switch's geometry (W, L, T) are (320, 500,10) µm. The simulated pull-in voltage for designs having a different number of comb fingers obtained using CoventorWare FEM analyser tool are also shown in Figure 1. The pull-in voltage was further reduced to 21 V by reducing the spring stiffness. This was achieved by changing the spring geometry, having a length and width of 160 µm and 24 µm respectively.

Why EUROPRACTICE?

The EUROPRACTICE service offers affordable simple procedures to access the technology to produce MEMS prototypes for research purposes, and this service is always open to provide support and answer questions regarding technical issues encountered by the users.

Acknowledgement

We would like to acknowledge the Ministry of High Education in Libya for supporting the Ph.D. research work of Mounira Bengashier, which is currently being carried out at the Department of Microelectronics and Nanoelectronics at the University of Malta.

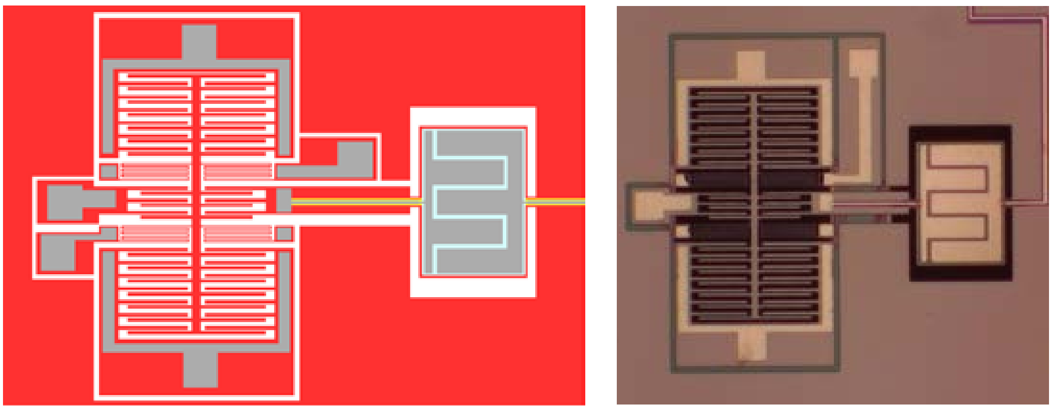


Fig.2: The final selected 3-state non-contact Switch connected to a PiezoMUMPs resonator.

Z-axis MEMS Accelerometer for Vibrotactile Display Pad

Department of Electronic and Electrical Engineering, University of Bath, UK

Contacts: Dr Ali Mohammadi, Mr Steven Ng
E-mail: am3151@bath.ac.uk

Technology: X-FAB MEMS XMB10
Die size: 4mm × 2.5mm
Design tools: Coventor MEMS+, Cadence

Description

Assistive technologies such as Braille and swell papers have been evolved to digital tactile displays, which help the visually impaired (VI) individuals to receive graphical information through the sense of touch. At the University of Bath, we have developed a new high-resolution vibrotactile display technique [1] following the feedback received from researchers in the Departments of Computer Science, Psychology and Education. Our technique allows one electromagnetic coil to selectively vibrate multiple smaller tactile pixels (taxels) based on their mechanical resonance frequency. This technique mitigates the resolution bottleneck of existing tactile displays. We now investigate the integration of tactile sensing mechanism in the new actuator to control the vibration of tactile elements. This sensor will allow the implementation of a closed-loop control system to accurately track the resonance frequency of taxels. In addition, the proposed sensor will create an interactive and bilateral communication to receive tactile input from the user.

Thereby, we have embedded off-the-shelf piezoelectric sensors underneath the taxels to track the resonance frequency of the taxels. However, the bulky size of these sensors avoids using individual sensors especially in the high-resolution taxel configuration, whereby multiple taxels are implemented within a small area. In this project, we have designed capacitive MEMS sensors in XFAB processes to measure the vibration of 3D printed taxels. The capacitive sensors built in XMB10 processes will measure the displacement of taxels in Z direction and supply the measured output as the feedback signal to the actuator input.

References

[1] A. Mohammadi, M. Abdelkhalek, and S. Sadrafshari, *"Resonance frequency selective electromagnetic actuation for high-resolution vibrotactile displays,"* Sensors and Actuators A: Physical, vol. 302, p. 111818, 2020.

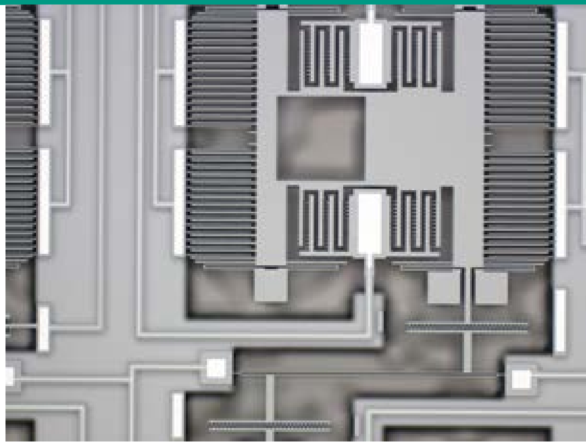


Fig.1: SEM image of the z-axis accelerometer with comb finger capacitive transducers for sensing and actuation purposes.

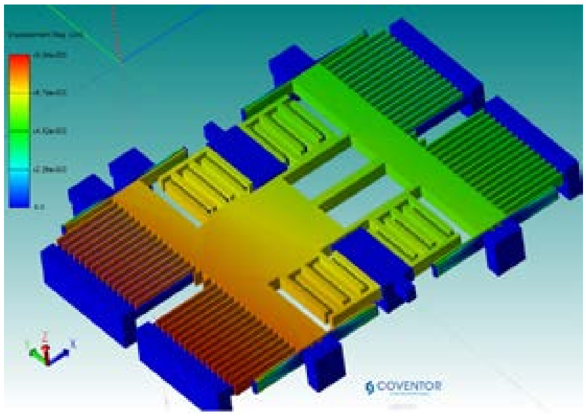


Fig.2: The proof mass deflection in the heavier side is larger than the lighter side, which is needed for measuring out-of-plane acceleration.

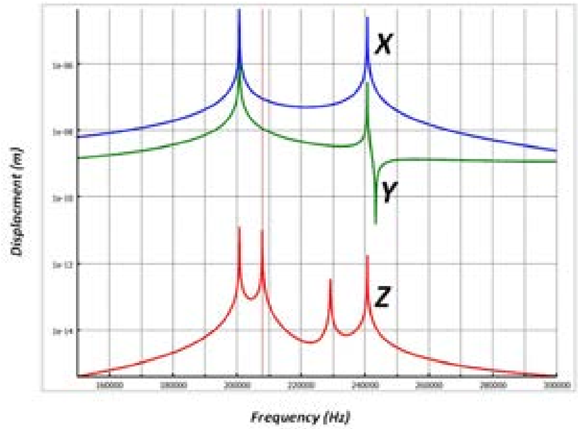


Fig3: Harmonic analysis in Coventor MEMS+ shows the resonant modes in X, Y and Z direction.

Acknowledgement to EUROPRACTICE and X-FAB

EUROPRACTICE microfabrication and software services helped us to establish a new line of research in Microelectromechanical Systems (MEMS) at University of Bath. We highly appreciate the availability of technical guidance and expertise, choice of reliable microfabrication process technologies, and reasonable prices – all provided by EUROPRACTICE. The training programs for software and webinars for process technologies are extremely useful services. This project was specifically supported by the X-FAB and EUROPRACTICE MEMS Design Award in 2020.

A scanning diffraction grating for high performance gas sensing applications

University of Malta - Department of Microelectronics and Nanoelectronics, Msida, Malta

Designer: Russell Farrugia
Supervisor: Prof. Ivan Grech, Prof. Joseph Micallef
E-mail: russell.farrugia@um.edu.mt

Technology: X-FAB MEMS XMB10
Die size: 4.5mm × 2.2mm
Design tools: CoventorWare

Introduction

The University of Malta is currently developing an infrared Czerny-Turner spectrometer for multi-gas detection. In the spectrometer design of Figure 1, a collimated broadband IR source is directed towards a diffraction grating. The diffracted beam is then focused on to the detector plane using an imaging mirror. The spectral image is typically measured using an expensive linear photodetector array. The latter can be replaced by a single element photodetector with the implementation of a MEMS scanning diffraction grating. The design of a novel MEMS scanning grating was fabricated using the XFAB XMB10 process. Figure 2 depicts the layout of the 2.2 mm × 4.5 mm chip. The MEMS scanning grating enables the realization of a compact IR spectrometer for high speed, high resolution gas spectral analysis and eliminates the problems of cross-sensitivity and decay which characterize metal oxide gas sensors.

Description

The scanning grating of Figure 3 is designed to oscillate at a torsional out-of-plane resonant mode at a frequency of 2 kHz. The resonating micro-scanner is driven by angular vertical comb drive structures. The electrostatic and mirror plate structures are etched from the 30µm silicon device layer. A lamellar grating pattern is formed using the 5µm deep DRIE process step, typically intended for the fabrication of comb fingers with a reduced height. The aluminum layer, intended for wiring and bond pad metallization is considered in order to improve the reflectivity of the grating pattern. The scanning mirror plate is supported on either side by dual torsion beam structures. The torsion beams are optimized such that the torsional stiffness is minimized, and the lateral and out-of-plane bending stiffness is maximized. Lateral springs are also included in the scanning grating design to

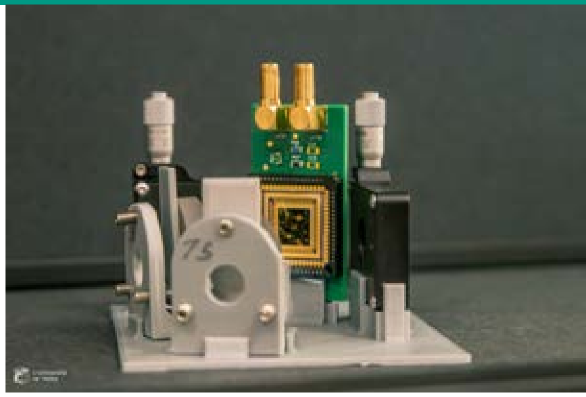


Fig.1: Czerny-Turner Spectrometer prototype design.

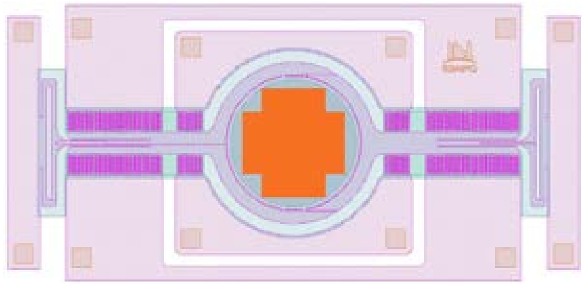


Fig.2: Layout of the fabricated chip.

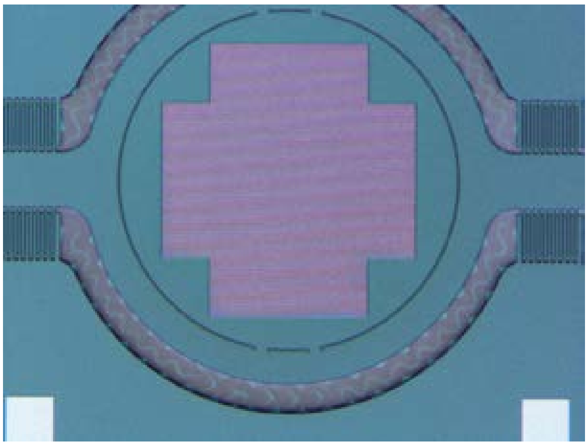


Fig.3: SEM image of the indirect-drive resonant micro-mirror.

provide a degree of compliance against external forces along the rotational axis. Moreover, stoppers are added to the end of the torsion beams to limit excessive out-of-plane rotation.

Why EUROPRACTICE?

EUROPRACTICE provides doctoral students, researchers and academics with access to state-of-the-art MPW foundry services for the fabrication of MEMS/MOEMS device prototypes. The University of Malta has always been provided with the necessary technical feedback and expertise at every stage of the chip design process.

Acknowledgements

The authors would like to acknowledge imec/EUROPRACTICE for their support through the MEMS Design Contest for Users of chip design in X-FAB XMB10 technology and Malta Enterprise for their financial support as part of the PENTA project ESAIRQ.

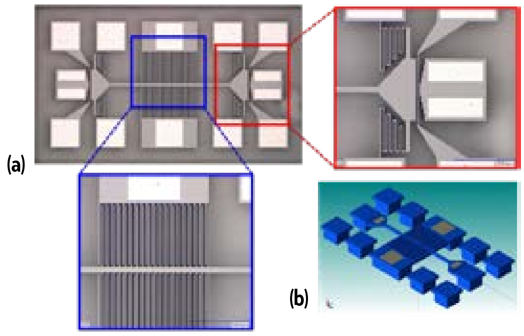


Fig.1: (a) Top-view micrograph of the fabricated comb-drive actuator, with zoom-in on some finer features (interdigitated combs, springs, and stepped electrostatic gate region). (b) 3D device layout using XMB10 PDK in CoventorWare MEMS+. The software supports mask generation from the in-built process module.

Silicon MEMS comb-drive actuators for strain engineering

Dept. of Precision and Microsystems Engineering, Delft University of Technology, the Netherlands

Contacts: Satadal Dutta, Peter G. Steeneken, Gerard J. Verbiest
E-mail: s.dutta-1@tudelft.nl
Technology: X-FAB MEMS XMB10
Die size: 3mm × 3mm
Design tools: Coventor MEMS+

Description

We designed a set of electrostatic comb drive actuators (Figs. 1, 2a) and piezo resistive MEMS actuators (Fig. 2b) in silicon, with varying configurations and geometry. These can be used to gain strain control in suspended metallic or semiconducting membranes for static as well as dynamic excitations. These are beneficial for the development of new sensors and increasing the outreach of standard silicon MEMS technology.

Micro-machined comb-drive (CD) actuators have been developed in the last years from highly p-doped silicon, which allows low-temperature operation [1][2]. The actuators are intended to be driven differentially to increase the range of linearity between small signal force and displacement. The XMB10 process allowed us to place silicon membranes of recessed height (in the vertical axis), which enabled us to integrate a vertical electrostatic gate with an air gap of 5µm. The strong bending thickness of the active layer allows us to gently push on the suspended comb without destroying it (Fig. 1). The relatively high p-doping is beneficial for the combs to be actuated both at room temperature and also at around liquid nitrogen temperature. An important parameter is the stroke of the interdigitated fingers. We need enough stroke to induce a few percent of strain in a membrane longer than 10 microns. The meshed design of the movable comb (Figs. 1, 2a) helps in reducing the inertial mass and thus increasing the stroke in the lateral direction. Further, we opted not to include the capping wafer during fabrication, and the yield of our devices was still very good (> 95 %). The exceptions were four broken devices with spring-structures of very high lateral aspect ratio (> 20). Various configurations of comb-drive actuators were implemented which can be used to generate both shear (uniaxial, radial) and torsional strain on the plane of the die. The process includes ohmic contacts to silicon, which allowed us to design piezo-resistive MEMS actuators, in the form of silicon loops connecting two bond pads (Fig. 2b), with the thinnest finger with being 2 µm. The simulated fundamental eigenfrequency of the movable comb in our design was 39.15 kHz, with a total displacement of 0.15 µm for a bias of 10 V at 300 K.

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The EUROPRACTICE makes it easier and affordable for academia to access a wide range of foundry services under a common umbrella. The active design support is also valuable for research. The available component library of XMB10 and its consolidated process design kit with 3D design software such as Coventor MEMS+ helps the researchers to simplify and to improve the prototyping of active and passive devices by ensuring final top-quality.

Acknowledgment

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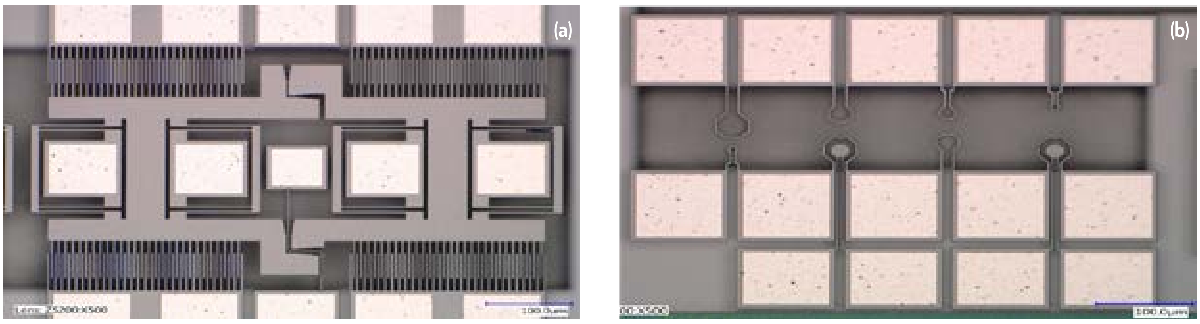

Fig. 2: Top-view die micrographs of (a) a variant of the comb drive actuator and (b) the piezo-resistive MEMS actuators.

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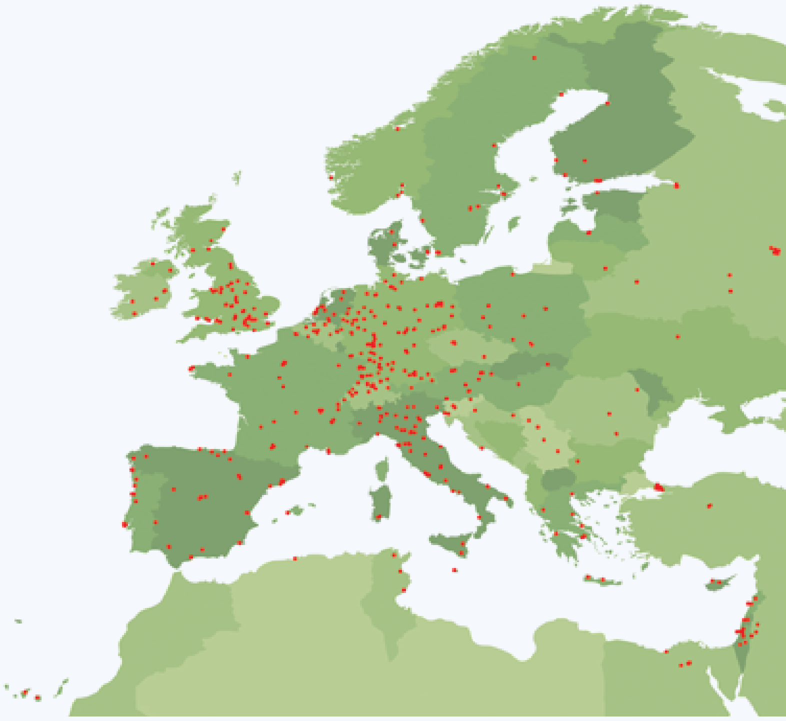

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A40100	Uniwersytet Zielonogórski
A40120	Politechnika Warszawska
A40130	Politechnika Lódzka - Mikroelektroniki I Technik Informatycznych (DMCS)
A40140	Akademia Górniczo-Hutnicza im. Stanislawa Staszica
A40150	Instytut Fizyki Jadrowej im. Henryka Niewodniczanskiego
A40160	Politechnika Wroclawska
A40530	Politechnika Slaska
A47300	Politechnika Gdanska
A47400	Politechnika Poznanska - Inzynierii Komputerowej
A47670	Politechnika Poznanska - Radiokomunikacji
A47740	Politechnika Lódzka - Pólprzewodnikowych I Optoelektronicznych
R22610	Institute of High Pressure Physics (UNIPRESS)
R40030	Siec Badawcza Lukasiewicz - Instytut Mikroelektroniki I Fotoniki
R49030	Instytut Podstawowych Problemów Techniki PAN (IPPT-PAN)
R49050	Bioinfobank Institute
R49080	Centrum Badan Kosmicznych PAN

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A12550	Universidade do Minho
A13710	Instituto Superior de Engenharia de Lisboa
A35540	Universidade do Porto
A35670	Universidade de Aveiro
A35970	Instituto Superior Técnico
A37230	Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento
R14120	Instituto de Telecomunicações - Lisboa
R21710	Laboratório de Instrumentação e Física Experimental de Partículas
R21750	International Iberian Nanotechnology Laboratory
R21890	Instituto de Telecomunicações - Aveiro
R22170	Instituto de Sistemas Robótica (ISR-UC)

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A15560	Universitatea Tehnică "Gheorghe Asachi" din Iași
A16070	Universitatea Transilvania Brasov
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R49060	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Particle Physics

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A47330	St. Petersburg State Polytechnical University
A47520	National Research University of Electronic Technology (MIET)
A47790	St. Petersburg State University of Aerospace Instrumentation
A47810	Lomonosov Moscow State University
A47850	Moscow Institute of Physics & Technology (MIPT) - Wireless Technologies
A47990	St. Petersburg Electrotechnical University 'LETI'
A48030	Omsk State Technical University
A48040	Moscow Institute of Physics & Technology (MIPT) - Control Systems
A48130	Ufa State Aviation Technical University
A48140	Ulyanovsk State University
A48160	Southern Federal University
A60030	Tomsk State University
A60040	Tomsk State University of Control Systems and Radioelectronics
A60060	Mordovian State University named after N.P.Ogarev
A60080	Novosibirsk State Technical University
A60100	National Research University Higher School of Economics
A60110	National Research Nuclear University MEPHI
A60150	Moscow Institute of Physics & Technology (MIPT) - Photonics
A60160	Bauman Moscow State Technical University - Kaluga
A60170	Moscow State Technical University of Radioengineering, Electronics and Automation
A60190	Bauman Moscow State Technical University - Moscow
A60200	Rzhanov Institute of Semiconductors Physics
A60220	Voronezh State Academy of Forestry Engineering
A60230	Samara National Research University (Samara University)
A60240	National University of Science & Technology 'MISiS'
A60250	Bryansk State Technical University
R21930	Scientific Manufacturing Complex "Technological Centre" MIET (SMCTC)
R47900	Budker Institute of Nuclear Physics
R49070	Space Research Institute (IKI)
R49210	Institute of Physical Materials Science (IPMS SB RAS)

Serbia

A47510	Univerzitet u Nišu
A47600	Univerzitet u Novom Sadu
A48010	Univerzitet u Beogradu
A48170	Univerzitet u Kragujevcu

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A40050	Slovenská technická univerzita v Bratislave
A47930	Technická univerzita v Kosiciach

Slovenia

A40280	Univerza v Ljubljani
A47690	Institut "Jozef Stefan"
A47820	Univerza v Mariboru
R22580	Skylabs Vesoljske Tehnologije Doo

South Africa

A14560	University of Pretoria

Spain

A12320	Universidad Politécnica de Cartagena
A12590	Universidad de Castilla - La Mancha
A13150	Universitat de València
A13340	Universidad de Alcalá
A13860	Universidad de Salamanca
A14720	Universidad de La Laguna
A15370	Universidad de Deusto
A16290	Universitat Pompeu Fabra
A16340	University of Vigo - AtlanTTic
A35130	Universidad Politécnica de Madrid - Departamento de Ingeniería Electrónica
A35190	Universitat Politècnica de València
A35870	Universidad de Sevilla - Instituto de Microelectrónica de Sevilla (IMSE-CNM)
A35891	Universidad de Cantabria
A36250	Universitat Autònoma de Barcelona
A36390	Universidad de Las Palmas de Gran Canaria - Instituto Universitario de Microelectrónica Aplicada (IUMA)
A37060	Universidad de Zaragoza - Dpto.Ingenieria Electronica y Comunicaciones
A37080	Universidad de Santiago de Compostela
A37330	Universidad Complutense de Madrid
A37580	Universidad de Malaga
A37690	Universidad del Pais Vasco
A38330	Universidad de Vigo
A38360	Universitat de les Illes Balears
A38580	Universidad de Sevilla - Ingenieria Electronica
A38590	Universidad de Granada
A38600	Universidad de Navarra
A38660	Universitat de Barcelona
A38780	Universidad de Las Palmas de Gran Canaria - Departamento de Informàtica y Sistemas
A38790	Universidad de Zaragoza - Facultad de Ciencias
A38820	Universidad Politécnica de Madrid - Centro de Electrónica Industrial
A39080	Universidad de Extremadura
A39100	Universidad Pública de Navarra
A39150	Universitat Politècnica de Catalunya - Departamento de Ingeniería Electrónica (Campus Nord)
A39180	Universitat Rovira i Virgili
A39390	Universitat Autónoma de Madrid
A39540	Universidad Carlos III de Madrid
R00060	CNM - Instituto de Microelectrónica de Barcelona
R20700	Ikerlan
R20850	Centre Tecnològic de Telecomunicacions de Catalunya
R21230	Instituto de Fisica Corpuscular
R21520	Institut de Ciències de L'Espai
R21550	Institut de Ciències Fotòniques
R21740	Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
R21910	Instituto de Tecnologías Físicas y de la Información
R22100	Centro Nacional de Supercomputación, Barcelona
R22460	Consorcio ESS Bilbao
R22470	Asociacion Centro Tecnológico
R22600	Centro Tecnológico de Automoción de Galicia

Sweden

A00260	Luleå tekniska universitet
A13720	Uppsala universitet
A16350	Stockholms universitet
A16360	Kungliga Tekniska Hogskolan, Stockholm
A37350	Linköpings universitet
A37370	Lunds universitet
A38180	Kungliga Tekniska högskola, Kista
A38670	Chalmers Tekniska högskola
A39840	Mittuniversitetet
R20690	Research Institutes of Sweden, ICT Acreo
R20910	Totalförsvarets forskningsinstitut FOI
R21700	MAX IV Laboratory
R21990	European Spallation Source
R22050	Institutet för Rymdfysik

Switzerland

A05000	Scuola Universitaria Professionale della Svizzera Italiana
A12730	École Polytechnique Fédérale de Lausanne - Laboratoire de Physique des Hautes Energies
A12920	Universität Zürich
A13090	Università della Svizzera Italiana
A13630	Université de Genève
A13780	Hochschule Luzern
A14780	Haute école d'ingénierie et d'architecture Fribourg
A15480	Universität Basel
A15530	Universität Bern
A16440	Universität Zurich
A36110	École Polytechnique Fédérale de Lausanne - Microelectronics Systems
A37340	École Polytechnique Fédérale de Lausanne - Neuchâtel
A38100	Ostschweizer Fachhochschule
A38310	Eidgenössische Technische Hochschule Zürich
A38410	Berner Fachhochschule
A38800	Eidgenössische Technische Hochschule Zürich - Basel
A39760	Haute école du paysage d'ingénierie et d'architecture de Genève
A39820	Fachhochschule Nordwestschweiz
R20350	Organisation Européenne pour la Recherche Nucléaire
R20680	Centre Suisse d'Electronique et Microtechnique - Neuchâtel
R20800	Paul Scherrer Institut
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich
R22180	Eidgenössische Materialprüfungs- und Forschungsanstalt

The Netherlands

A00170	Universiteit Twente - CAES
A12010	Vrije Universiteit Amsterdam
A12650	Radboud Universiteit Nijmegen
A13730	Stichting Saxion
A14510	Rijksuniversiteit Groningen
A15420	Erasmus Universitair Medisch Centrum Rotterdam
A15960	Universiteit van Amsterdam
A35491	Universiteit Twente - Electrical Engineering
A35701	Technische Universiteit Delft
A38050	Technische Universiteit Eindhoven
R00280	Nikhef
R20370	TNO-FEL
R20430	European Space Agency - ESTEC Microelectronics
R20520	Stichting Nederlandse Wetenschappelijk Onderzoek Instituten / Stichting ASTRON, Netherlands Institute for Radio Astronomy
R20540	European Space Agency - ESTEC Payload Technology
R21200	Stichting imec Nederland
R21250	NWO-I/SRON

Tunisia

A12930	École Nationale d'ingénieurs de Sfax
A15300	École Nationale d'ingénieurs de Tunis
R22570	Center for Research in Microelectronics and Nanotechnology

Turkey

A13010	Sabanci Üniversitesi
A13270	Hacettepe Üniversitesi
A13820	Koc Universitesi
A14250	Yeditepe Üniversitesi
A14730	TOBB Ekonomi ve Teknoloji Üniversitesi
A15280	Orta Dogu Teknik Üniversitesi Kuzey Kibris Kampusu
A15680	Ankara Yildirim Beyazit Üniversitesi
A15870	Istanbul Bilgi Üniversitesi
A15970	Özyegin Üniversitesi
A16250	Istanbul Medipol Üniversitesi
A16550	Maltepe University
A37960	Istanbul Teknik Üniversitesi
A38270	Ihsan Dogramaci Bilkent Üniversitesi
A38440	Orta Dogu Teknik Üniversitesi
A39170	Bogaziçi Üniversitesi
R20360	Türkiye Bilimsel ve Teknik Arastirma Kurumu Uzay Teknolojileri Arastırma Enstitüsü
R38860	Türkiye Bilimsel ve Teknik Arastirma Kurumu -BILGEM

UK

A12260	University of Dundee
A12480	University of Bath
A13480	Imperial College London
A13510	Royal Holloway University of London
A13520	University College London
A13620	University of Manchester Jodrell Bank Observatory
A14580	University of Lincoln
A14750	UCL Mullard Space Science Laboratory
A14760	University of Leicester
A14980	Queen Mary University of London
A15390	The Open University
A15450	Cardiff University
A15790	City University London
A15850	Nottingham Trent University
A16000	Coventry University
A16050	Cranfield University
A16540	University College London, Stanmore
A16580	University of Chester
A35030	Sheffield Hallam University
A35080	University of Manchester
A35111	University of Sussex
A35180	University of Nottingham
A35200	University of Aberdeen
A35250	University of Westminster
A35330	Newcastle University
A35410	University of Hull
A35440	University of Essex
A35470	University of Sheffield
A35520	Northumbria University
A35630	University of Kent
A35780	University of Cambridge
A36000	University of Bristol
A36090	University of Ulster
A36120	University of Strathclyde
A36280	Brunel University
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A36342	Liverpool John Moores University
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A37870	Swansea University
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A38040	Oxford Brookes University
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A38810	University of York
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A39450	Aston University
A39650	University of Salford
R00050	STFC Rutherford Appleton Laboratory
R20600	STFC Daresbury Laboratory
R20950	Diamond Light Source
R22030	STFC UK Astronomy Technology Centre
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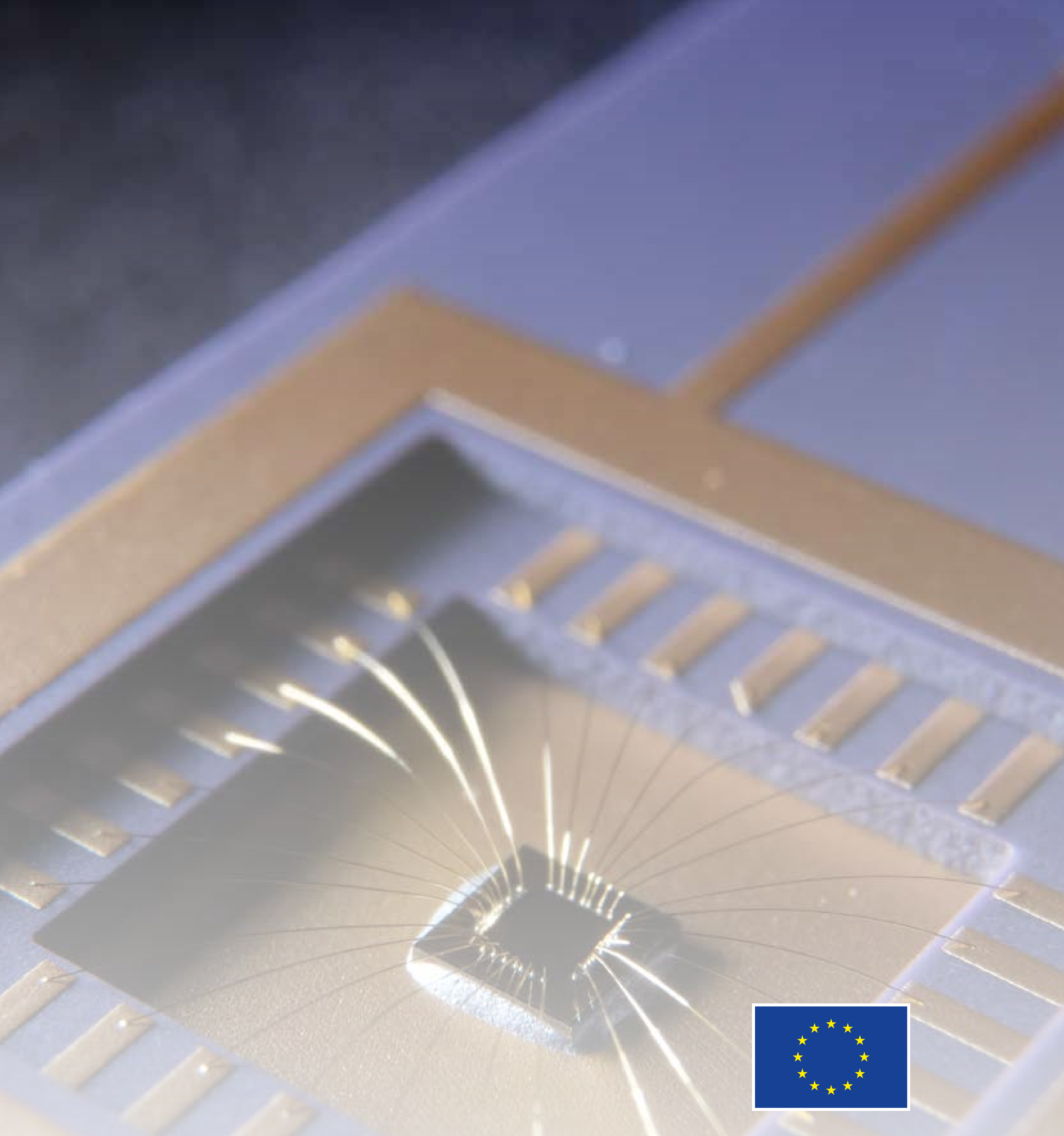

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EUROPRACTICE

All information for fabrication support, MPW run schedules and prices is available on our Technology & Fabrication website
www.europractice-ic.com

Design tools are available to Academic Institutions and publicly funded Research Laboratories in the EMEA region. More information can be obtained on our Design Tool & Training website
www.europractice.stfc.ac.uk

For more information, please contact one of our EUROPRACTICE service centers.

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