

# TSMC TECHNOLOGY OPTIONS

## Options for mini@sic runs

Options mini@sic Runs	IO	Core	Remarks
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	3.3V	1.8V	Low noise IO device not supported
TSMC 0.18 CMOS High Voltage BCD Gen II	5V	1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5V	Deep trench not supported
TSMC 65nm CMOS Logic or Mixed-Signal/RF, Low Power	2.5V (1.8UD, 3.3OD)	1.2V	
TSMC 40nm CMOS Mixed-Signal/RF, Low Power	2.5V (1.8UD, 3.3OD)	1.1V	Triple gate oxide not supported
TSMC 28nm CMOS RF HPC (+)	1.8V	0.9V	

**Important note:** The metal scheme is free to choose from the list below to ensure all verification and extraction (RC) decks are available.

## Metal stacks

Technology	Metalization	Topmetal Mz/Mn	Topmetal Mu
<b>0.18 G</b>	4M	/	lp4m_2x1u_mim_40k
	5M	lp5m_3x1n	lp5m_3x1u_mim_20k
	6M	lp6m_4x1n	lp6m_4x1u_mim_20k
			lp6m_4x1u_mim_40k
<b>65 LP</b>	6M	lp6m_4x1z_mim_alrdl	lp6m_3x1z1u_mim_alrdl
			lp6m_4x1u_mim_alrdl
	7M	lp7m_4x2z_mim_alrdl	lp7m_4x1z1u_mim_alrdl
			lp7m_4x1z1u_mim_ut-alrdl
	8M	/	lp7m_5x1z_alrdl
			lp7m_5x1u_alrdl
9M	lp9m_6x2z_mim_alrdl	lp9m_6x1z1u_mim_alrdl	
<b>40 LP</b>	6M	lp6m_3x2z_alrdl	lp9m_6x1z1u_mim_ut-alrdl
			/
	7M	lp7m_4x2z_alrdl	lp6m_4x1z_alrdl
			lp7m_4x1z1u_alrdl
			lp7m_4x1z1u_ut-alrdl
			lp7m_5x1z_alrdl
	8M	lp8m_5x2z_alrdl	lp8m_5x1z1u_alrdl
			lp8m_5x1z1u_ut-alrdl
			lp8m_6x1z_alrdl
	9M	lp9m_6x2z_alrdl	/
lp9m_6x2z_ut-alrdl			
lp9m_7x1z_alrdl			
10M	lp10m_7x2z_alrdl	lp10m_7x1z1u_alrdl	
<b>28 HPC</b>	8M	/	lp8m_5x1z1u_ut-alrdl
<b>28 HPC+ (use MMWAVE PDK)</b>	7M	lp7m_4x1y1z_alrdl	/
	8M	lp8m_5x2r_alrdl	lp8m_5x1z1u_ut-alrdl
			lp8m_5x2r_ut-alrdl
9M	/	lp9m_5x1y1z1u_ut-alrdl	

**Important note:** alrdl = 14kA, ut-alrdl = 28kA