TSMC TECHNOLOGY OPTIONS

Options for mini@sic runs

Options mini@sic Runs	IO	Core	Remarks
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	3.3V	1.8V	Low noise IO device not supported
TSMC 0.18 CMOS High Voltage BCD Gen II	5V	1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5V	Deep trench not supported
TSMC 65nm CMOS Mixed-Signal/RF, Low Power	2.5V (1.8UD, 3.3OD)	1.2V	
TSMC 40nm CMOS Mixed-Signal/RF, Low Power	2.5V (1.8UD, 3.3OD)	1.1V	Triple gate oxide not supported
TSMC 28nm CMOS RF HPC (+)	1.8V	0.9V	

Important note: The metal scheme is free to choose from the list below to ensure all verification and extraction (RC) decks are available.

Metal stacks

Technology	Metalization	Topmetal Mz/Mn	Topmetal Mu
0.18 G	4M	/	1p4m_2x1u_mim_40k
	5M	1p5m_3x1n	1p5m_3x1u_mim_20k
	6M	1p6m_4x1n	1p6m_4x1u_mim_20k
			1p6m_4x1u_mim_40k
65 LP	6M	1p6m_4x1z_mim_alrdl	1p6m_3x1z1u_mim_alrdl
			1p6m_4x1u_mim_alrdl
	7M	1p7m_4x2z_mim_alrdl	1p7m_4x1z1u_mim_alrdl
		1p7m_5x1z_mim_alrdl	1p7m_4x1z1u_mim_ut-alrdl
			1p7m_5x1u_alrdl
	8M	/	
	9M	1p9m_6x2z_mim_alrdl	1p9m_6x1z1u_mim_alrdl
			1p9m_6x1z1u_mim_ut-alrdl
40 LP	6M	1p6m_3x2z_alrdl	/
		1p6m_4x1z_alrdl	
	7M	1p7m_4x2z_alrdl	1p7m_4x1z1u_alrdl
		1p7m_5x1z_alrdl	1p7m_4x1z1u_ut-alrdl
	8M	1p8m_5x2z_alrdl	1p8m_5x1z1u_alrdl
		1p8m_5x2z_ut-alrdl	1p8m_5x1z1u_ut-alrdl
		1p8m_6x1z_alrdl	
	9M	1p9m_6x2z_alrdl	/
		1p9m_6x2z_ut-alrdl	
		1p9m_7x1z_alrdl	
	10M	1p10m_7x2z_alrdl	1p10m_7x1z1u_alrdl
28 HPC	8M	/	1p8m_5x1z1u_ut-alrdl
28 HPC+ (use MMWAVE PDK)	7M	1p7m_4x1y1z_alrdl	/
	8M	1p8m_5x2r_alrdl	1p8m_5x1z1u_ut-alrdl
		1p8m_5x2r_ut-alrdl	
	9M	/	1p9m_5x1y1z1u_ut-alrdl

Important note: alrdl = 14kA, ut-alrdl = 28kA