

TSMC TECHNOLOGY OPTIONS

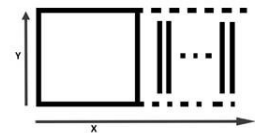
Common flow for 28 nm and 65 nm mini@sic

We see an increased interest in the TSMC 28 nm and 65 nm mini@sic. To optimise the number of designs on the mini@sic runs, we have defined a **common process flow** shown below. Supporting different process flows for all customer designs is not possible.

If you are planning to use any different process flow than shown in the two tables below, please take into account that **your design may end up on the waiting list**, and in the worst case, it may be postponed to the next mini@sic run.

Recommended 28 nm mini@sic options

| | |
|------------------------------|---|
| Metal Scheme | 9M_5X1Y1ZIU UT-ALRDL |
| Flip-Chip/bumping | Not supported in the common flow. Please contact eptsmc@imec.be . |
| Allowed devices | (1) ultra low Vt = {VTUL_N OR VTUL_P} (2) low Vt = {VTL_N OR VTL_P} (3) high Vt = {VTH_N OR VTH_P} (4) ultra high Vt = {UHVT_N OR UHVT_P} Standard devices are by default allowed Contact eptsmc@imec.be if other Vt's are needed. |
| SRAM/ ULL SRAM | Not supported in the common flow. Please contact eptsmc@imec.be . |
| AP thickness | 28kÅ |
| Backlapping thickness | 11 mils |
| Chip size | The height of the layout (Y-dimension) should be fixed: 1mm, 1.5mm, 2 mm or 2.5mm. The X-dimension of the layout is not fixed (minimum 1mm). |

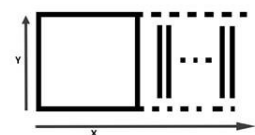


Important note:

Always use the T-N28-CR-SP-029 (mmWave ULL) PDK with flavor RF HPC+ 0.9/1.8V.
Sub-dicing of multiple sub-chips is not possible.

Recommended 65 nm mini@sic options

| | |
|------------------------------|---|
| Metal Scheme | 1p9m_6x1z1u_MIM_APRDL |
| Flip-Chip/bumping | Not supported in the common flow. Please contact eptsmc@imec.be . |
| AP thickness | 14kÅ |
| MIM Value | 2fF/um ² |
| Backlapping thickness | 11 mils |
| Chip size | The height of the layout (Y-dimension) should be fixed: 1mm, 1.5mm or 2 mm. The X-dimension of the layout is not fixed (minimum 1mm). |



Important note:

No deviation possible from MS/RF LP flavor with 1.2V core and 2.5V IO.
Sub-dicing of multiple sub-chips is not possible.

Full list of mini@sic options

| Options mini@sic Runs | IO | Core | Remarks |
|---|------------------------|------|--|
| TSMC 0.13µm CMOS High Voltage Mixed Signal based, Low Power, BCD Plus Triple Gate 1.5/3.3/5/10/12/16/20/24/28/36/VG1.5/3.3/5VV | 3.3/5V | 1.5V | 0.13µm BCD/BCD+ MiM Capacitor 1.0ff/µm ² : Only offered at FAB12 |
| TSMC 65nm CMOS Mixed-Signal/RF, Low Power | 2.5V (1.8UD, 3.3OD) | 1.2V | |
| TSMC 40nm CMOS Mixed-Signal/RF, Low Power | 2.5V (1.8UD, 3.3OD) | 1.1V | Triple gate oxide not supported |
| TSMC 28nm CMOS RF HPC (+) | 1.8V | 0.9V | |
| TSMC 16nm RF FinFET Compact | 1.8V | 0.8V | |

Important note:

Contact epstsmc@imec.be if any of the following options are used: Bumping, MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS. The metal scheme can be chosen from the list below to ensure all verification and extraction (RC) decks are available.

Metal stacks

| Technology | Metalization | Topmetal Mz/Mn | Topmetal Mu | |
|---------------------------------|------------------|--------------------------|-----------------------------|--------------------------|
| 0.13µm HV BCD Plus | 6M | lp6m_4x1n_alrdl | / | |
| 65 LP | 6M | lp6m_4x1z_mim_alrdl | lp6m_3x1z1u_mim_alrdl | |
| | | | lp6m_4x1u_mim_alrdl | |
| | | 7M | lp7m_4x2z_mim_alrdl | lp7m_4x1z1u_mim_alrdl |
| | 8M | | lp7m_5x1z_mim_alrdl | lp7m_4x1z1u_mim_ut-alrdl |
| | | | | lp7m_5x1u_alrdl |
| | | 9M | lp9m_6x2z_mim_alrdl | lp9m_6x1z1u_mim_alrdl |
| | | lp9m_6x1z1u_mim_ut-alrdl | | |
| 40 LP | 6M | lp6m_3x2z_alrdl | / | |
| | | | lp6m_4x1z_alrdl | |
| | 7M | lp7m_4x2z_alrdl | lp7m_4x1z1u_alrdl | |
| | | | lp7m_5x1z_alrdl | lp7m_4x1z1u_ut-alrdl |
| | | 8M | lp8m_5x2z_alrdl | lp8m_5x1z1u_alrdl |
| | 9M | | lp8m_5x2z_ut-alrdl | lp8m_5x1z1u_ut-alrdl |
| | | | lp8m_6x1z_alrdl | |
| | | | lp9m_6x2z_alrdl | / |
| | | | lp9m_6x2z_ut-alrdl | |
| | | | lp9m_7x1z_alrdl | |
| 10M | lp10m_7x2z_alrdl | lp10m_7x1z1u_alrdl | | |
| 28 HPC+ (use MMWAVE PDK) | 7M | lp7m_4x1y1z_alrdl | / | |
| | 8M | lp8m_5x2r_alrdl | lp8m_5x1z1u_ut-alrdl | |
| | | | lp8m_5x2r_ut-alrdl | |
| 9M | / | lp9m_5x1y1z1u_ut-alrdl | | |
| 16nm RF FinFET Compact | 9M | / | IP9M_2XAIXD3XEIZIU_UT AIRDL | |

Important note: alrdl = 14kA, ut-alrdl = 28kA