Tyndall National Institute
Institiúid Náisiúnta

Photonic, Electronics, MEMS Packaging and System Integration Design Rules

Photonic Packaging & System Integration Group

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EUROPRACTICE

Contents

1 Introduction

Packaging and system integration covers the optical, electronic, mechanical and thermal coupling of photonic integrated circuits (PICs) to the outside world. The advanced manufacturing processes required for packaging covers areas such as (1) photonics and electronics co-packaging and (2) MEMS and integrated system co-packaging. The challenges associated with the packaging of photonic devices. particularly co-packaging, is often underestimated and remains technically challenging due to the variety and complexity of the technologies involved, combined with the lack of standards available to PIC designers. This significantly impacts the cost of assembling prototype photonic packages as well as how this is scaled to volume manufacturing. An overview of some of the main packaging processes available to users is shown in Figure 1.

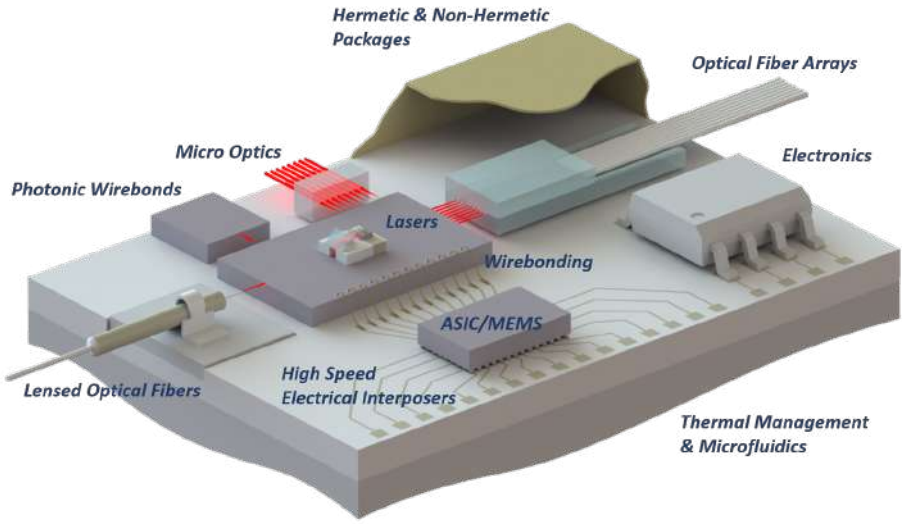

Figure 1: Overview of some of the typical packaging processes available to users, including: fibre array attach, hybrid integration, micro-optics assembly, wire bonding, electrical assembly, ASIC and MEMS integration.

To ensure that PICs, EICs (ASICs) and MEMS can be co-packaged efficiently and reproducibly, it is important to standardise their layout so that generic packages and packaging processes can be utilised. To aid with this, the Photonic Packaging Group (`www.tyndall.ie/packaging`) at Tyndall have developed a series of photonic packaging design rules (PDRs) that cover some of the most widely used packaging and assembly technologies. These design rules specify the acceptable dimensions and locations of optical and electronic input or output ports on a PIC, with respect to the physical footprint of the PIC-die.

In this document, we present these PDRs and review some of the main technology challenges associated with photonic packaging in general. The Photonic Packaging Group at Tyndall is constantly working to develop technologies that improve the efficiency of optical, electronic packaging and system integration processes, while also lowering the cost. Some advanced

manufacturing solutions currently in development may not yet be mature enough to offer as standard processes, but we are open to offering them to companies and research partners, in terms of collaborative development projects. In the final section of this document, we present a short overview of some of the different ways users can access PIC packaging technologies across Europe depending on their specific requirements and Technology Readiness Levels (TRL). This includes information on how to contact EUROPRACTICE, ACTPHAST and PIXAPP for packaging and assembly solutions.

2 General PIC Layout

To facilitate clear discussions with the user, we use a compass-coordinate system to unambiguously label each side of the PIC-die. We can provide packaging solutions to all standard PIC-dies, including the miniPhotonic blocks from IMEC and CEA-Leti, provided the PDRs are correctly followed. In all cases, we recommended to review your PIC design with your chosen packaging partner before submission to a foundry.

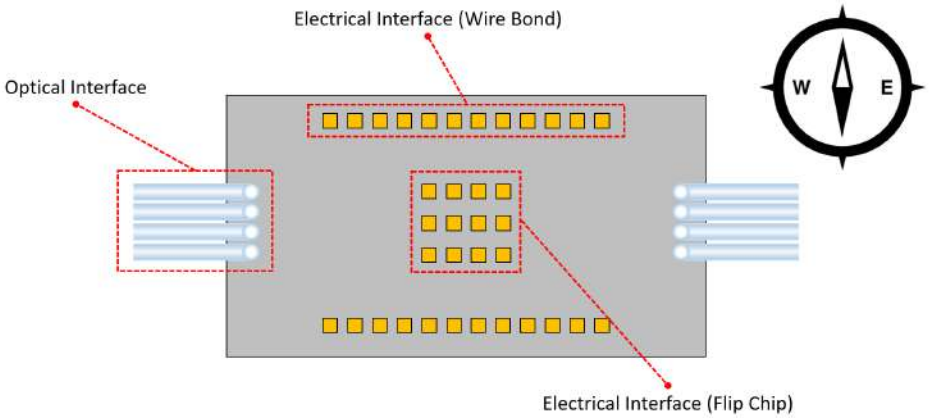

Figure 2: General PIC design and layout guidelines. Allows compatibility with standard photonic packaging and assembly processes.

To avail of the packaging and assembly processes at Tyndall, we recommend that users design the optical and electrical interface of their PIC according to layout outlined in Figure 2. This layout provides the user with the option of using generic packaging solutions that can be more cost effective with reduced process development times. Optical interfaces are typically where an optical fibre is coupled to the PIC via an edge coupler or grating coupler. Electrical interfaces are where wire bonds or a BGA connect the PIC to an external carrier. An example of PIC that has been well-designed for packaging is shown in Figure 3, where the optical, electrical (DC and RF) interfaces are clearly separated.

For optimised packaging, one side of the PIC should be designated for the optical interface (typically the West-side). If more than one optical interface is required, this should be at the opposite side of the PIC (typically the East-side) to facilitate parallel optical alignment using standard packaging equipment. More detailed design guidelines for the optical interface will

be described in Section 3, including the concept of the optical "shunt" or "loop-back" which is important for fast and efficient optical alignment.

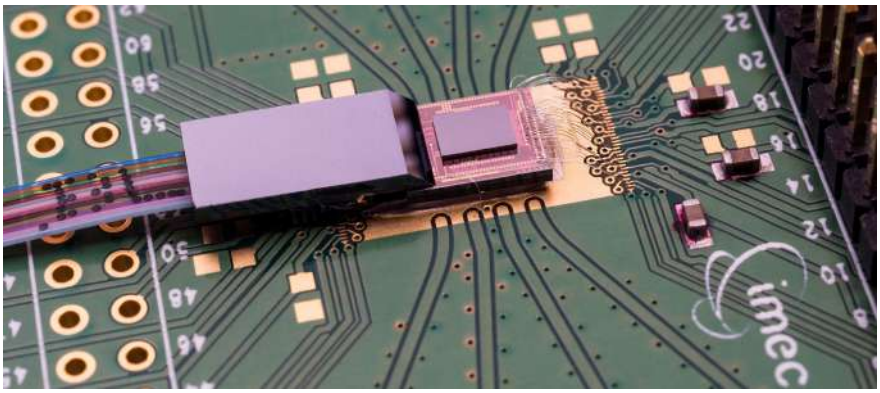

Figure 3: Example of a well designed package that facilitates assembly of a photonic IC with integrated ASIC on an electrical carrier using standard assembly processes.

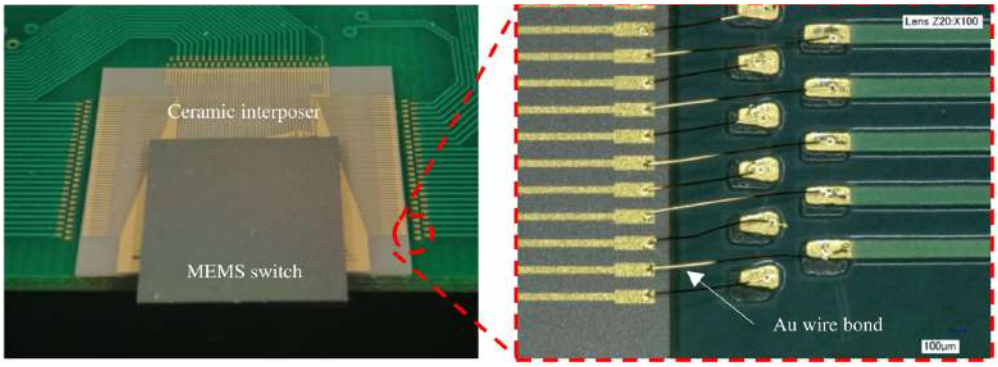

Figure 4: Example of a well designed package that facilitates assembly of a MEMS chip on an electrical carrier using standard assembly processes.

Electronic connections between the PIC and the outside world are typically made by wire-bonding to a PCB. To ensure reproducible and reliable wire-bonding, the location and pitch of the bond-pads on the PIC must be controlled. Specific design guidelines will be detailed in Section 4. In general, we recommend that optical and electronic assembly processes should not be made from the same side of the PIC-die. By default, bond-pads are located along the North- and South-side edges of the PIC. If it is not being used for optical-coupling, then bond-pads can also be placed along the East-side edge of the PIC-die.

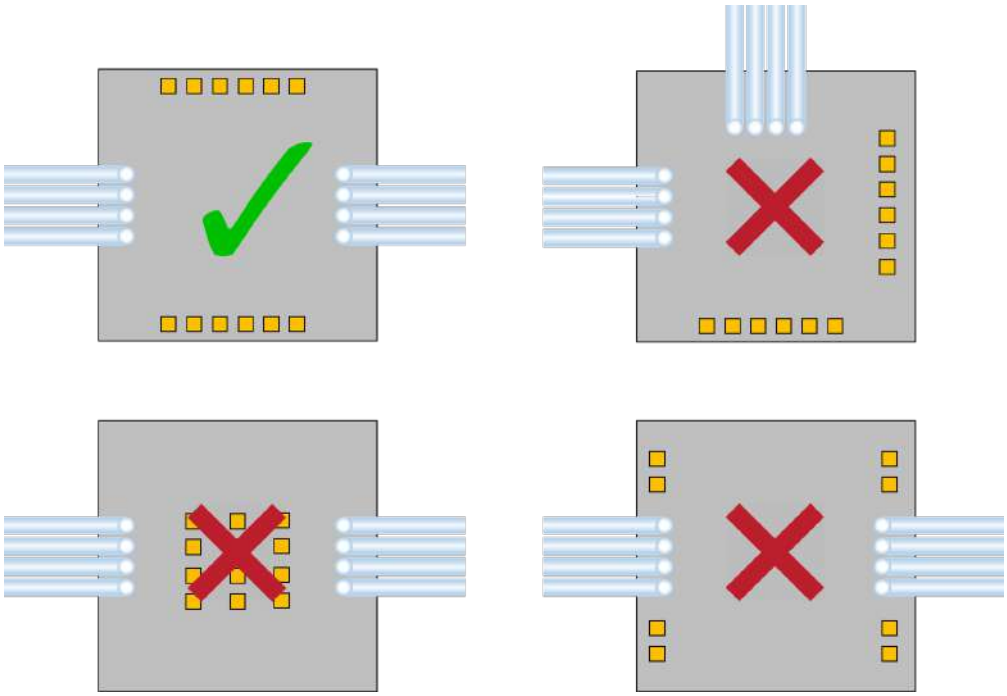

Figure 5: Examples of some best-practice rules for designing a PIC. Adhering to these rules allows compatibility with standard packaging and assembly processes.

When a PIC design calls for DC and RF electrical-connections, we recommend locating all DC bond pads along one edge of the PIC-die (i.e. along the North-side), and all RF bond-pads along the other edge (i.e. along the South-side). Regardless of type, bond-pad arrays should be centered with respect to the PIC, see Figure 2. Some of these optical and electrical design rules are summarised graphically in Figure 5. In the sections that follow, we will look at specific design rules for electrical and optical packaging of PICs in more detail.

3 Optical Packaging

The Photonic Packaging Group at Tyndall works to offer a flexible range of optical-coupling solutions for a wide variety of PICs and applications. These PDRs are written primarily aimed at 1550nm and 1310nm packaging solutions, but can also be applied to other wavelength ranges. In general, we can package single-fiber or fiber-arrays; single-mode fibers (SMFs) or polarization maintaining fibers (PMFs); and work with either grating-coupler or edge-coupler schemes. The more relaxed optical alignment tolerances of grating-couplers, compared to edge-couplers, often makes them the preferred choice for optically-packaging PICs. However, for optical-packaging of edge-emitting laser-chips, or optically-broadband / polarization-agnostic PICs, edge-coupling can be the better choice. Whatever coupler option is chosen, we recommend to carefully follow PDRs, to ensure that their PIC can be optically packaged.

3.1 Edge Couplers

Edge coupling offers low insertion-loss (IL), large spectral bandwidth (BW), and low-sensitivity to polarization. It is one of the more convenient means of getting light from an edge emitting laser or PIC waveguide into an optical fiber and is well established for the commercial packaging of laser diodes (LD). The alignment tolerances for edge-coupling are typically more stringent than for grating-coupling.

3.1.1 Single Fiber

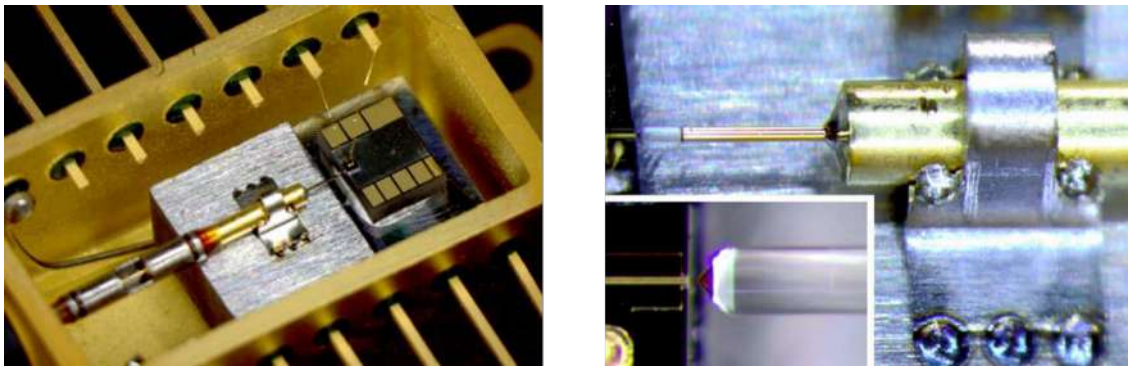

Figure 6: Example of laser welding within a photonic package.

For single-fiber edge-coupling to a laser-chip, we typically use a lensed optical fibre (focal length $10\mu m$) which is mounted in a metallic ferrule. The complete metallised assembly is locked into the optimum alignment position by means of laser-welding (to a Kovar Butterfly-package). This process is commonly referred to as "fiber pigtailing" and is a critical step of manufacturing of LD modules. This is accomplished with the optical alignment and laser welding process. The welding process produces a robust attachment fixture and is commonly

used for high-end photonic devices used in extremely harsh environments (eg. space or submarine applications). An example of the laser welding packaging process is shown in Figure 6.

For single-fiber edge-coupling to a PIC, we offer two standard options:

- Optical-packaging with a lensed fiber to an inverted-taper on the PIC
- Optical-packaging with a flat fiber to a $10\mu m$ mode-converter on the PIC

It is the responsibility of the user to ensure that their edge-coupler structure is sufficiently close to the edge of the PIC-die to allow for fiber access.

3.1.2 Fiber Array

Edge coupling to PICs typically requires a mode-adapter to match the PIC mode field diameter (MFD) with that of the edge coupled fiber. For many applications, multiple fiber-connections to the same PIC are needed. Instead of sequentially aligning several individual fibers, the solution is to use a fiber-array. The tight alignment tolerances of edge coupling make it challenging to couple fiber-arrays to PICs, unless the waveguide MFD can match that of the fiber. Advancements in photonic packaging technology has seen fiber arrays using ultra high numerical aperture (UHNA) fibers being used for coupling to large channel count Si and InP PICs with MFDs of $3\mu m$. These fibers provide good mode matching to small MFD PICs and can also be spliced to SMF28 fibre with minimal excess losses. For PICs with $10\mu m$ MFD waveguides, standard fibre arrays can provide low loss coupling using standard packaging processes. For illustrative purposes, a package showing the alignment of such a fibre array to a Si PIC is shown in Figure 7.

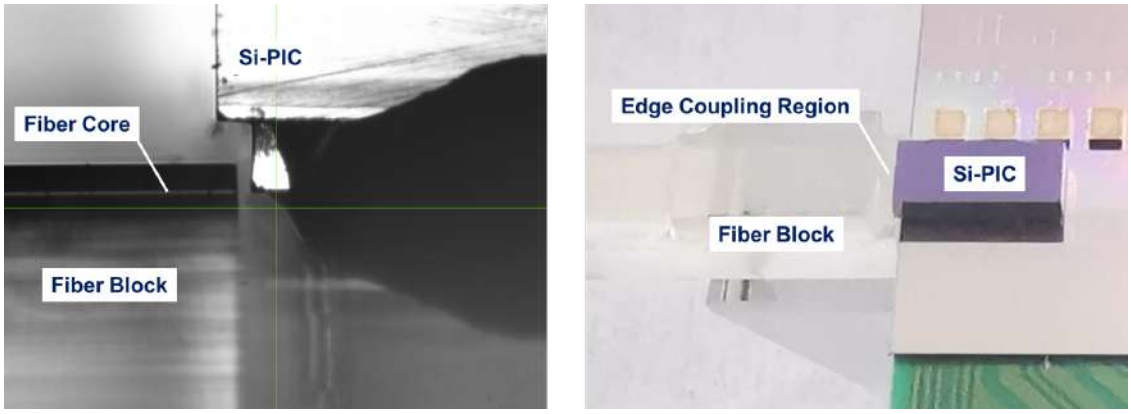

Figure 7: Coupling of a fibre array to the edge couplers on a Silicon PIC. (left) Close-up view of the fibre being aligned to the waveguides. (right) Expanded view of the fibre and PIC system.

In fibre-array edge coupling, multiple fibre-channels are aligned to multiple edge-couplers on the PIC at the same time. We recommend to use active alignment through a series of "optical-shunts" to align the fiber to pairs of looped waveguides at each side of the optical

interface. Given the high concentricity of the inner-cores of the fibres in the array ($<500nm$), this approach ensures that all intermediate fibre-channels are aligned to their corresponding edge-couplers. A typical implementation of such shunts on a PIC is shown in Figure 8.

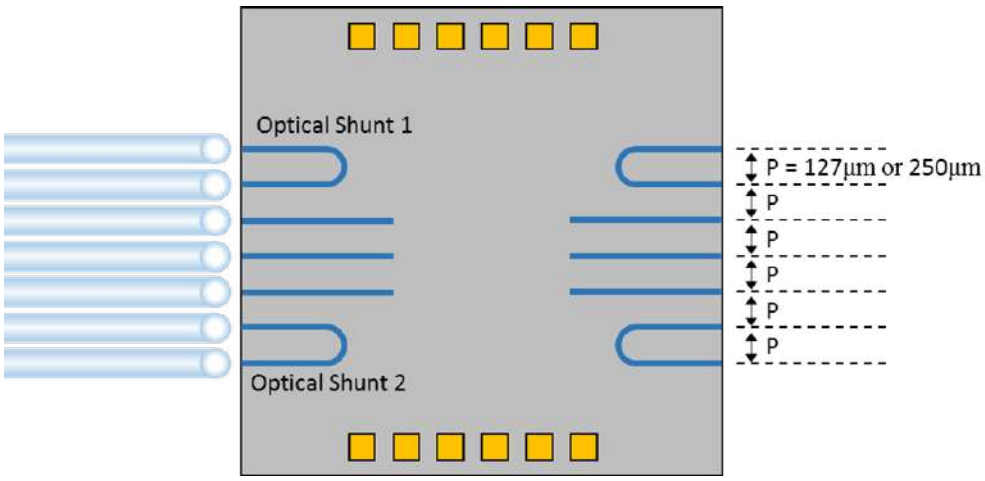

Figure 8: Overview of the "optical-shunt" concept that is used to assist with fibre array alignment within a photonic package.

The pitch of the edge-coupler array on the PIC must be exactly $250\mu m$ or $127\mu m$, to match the edge coupled arrays offered by Tyndall - see Figure 8. Since the first and last pairs of channels of the fibre-array and waveguide edge array are used for the optical-shunts, users requiring N channels for the operation of their PIC must choose a fibre-array with at least $N + 4$ channels. If two fibre-arrays are needed to package a PIC, they must be arranged on opposite sides of the PIC (e.g. West-side & East-side in some cases). Angled fibre arrays can also be accommodated for angled waveguide outputs. However, this is non-standard and should be discussed directly with Tyndall.

3.2 Grating Couplers

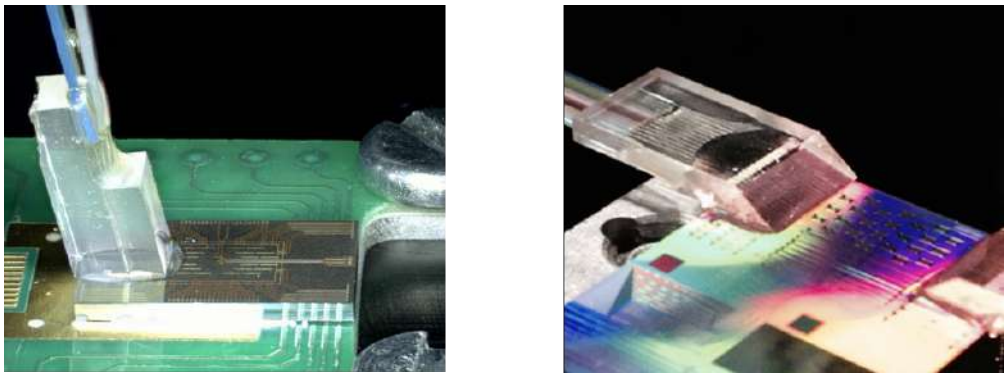

Figure 9: Examples of fibre arrays packaged to grating couplers on PICs. (left) Standard vertical coupling. (right) Quasi-planar coupling.

The alternative to edge-coupling, and more widely adopted solution for coupling light to and from an Si-PIC, is grating coupling. Examples of fibre coupling to PIC grating couplers is shown in Figure 9. For a typical grating coupler, miss-alignment of the fiber by $2.5\mu m$ from its optimum position results in a decrease in power coupling of about 1dB. Although this alignment tolerance is not so relaxed as to allow for passive alignment of the fiber with respect to the Si-PIC grating coupler, it significantly simplifies the process of active alignment, compared to edge-coupling schemes.

For optimum coupling efficiency, the fiber-mode should be near-normally incident on the grating-coupler. For example, the ISIPP50G PDK from *imec* indicates that their grating couplers are designed and tested for fibers with perpendicular (0° cleave) facets oriented at 10° in air. However, if the fiber itself is optically packaged at near-normal incidence, i.e. in the pigtail geometry, then the overall device becomes bulky and delicate.

To address this issue, a quasi-planar coupling (QPC) approach has been developed, in which the fiber lies on the surface of the Si-PIC, with a 40° polished facet providing a total internal reflection (TIR) condition the directs the fiber-mode onto the grating-coupler at the correct angle of 10° when packaged using an index matched epoxy. See Figure 9. The quasi-planar approach has an easily manageable 1dB roll tolerance of ±2.5°, in addition to the $\pm 2.5\mu m$ 1dB lateral alignment tolerance and offers an insertion loss that is on par with that of standard pigtail coupling to grating couplers.

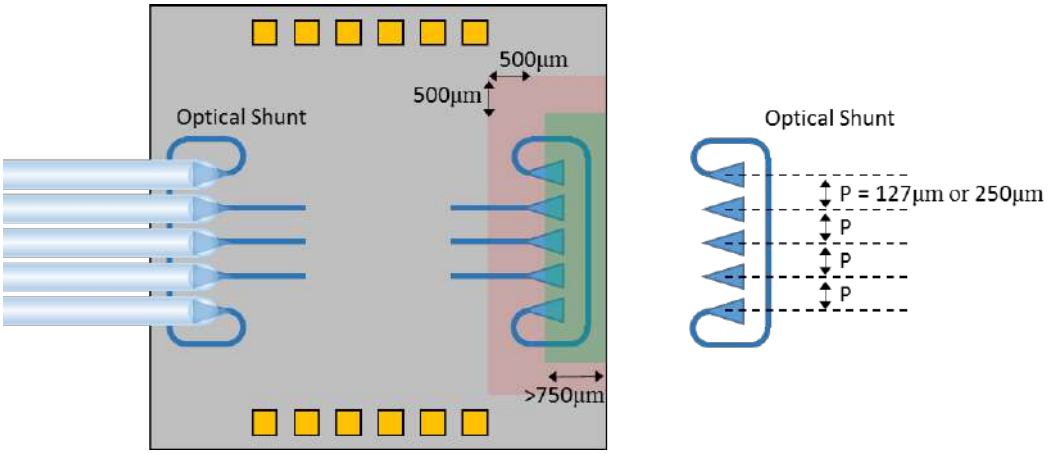

Figure 10: Overview of the "optical-shunt" concept that is used to assist with fibre array alignment within a photonic package.

In fibre-array QPC (and near vertical coupling), multiple fibre-channels are aligned to multiple grating-couplers on the PIC at the same time. We recommend to use active alignment through an "optical-shunt" to align the first and last channels of the fibre-array with the first and last channels in the grating-array. Given the high concentricity of the inner-cores of the fibres in the array ($<500nm$), this approach ensures that all intermediate fibre-channels are aligned to their corresponding grating-couplers. A typical implementation of such shunts on

a PIC is shown in Figure 10.
To facilitate shunt alignment and good mechanical bonding between the fibre-array and PIC, we require that the grating-coupler array be located no closer than $750\mu m$ from the edge of the PIC, and that the array runs parallel to edge of the PIC. Additionally, we suggest to leave a $500\mu m$ exclusion zone around the 5mm footprint of the fibre-array, to allow for epoxy flow. These design rules are illustrated in Figure 10.

The pitch of the grating-coupler array on the PIC must be exactly $250\mu m$ or $127\mu m$, to match the QPC arrays offered by Tyndall - see Figure 10. Since the first and last channel of the fibre-array and grating-array are used for the optical-shunt, users requiring N channels for the operation of their PIC must choose a fibre-array with at least $N+2$ channels. If two fibre-arrays are needed to package a PIC, they must be arranged on opposite sides of the PIC (e.g. West-side & East-side).

3.3 Optical Design Rule Summary

A summary of some of the main design rules and specifications for optical photonic packaging are provided in Table 1. Please note that these design rules are recommendations based on current standard processes. If you require packaging outside the scope of these rules, please contact the Photonic Packaging Group at Tyndall for information on the current state-of-the-art and what custom options are available.

Table 1: Optical packaging design rules.

Optical Packaging Design Rules	
Platforms	SOI, SiN, InP
Typical Coupler Mode Field Diameters (MFD)	$3.0\mu m$, $6.0\mu m$, $10.0\mu m$
Coupler Types	Grating or Edge Couplers
Fibre Options	SMF/PMF
Number of Optical Channels	1 - 64 (More on request)
Channel Pitch	$127\mu m$, $250\mu m$
Alignment Feedback	Optical Loopback (Shunt), Laser, PD

4 Electrical Packaging

Wire bonding is the most common method of providing an electrical connection from a PIC to a PCB within a package. The majority of packages assembled at Tyndall are manufactured using Au ball bonding (DC), with Ribbon or Wedge wire bonds used for high speed signals (RF). Examples of the different types of wire bond configurations are shown in Figure 11.

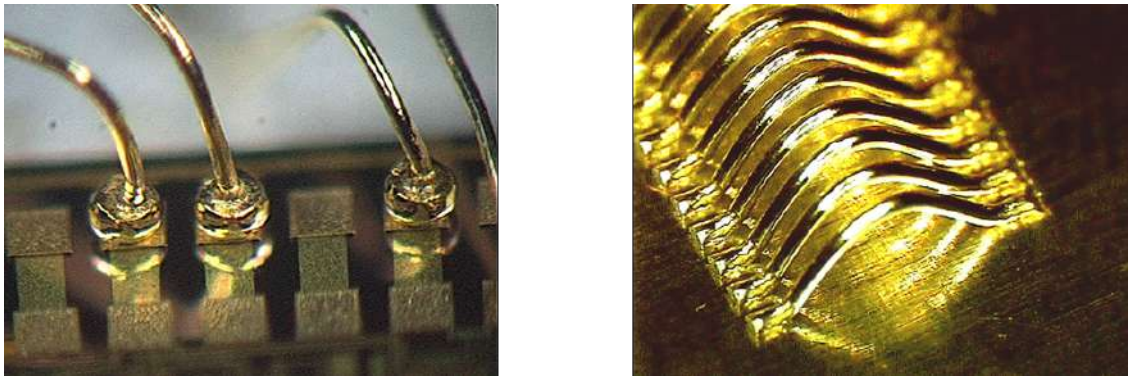

Figure 11: Examples of electrical wire bonds used in photonic packages. (left) Gold ball bond. (right) Ribbon or wedge bond.

Where there is a mechanical mismatch between the PIC and PCB bond pads, electrical interposers are used as intermediate structures to bridge them together. These can take the form of thin-film ceramics or Silicon ICs. For 2.5D and 3D integration, flip chip bonding of electrical ICs (or in some cases, PICs) is becoming popular due to its potential for package footprint reduction and improved electrical performance. The package shown in Figure 12 illustrates some of the key concepts of electrical packaging. In the sections that follow, we will briefly outline these technologies and describe some basic PDRs that should be followed for efficient electrical photonic packaging.

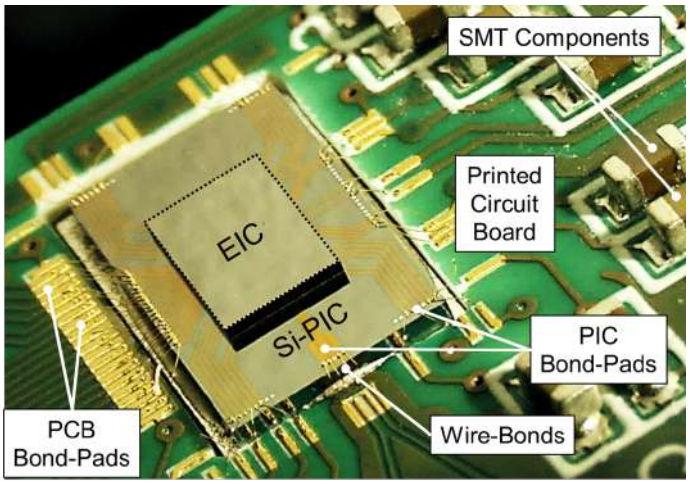

Figure 12: Overview of some key electrical features within a photonic package. Note: for clarity, fibre attach to PIC is not shown.

4.1 DC Electrical Connections

For standard ball bonding, DC bond-pads on a PIC should typically be at least $70\mu m \times 70\mu m$, and be separated by a pitch of at least $150\mu m$. We recommend against staggering bond-pads on the PIC due to the increased likelihood of shorting between adjacent wire-bonds. Smaller bond pad widths and pitches can typically be accommodated, particularly those defined as part of PDKs from main European foundries. In general, it is recommended to keep bonds as close to the chip edge as possible. This ensures that the wire bond length is kept as short as possible when connecting the PIC to a PCB or carrier. Additionally, it is recommended that bond-pads for electronic-coupling should be located along the North- and South-sides of the PIC-die, and centered with respect to the PIC-die. Some of these PDRs are summarised graphically in Figure 13. Information on the most appropriate choice of bond pad metallisation can be found in Table 2.

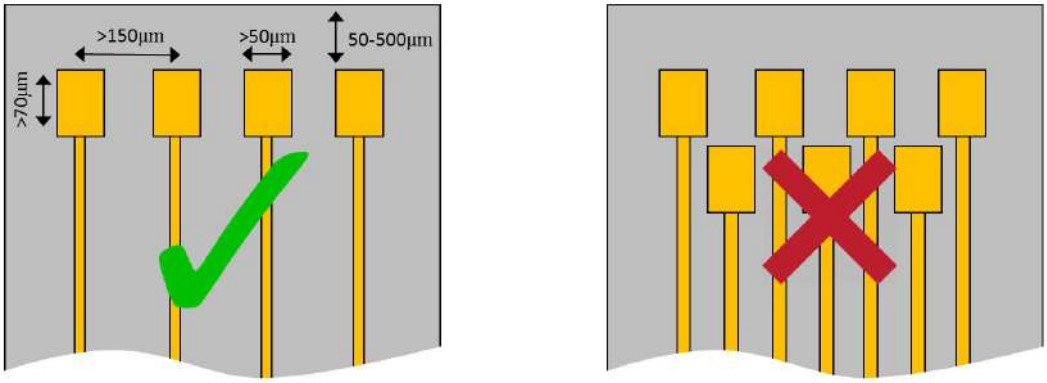

Figure 13: PIC bond design rules and best practice guidelines. Smaller pitches and sizes can be accommodated but may require non-standard processes.

4.2 RF Electrical Connections

The physical space on a PIC-die is relatively expensive when viewed as a cost per mm^2, so there is a need to keep the electrical contact pads on a PIC as small as possible to reduce the physical footprint. Compact DC bond pads and traces on a PIC can be designed to interface with standard PCB technology relatively easily, as shown in the previous section. However, for RF bond pads and traces on a PIC, there is an inherent mismatch with PCB technology due to the difference in dielectric constants of the materials involved.

This dimensional variation is illustrated in Figure 14. When wire bonding a PIC to a PCB in this configuration, it is critical that the wire bond length is kept as short as possible to reduce any parasitic losses. For PICs with single RF channels, this can usually be accomplished with a minimal impact on performance. For larger channel numbers, extra care must be taken to ensure the PIC and PCB can be physically connected together while maintaining impedance matching and minimising parasitic losses. As will be described in the following section, to solve the physical mismatch between a PIC and a PCB (or other electrical plat-

form, e.g. LTCC), electrical interposers are typically used. These interposers act as a bridge between the PIC and the PCB, allowing the electrical interfaces to be gradually matched over a chosen distance. Note: due to the wide variety of possible RF interfaces (PIC to PCB, glass, ceramic) it is difficult to provide detailed design rules for RF packaging. However, we list some general guidelines that may be useful in Table 3. It is recommended to see specific advice relating to the RF design of your PIC from your chosen packaging provider prior to PIC manufacture.

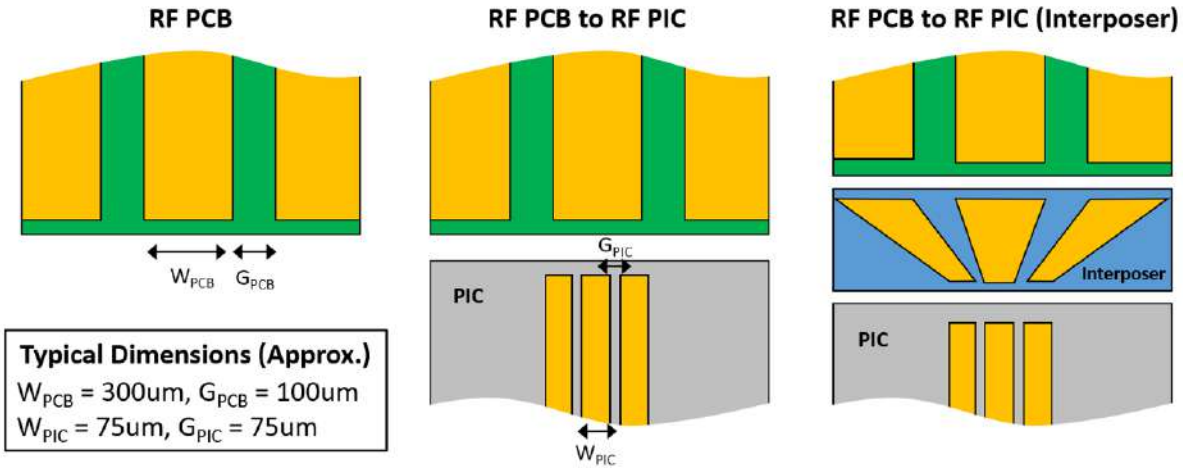

Figure 14: (left) Typical dimensions of a high-speed PCB. (middle) Mismatch between the physical dimensions of the RF lines on a PIC and high-speed PCB. (right) Electrical interposer are used to bridge the electro-mechanical mismatch between the PIC and PCB.

4.3 Electrical Interposers

As mentioned above and illustrated in Figure 14, interposers are typically used to bridge the electro-mechanical mismatch between the PIC and PCB bond dimensions for impedance matching. A variety of different interposer structures can be used depending on the specific application and RF requirements, such as glass, ceramic or an LTCC. A typical example of a ceramic interposer being used to interface 8 RF channels on a PIC to a PCB package is shown in Figure 15. The ceramic interposer is designed so that it's RF lines maintain a constant 50Ω impedance while moving from a size that matches the RF lines on the PCB to that of the PIC. Typically, these types of interposers are custom designed for particular applications.

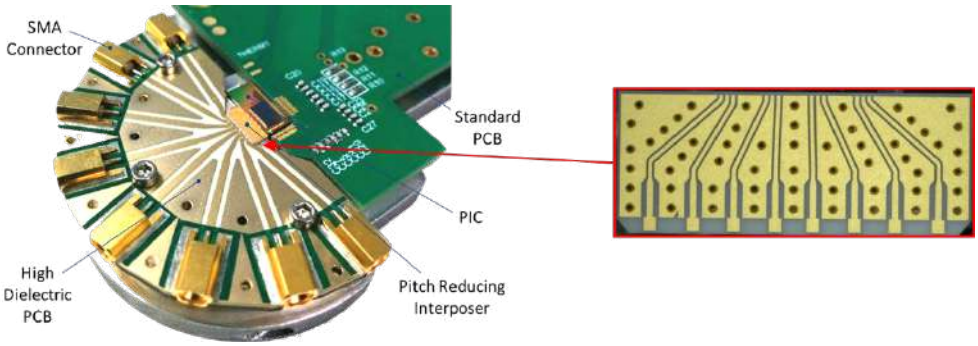

Figure 15: RF interposers are used to bridge the electro-mechanical mismatch between the PIC and PCB bond dimensions. This figure shows such an interposer being used to route 8 RF connections to a PIC.

For DC connections, interposers can also be used to facilitate the packaging of PICs with large numbers (i.e. 200+) of closely spaced electrical contacts which need to be fanned out towards a PCB. These type of interposers can include single level Silicon structures (8mm/3mm lines Spaces) or dual level glass interposers with $40\mu m$ vias. Examples of these structures are shown in Figure 16. These interposers are typically designed for use with flip chip bonding, which provides a convenient way of electrically interconnecting the PIC. Flip chip bonding will be described in the following section.

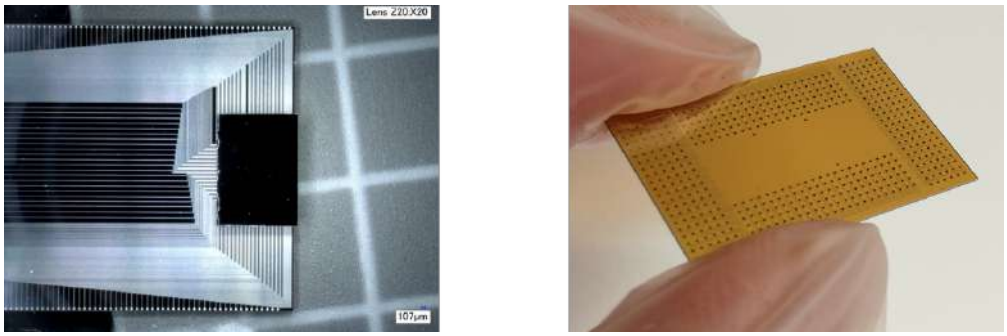

Figure 16: Interposers are used to fan-out electrical connections from a PIC to a PCB or other carrier. (left) Silicon interposer. (right) Glass interposer.

4.4 Metallisations

When any form of electrical packaging, it is critical to ensure that bond pad metallisation on the PIC is compatible with the chosen assembly process (wire bonding, flip chip bonding). Table 2 lists some of the preferred and acceptable metallisations depending on the specified process.

Table 2: PIC metallisations for compatibility with electrical packaging processes.

Process Type	Preferred Metal	Acceptable Metal
Wire Bonding (DC)	Au	Al
Wire Bonding (RF)	Au	Al
Flip Chip Bonding	Au, Copper Pillar Bump	Al (with Au Stud Bumps)

4.5 Electrical Design Rule Summary

A summary of some of the main design rules and specifications for electrical photonic packaging are provided in Table 3. Please note that these design rules are recommendations based on current standard processes. If you require packaging outside the scope of these rules, please contact the Photonic Packaging Group at Tyndall for information on the current state-of-the-art and what custom options are available.

Table 3: Electrical packaging design rules.

Electrical Packaging Design Rules		
Wire Bonding (DC)	Bond Pad Size	50μm × 50μm (minimum)
	Bond Pad Pitch	125μm (minimum)
	Max Channels	1 - 100
Wire Bonding (RF)	Bond Pad Size	50μm × 50μm (minimum)
	Bond Pad Pitch	150μm (minimum)
	Max Channels	4 - 8
Flip Chip Bonding (DC/RF)	Bond Pad Size	50μm × 50μm (minimum)
	Bond Pad Pitch	100μm (minimum)
	Max Size	1500μm × 1500μm
Interposer	Material	Ceramic, Silicon
	Trace Sizes	Silicon: 10μm Width, 10μm Gap
	Max Channels	1 - 1000

5 Micro-System Integration

Micro-system integration and packaging involves two key categories: device packaging, and system packaging. Device level involves connecting the device electrically and optically. It also includes powering, cooling and providing structural support to the device if necessary. The second type, referred to as system packaging, involves assembling the components together, usually through a common carrier on top or below of the device. It also includes interconnecting these components electrically or optically, and again providing power, cooling and mechanical support if necessary between the components.

5.1 Flip Chip Bonding

For high-speed RF photonic devices, the physical length of the electrical connections between the electronic-IC (EIC) and PIC should be minimized. Using our our PacTech Solder Bumper (SB2) and Finetech Flip Chip system, an EIC can be bonded onto a PIC (or vice versa) to reduce the electrical length. This approach can also be useful for PICs with large numbers of electrical connections, where the PIC is bonded to a carrier interposer to fan-out the electrical lines. The general process for flip chip bonding is outlined in Figure 17. The SB2 can rapidly apply $50\mu m$ solder-balls to an extended 2D array of Au-finished bond-pads on the PIC, which are then aligned with respect to their corresponding bond-pads on the EIC, using the flip-chip system. The EIC and PIC are then brought into contact, and electro-mechanically-bonded together by solder re-flow at 250°C. For solder-ball-bump and flip-chip packaging, the bond-pads on the PIC and EIC should both be a minimum of $50\mu m \times 50\mu m$ in size, and be separated by a pitch of at least $100\mu m$. The maximum size EIC which can be bonded in this manner is $1500\mu m \times 1500\mu m$.To ensure good adhesion of the solder ball to the bond-pad, the Au-thickness on the pads should be at least 500nm. If multiple EICs are integrated onto a common PIC (or carrier in general), the minimum spacing between the dies should be greater than $250\mu m$. An overview of these design rules are shown in Figure 17 and are also summarised in Table 3. Examples of flip chip bonding of ASICs to Si-PICs are shown in Figure 18.

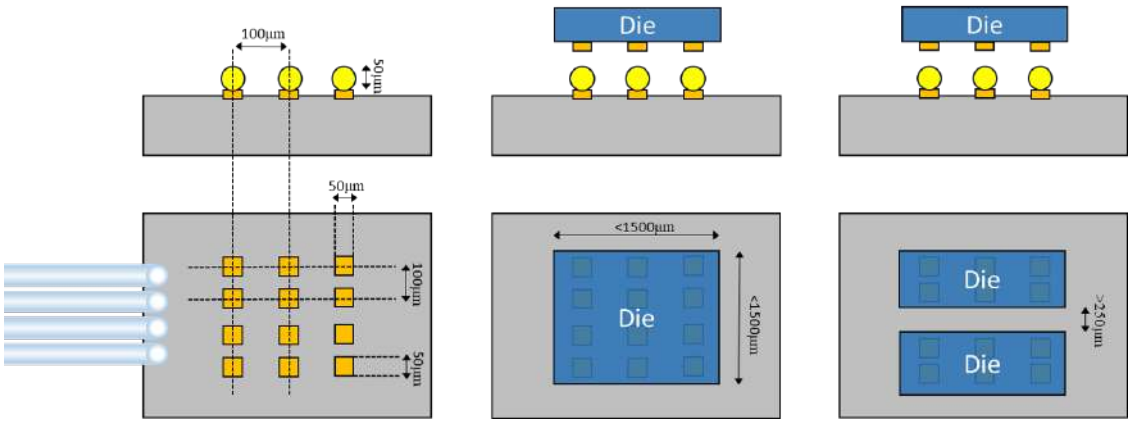

Figure 17: Summary of key design rules for flip-chip bonding of ASIC and MEMS dies. (left) Minimum bond size and pitch. (center) Maximum size die which can be bonded. (right) Minimum separation between adjacent dies when bonded to a common carrier.

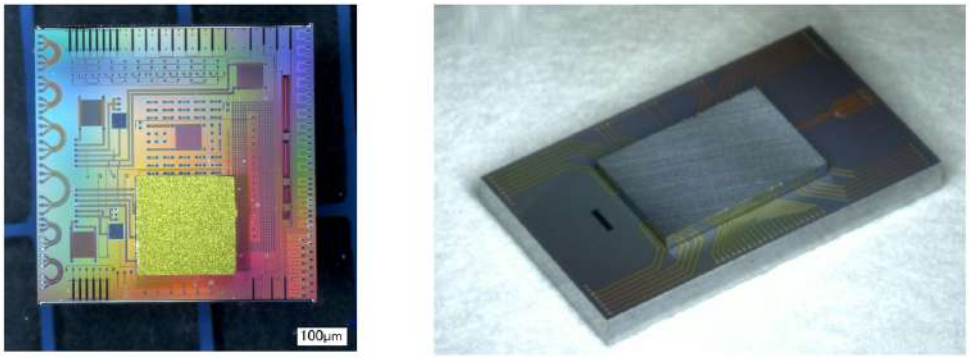

Figure 18: Examples of flip-chip bonding on Si-PICs.

5.2 Photonic, Electronic and MEMS Carriers

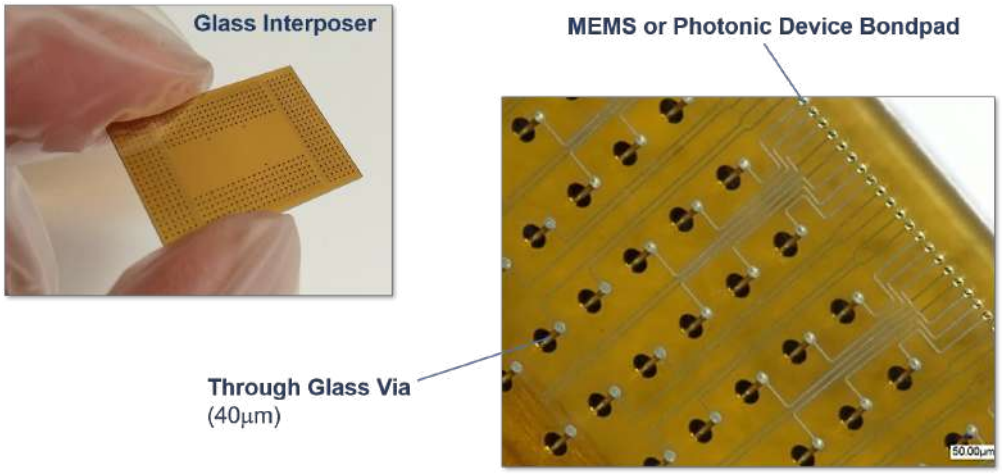

Figure 19: MEMS Carrier

5.3 Photonics and Electronics Co-Packaging

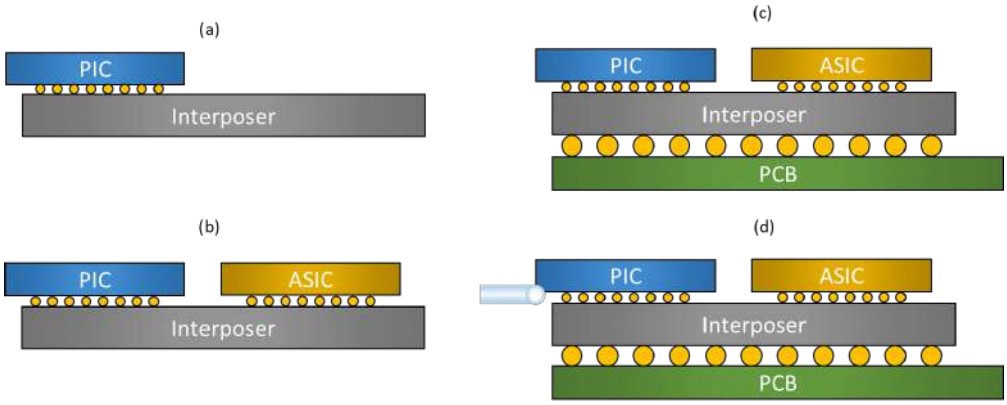

Figure 20: Photonics and Electronics Co-Packaging Process Flow

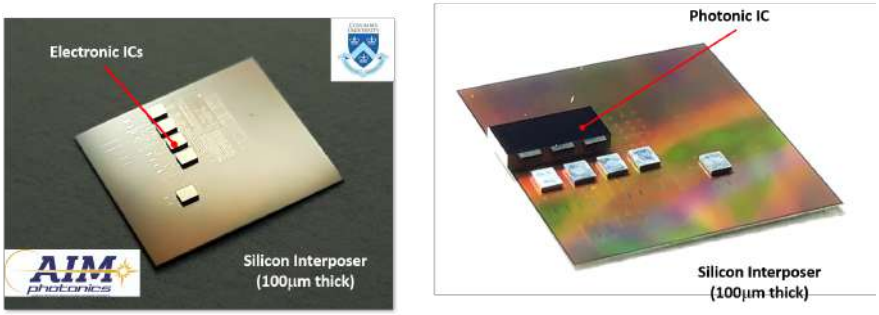

Figure 21: AIM

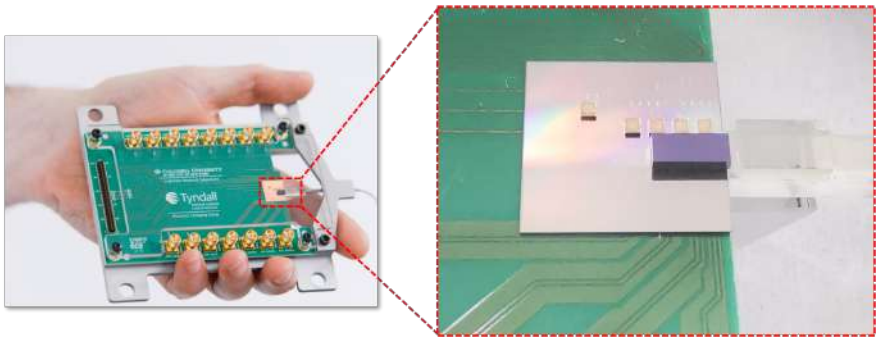

Figure 22: AIM

5.4 MEMS and Integrated System Co-Packaging

Micro-Electro-Mechanical Systems (MEMS) technologies are tiny machines with gears thinner than a stand of hair. The nature of MEMS technologies is that they are not stand-alone devices, they complement the function of other devices, or interface with other devices. This means that MEMS devices are usually application focused, such as sensors, and actuators. As such, the packaging and integration of MEMS usually involves other technologies, such as optics, photonics, RF/wireless, and microelectronics such as ASICS/EICs, or combinations of such devices. As MEMS devices include electrical functions and micromachined elements, they form a system-on-chip (SOC) or system-on package (SOP).

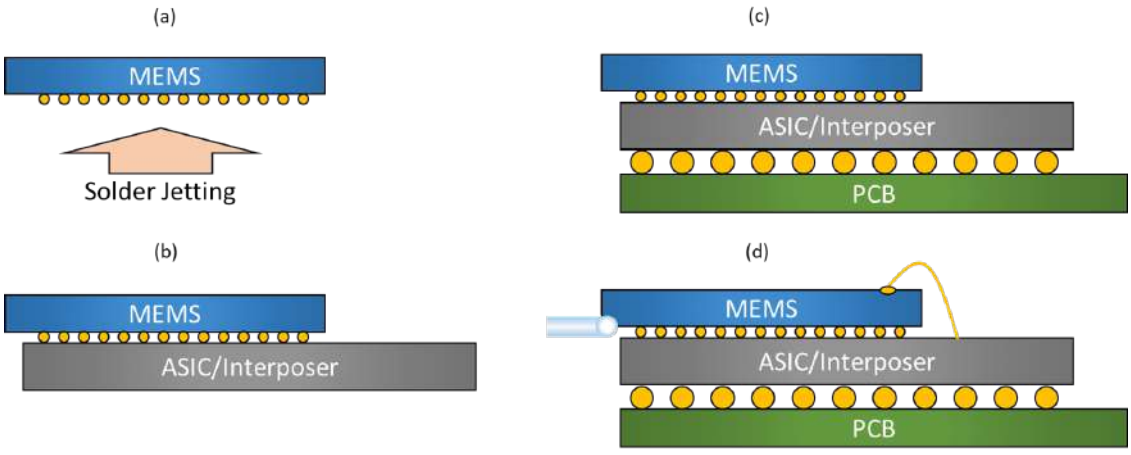

Figure 23: Packaging and assembly process flow for an integrated silicon photonic MEMS device. (a) Solder jetting of MEMS device. (b) Flip-chip soldered MEMS device onto interposer. (b) Attach flip-chip assembly onto test board (PCB), (d) optical assembly (and top-level wire bonding if required)

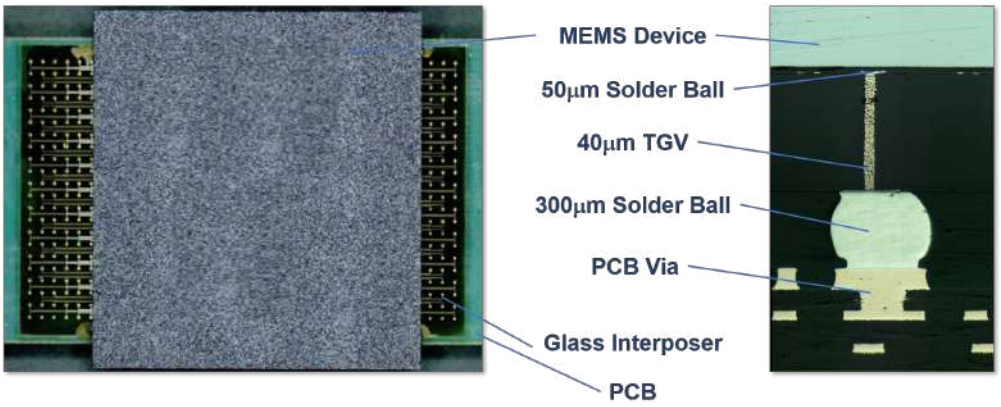

Figure 24: MEMS Packaging.

6 Accessing Photonic Packaging Technologies

6.1 ACTPHAST

Tyndall National Institute is a partner in the EU-funded ACTPHAST project which is a one-stop shop for photonics innovation in Europe. ACTPHAST supports and accelerates the innovation capacity of European SMEs by providing them with direct access to the expertise and state-of-the-art facilities in 23 of Europe's leading photonics research centres.

Figure 25: ACTPHAST supports and accelerates the innovation capacity of European SMEs by providing them with direct access to the expertise and state-of-the-art facilities in 23 of Europe's leading photonics research centres.

The technologies available within the consortium range from fibre optics and micro optics, to highly integrated photonic platforms, with capabilities extending from design through to full system prototyping. At Tyndall all our photonics packaging facilities and expertise are fully available through ACTPHAST.

For more information about this SME-focussed programme, please visit www.actphast.eu.

6.2 EUROPRACTICE and NEXTS

The photonic packaging group at Tyndall has been selected to bring advanced packaging and system integration services to Europractice. Tyndall manages the provision of advanced photonic, electronic and MEMs packaging and system integration services. The initiative is called NEXTS and is funded by the European Union's Horizon 2020 research and innovation programme. EUROPRACTICE has supported the European academic sector with design tools and Integrated Circuit prototyping for almost 30 years. The NEXTS initiative will build upon the well-established, widely-used and successful services offered by the partners, extending the service to SMEs.

For information on Photonic Packaging Services through EUROPRACTICE and NEXTS, please visit europractice-ic.com/packaging-integration/general/

Figure 26: The Photonics Packaging Group at the Tyndall National Institute in Ireland is a EUROPRACTICE partner, and offers packaging and integration services for the Silicon Photonic Integrated Circuits (Si-PICs) fabricated in the MPW runs.

6.3 PIXAPP

Figure 27: The goal of PIXAPP is to support the transition of integrated photonic devices from prototypes to manufacture via pilot-scale production.

PIXAPP is funded by the European Commission and was established in January 2017. The goal of PIXAPP is to support the transition of integrated photonic devices from prototypes to volume manufacture via pilot-scale production. PIXAPP is a distributed consortium of partners with a wide range of packaging technologies and capabilities, from the development of advanced photonic prototypes through to commercial production. A key focus of PIXAPP is to establish a set of packaging design standards and related design rules which provides users with easy access to well-defined and qualified packaging technologies that are sufficiently flexible to address a wide range of markets, from communications to sensing and medical diagnostics. PIXAPP also provides advanced training to industry, including practical hands-on laboratory-based training using state-of-the-art equipment and training on advanced PIC design, test and reliability systems.

For more information on how PIXAPP can help you move to pilot-scale photonic manufacturing, please see `www.pixapp.eu`.