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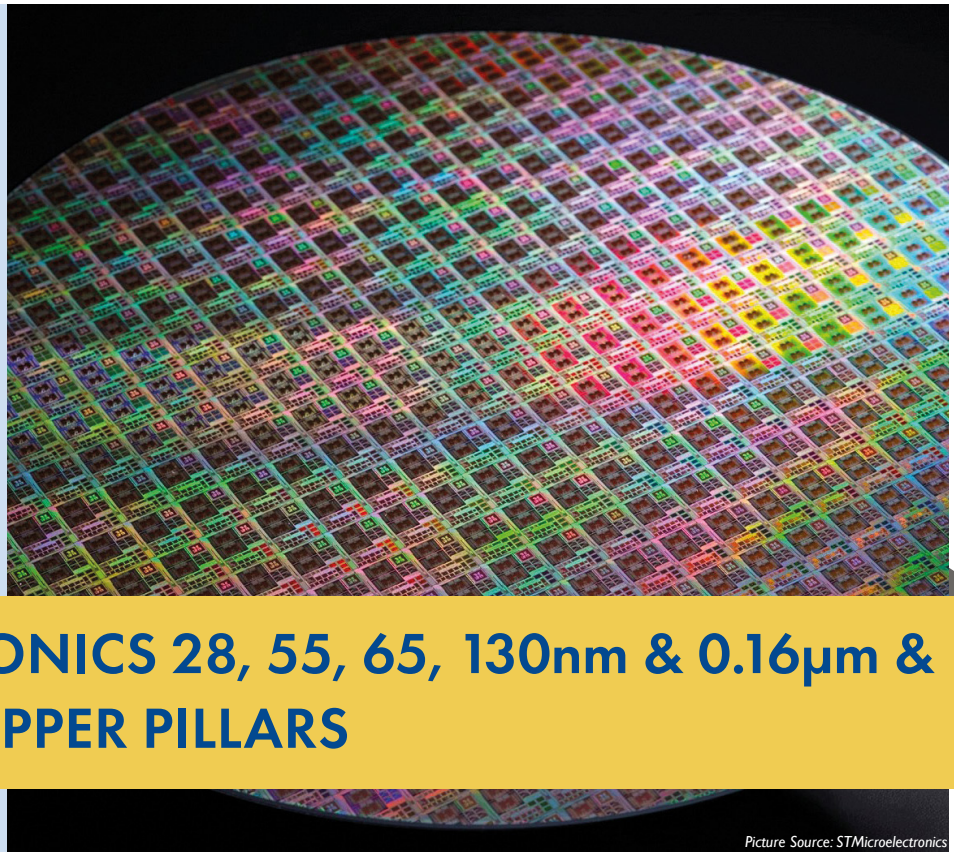

Picture Source: STMicroelectronics

STMICROELECTRONICS 28, 55, 65, 130nm & 0.16µm & WAFER LEVEL COPPER PILLARS

EUROPRACTICE-IC provides access to STMicroelectronics CMOS, BiCMOS SiGe and High Voltage Technologies for Multi-Project-Wafer Prototyping and Small Volume Production.

Why EUROPRACTICE?

- Affordable and easy access to Prototyping and Small Volume Production services for academia and industry.
- MPW (Multi-Project-Wafer) runs for various technologies, including ASICs, Photonics, MEMS and GaN.
- Advanced packaging, system integration solutions and test services.

Why STMicroelectronics?

- Leading European foundry for analog/mixed-signal (MS) semiconductor applications.
- Technologies ranging from 160nm to 28nm MS CMOS, FDSOI, SiGe, SOI, HV for telecommunication, automotive, industrial and other applications.
- Best-in-class high performance processes at affordable prices. Extensive design-kits and libraries offer.

Technology Highlights

ST 28 nm FDSOI

The 28nm FDSOI CMOS technology is the most advanced node offered by STMicroelectronics. SOI based technology provides low leakage devices and wide back biasing voltage capabilities. Main applications are for low power digital and mixed-signal (MS)/RF applications. Extensive design kit and libraries are offered with compatibility with a wide range of CAD tools.

ST 55 nm SiGe BiCMOS

European flagship industrial SiGe BiCMOS technology for terahertz range applications. The process comes with an extremely fast bipolar transistor and with 8 Cu backend metal layers including a very thick top layer for inductances with high-quality factors. The CMOS part also comes with extended digital standard cells and IO libraries.

ST 65 nm CMOS

Standard CMOS process with digital, mixed-signal and RF capabilities. RF components like inductors, varactors and MIM capacitors are provided. This is a technology of choice for applications where a high density of digital circuitry is required along with analog components, i.e. for mixed-signal applications.

ST 130 nm SiGe BiCMOS 9MW

130nm SiGe process with Bipolar transistor and thick metal layers for RF/mmW applications (Frequencies up to 77 GHz), wireless communication (around 60GHz for WLAN) and optical communications systems.

ST 130nm CMOS 9A

Low Power 130nm CMOS process with the extension of the RRAM/OxRAM NVM done as a post-process at CEA-Leti.

ST 130nm HCMOS 9-SOI-FEM

H9-SOI-FEM is built on the same solid basis of the previous standard H9SOI technology and shares with it the robustness, the capability to address all FEM (stands for Front End Module) applications (RF Switches, PA, LNA) and the expertise in RF SOI process.

ST 0.16µm BCD

Smart-Power BCD8sP and BCD8s-SOI technologies combine high power transistors with low power digital and analog devices on a single chip. This technology is dedicated to power management systems, power supplies, motor drivers, amplifiers.

ST Cu Pillars Interconnects

To extract the maximum performance out of the chips taped out in advanced technology nodes and for reduced interconnect parasitic losses, Cu pillars (micro bumps) of Sn/Ag alloy is offered on 300mm ST technologies with a pitch of 90µm.

Technology Details

CMOS 28nm FDSOI

- 28nm drawn poly length.
- Triple well. Fully Depleted SOI devices with ultrathin BOX and Ground Plane.
- Body biasing. Dual Vt MOS transistors (LVT, RVT).
- 8 metal layers for interconnect.
- 2 thick Cu top metal (0.88 micron).
- Dual gate oxide (1.0V for core and 1.8V for IO).
- Low k inter-level dielectric.
- Fringe MOM capacitors.
- Inductors Analog / RF capabilities
- Various power supplies supported: 1.8V, 1.0V.
- Standard cell libraries.
- Embedded memory (Single port RAM / ROM / Dual port RAM).

BiCMOS 55nm SiGe

- 55nm drawn poly length.
- Bipolar SiGe-C NPN transistors: High Speed NPN with Ft=320GHz.
- Deep Nwell, Deep Trench Isolation.
- Triple Vt MOS transistors (LVT, RVT and SVT).
- Ultra-thick Cu top metal 3.0 micron.
- 8 Cu metal layers with ultra-thick top layer (3.0µm).
- Millimetre-wave inductors.
- Analog / RF capabilities.
- MIM & Fringe MOM capacitors.
- Various power supplie supported: 2.5V, 1.2V, 1V.
- Standard cell libraries.
- Embedded memory (Single port RAM / ROM / Dual port RAM).

CMOS 65nm LPGP

- 65nm drawn poly length.
- 7 metal layers.
- Deep Nwell and Deep Trench Isolation.
- Triple Vt MOS transistors (LVT, RVT and SVT).
- Low Power and General Purpose MOS transistors.
- Dual gate oxide (1.0V for core and 2.5V for IO).
- MIM & Fringe MOM capacitors.
- Inductors Analog / RF capabilities.
- Various power supplies supported: 2.5V, 1.2V, 1V.
- Standard cell libraries.
- Embedded memory (Single port RAM / ROM / Dual Port RAM).

BiCMOS9MW 130nm SiGe

- 130nm drawn, 130nm effective.
- Deep Nwell and Deep Trench Isolation.
- Double Vt transistor offering (Low Leakage, High Speed).
- Dual gate oxide (1.2V for core and 2.5V for IO).
- Bipolar SiGe transistors.
- Typical Ft (for 2 families above): 230/150GHz.
- Power supply 1.2V.
- 6 Cu metal layers.
- MIM capacitors.
- Standard cell libraries.
- Embedded memory (Single port RAM).

HCMOS9A 130nm

- CMOS gate length: 130nm drawn poly length.
- Deep Nwell, Deep Trench Isolation.
- Vt transistor offering (Low Power, Analog).
- Bipolar NPN transistors.
- Typical beta: 90.
- Ft Max @ Vbc=0: 2,4GHz.
- 2 specific implant levels: NDRIFT & PDRIFT MIM 5fF/µm2.
- Double gate oxide for analog features.
- 4 metal layers in standard Fluorinated SiO2 (intermetal dielectric).
- Power supply: 1. 2V for Digital, 4.6V for Analog application multiple.
- Standard cell libraries.

H9-SOI-FEM 130nm

- CMOS gate length: 130nm.
- SOI wafers with high resistive substrate 2.5V.
- Body Contacted CMOS.
- Floating Body CMOS 5.0V NLD-MOS.
- PLDMOS 1.2V High Speed 130nm.
- 4 metal layers for interconnect
- Ultra-thick Cu top metal (4.0 micron).
- High Linearity MIM capacitor.
- Standard cell libraries.

BCD8sP & BCD8s-SOI

- Bipolar-CMOS-DMOS.
- 4 Metal Levels with last Al Thick-Power metal.
- Baseline 3.3V CMOS.
- Medium Voltage Modules: 6V / 20V / 40V NDMOS and PDMOS.
- High Voltage Modules: 70V / 100V / 140V / 200V NDMOS and PDMOS Optional 2nd gate oxide for 1.8V.
- CMOS Dielectric Isolation on SOI.
- Available memory: OTP.

Cu Pillars Interconnects

- Pillar of copper + Sn/Ag alloy capping.
- Small Diameter / Height: 62µm / 65 µm.
- Fine pitch (down to 90µm).
- Available on ST 300mm processes.
- Fast turnaround (2 weeks).

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