EUROPRACTICE

TSMC RUN SCHEDULE 2026

December 11, 2025 – v1.2

MPW RUN SCHEDULE 2026

N7, N16, 22nm

28nm & 40nm

55nm ~ 0.13um

MPW RUN SCHEDULE 2026 – N7, N16, 22nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
7nm CMOS Logic or RF FinFET***	April	10086	TMWB84	15	Dec 23	Feb 6	Mar 11	Apr 5	Apr 7	Aug 6
	The 7nm Cybershuttle deadline(s) for the second half of 2026 will be known in March '26									
16nm CMOS Logic or RF FinFET Compact***	February	10078	TMWB78	14	Oct 24 (2025)	Dec 4 (2025)	Jan 5	Jan 29	Feb 2	May 1
	April	10079	TMWB79	14	Dec 23	Feb 6	Mar 11	Apr 5	Apr 7	Jul 4
	June	10080	TMWB80	14	Feb 25	Apr 2	May 4	May 28	Jun 1	Aug 28
	August	10081	TMWB81	14	Apr 27	Jun 11	Jul 13	Aug 6	Aug 10	Nov 6
	October	10082	TMWB82	14	Jun 30	Aug 6	Sep 7	Oct 1	Oct 5	Jan 2 (2027)
	November	10083	TMWB83	14	Aug 3	Oct 1	Nov 2	Nov 26	Nov 30	Feb 26 (2027)
22nm CMOS Logic or RF ULL (w/ or wo/ ReRam)	March	10070	TMWB70	15	Nov 25 (2025)	Jan 2	Feb 4	Mar 1	Mar 3	May 30
	April	10071	TMWB71	15	Dec 23	Feb 13	Mar 18	Apr 12	Apr 14	Jul 11
	May	10072	TMWB72	15	Jan 26	Mar 13	Apr 15	May 10	May 12	Aug 8
	June	10073	TMWB73	15	Feb 25	May 1	Jun 3	Jun 28	Jun 30	Sep 26
	August	10074	TMWB74	15	Apr 27	Jun 5	Jul 8	Aug 2	Aug 4	Oct 31
	September	10075	TMWB75	15	May 25	Jul 3	Aug 5	Aug 30	Sep 1	Nov 28
	November	10076	TMWB76	15	Aug 3	Sep 4	Oct 7	Nov 1	Nov 3	Jan 30 (2027)
	December	10077	TMWB77	15	Aug 31	Oct 2	Nov 4	Nov 29	Dec 1	Feb 27 (2027)

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* Shipment date is an estimation. Additional cycle time of (1~3 weeks) might be required. See shipment guidelines.
** Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.
*** The estimated shipment date for RF FinFET Compact (0.8/1.8V) will be 2 days later.

MPW RUN SCHEDULE 2026 – 28nm & 40nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
TSMC 28nm CMOS Logic or RF HPC/HPC+	February	10057	TMWB61	15	Oct 24 (2025)	Dec 5 (2025)	Jan 7	Feb 1	Feb 3	Apr 26
	March	10058	TMWB62	15	Nov 25 (2025)	Jan 2	Feb 4	Mar 1	Mar 3	May 24
	May	10059	TMWB63	15	Jan 26	Mar 6	Apr 8	May 3	May 5	Jul 26
	June	10060	TMWB64	15	Feb 25	Apr 3	May 6	May 31	Jun 2	Aug 23
	August	10061	TMWB65	15	Apr 27	Jun 12	Jul 15	Aug 9	Aug 11	Nov 1
	September	10062	TMWB66	15	May 25	Jul 10	Aug 12	Sep 6	Sep 8	Nov 29
	November	10063	TMWB67	15	Aug 3	Sep 11	Oct 14	Nov 8	Nov 10	Jan 31 (2027)
	December	10064	TMWB68	15	Aug 31	Oct 9	Nov 11	Dec 6	Dec 8	Feb 28 (2027)
40nm CMOS Logic or MS/RF, LP (no triple gate oxide)	January	10046-LP	TMWB50	12	Sep 24 (2025)	Nov 20 (2025)	Dec 22 (2025)	Jan 15	Jan 19	Apr 4
	February	10047	TMWB51	14	Oct 24 (2025)	Dec 25 (2025)	Jan 26	Feb 19	Feb 23	May 9
	April	10048-LP	TMWB52	12	Dec 23	Feb 12	Mar 16	Apr 9	Apr 13	Jun 27
	May	10049-LP	TMWB53	14	Jan 26	Mar 12	Apr 13	May 7	May 11	Jul 25
	June	10050-LP	TMWB54	14	Feb 25	Apr 16	May 18	Jun 11	Jun 15	Aug 29
	August	10051-LP	TMWB55	14	Apr 27	Jun 11	Jul 13	Aug 6	Aug 10	Oct 24
	September	10052	TMWB56	12	May 25	Jul 16	Aug 17	Sep 10	Sep 14	Nov 28
	October	10053-LP	TMWB57	14	Jun 30	Aug 13	Sep 14	Oct 8	Oct 12	Dec 28
	December	10054-LP	TMWB58	14	Aug 31	Oct 15	Nov 16	Dec 10	Dec 14	Feb 27 (2027)
40nm CMOS Logic or MS/RF, GP (no triple gate oxide)	April	10047	TMWB52	12	Dec 23	Feb 12	Mar 16	Apr 9	Apr 13	Jun 27
	September	10052	TMWB56	12	May 25	Jul 16	Aug 17	Sep 10	Sep 14	Nov 28

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MPW RUN SCHEDULE 2026 – 55nm ~ 0.13um

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
55nm CMOS Logic or MS/RF, GP or LP or ULP	June	10045	TMWB49	14	Feb 25	Apr 17	May 20	Jun 14	Jun 16	Aug 27
65nm CMOS Logic or MS/RF, GP or LP***	March	10031	TMWB40	14	Nov 25 (2025)	Jan 9	Feb 11	Mar 8	Mar 10	May 22
	April	10032	TMWB41	12	Dec 23	Feb 20	Mar 25	Apr 19	Apr 21	Jul 3
	June	10033	TMWB43	12	Feb 25	Apr 17	May 20	Jun 14	Jun 16	Aug 28
	July	10034	TMWB44	14	Mar 25	May 22	Jun 24	Jul 19	Jul 21	Oct 2
	September	10035	TMWB45	14	May 25	Jul 17	Aug 19	Sep 13	Sep 15	Nov 27
	October	10036	TMWB46	12	Jun 30	Aug 21	Sep 23	Oct 18	Oct 20	Jan 3 (2027)
	November	10037	TMWB47	14	Aug 3	Sep 18	Oct 21	Nov 15	Nov 17	Jan 29 (2027)
90nm CMOS Logic or MS/RF, GP or LP	August	10030	TMWB38	14	Apr 27	Jun 19	Jul 22	Aug 16	Aug 18	Oct 23
0.13µm CMOS Logic or MS/RF, GP or LP (12-inch)	April	10026	TMWB33	12	Dec 23	Feb 13	Mar 18	Apr 12	Apr 14	Jun 18
	August	10027	TMWB35	12	Apr 27	Jun 19	Jul 22	Aug 16	Aug 18	Oct 22
	November	10029	TMWB36	14	Aug 3	Sep 18	Oct 21	Nov 15	Nov 17	Jan 21 (2027)
0.13µm CMOS BCD plus (12-inch)	April	10026	TMWB33	12	Dec 23	Feb 13	Mar 18	Apr 12	Apr 14	Jun 18
	August	10027	TMWB35	12	Apr 27	Jun 19	Jul 22	Aug 16	Aug 18	Oct 22
	November	10029	TMWB36	14	Aug 3	Sep 18	Oct 21	Nov 15	Nov 17	Jan 21 (2027)

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* Shipment date is an estimation. Additional cycle time of (1~3 weeks) might be required. See shipment guidelines.
** Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.
*** 65nm eFuse is only supported in Fab12. Please select the correct shuttle.

GUIDELINES FOR SCHEDULE 2026

Design registration guidelines

- Single reservation for multiple chips
- No backup reservation
- Provide single GDS with all designs,
  - Enclosed with TSMC sealring + 80um scribe (post-shrink if applicable).
  - If designs are not identical, put marker in the scribe line.
  - Add dummies to the scribe line for 12-inch tape-outs.
  - Exception: multiple reservations accepted for different projects with different metal stacks or far backend.

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Shipment guidelines

- The estimated shipment date is applicable for reservations with quantity <200 dies.
- If additional samples are required above 200 dies, additional cycle time of 1~3 weeks might be needed.
- Cycle time estimates are based on typical conditions. Corner wafers or SHDMiM processing requires additional cycle time.
- Optional services adding cycle time
  - Lead free & cupper bumping: 4 days
  - Extra wafer thinning (thinner than 10mils): up to 12 days
  - Additional bumped wafer thinning and die saw (each 200 ea.): 5 working days

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ReRam IP Merge Guidelines

- To ensure timely inclusion in the TSMC MPW when an IP merge is required, deliver the final GDS 2 weeks in advance to allow sufficient time for integration and validation.
- Why This Matters:
  - **Complete LVS Setup Required**

    A fully validated LVS setup must be in place before initiating the merge process.
  - **Ip-transfer**

    Third-party IPs have to be transferred from the vendor to the TSMC merge team, which may introduce delays in the process.
  - **Increased Complexity with Multiple IP Instances**

    Merging several IP blocks adds significant complexity and increases the risk of integration issues.
  - **Merge Errors Can Jeopardize the Deadline**

    Errors discovered after merging may delay the process and reduce the likelihood of meeting the MPW schedule. TSMC requests to re-submit the merge even for minor typos or missing files

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Questions?

Contact our teams through a portal support case:

Support Tape-out	For support on the tape-out submission
Support SalesOps	For support on portal, quotations, export documents, purchase orders, and design registration questions
Support EP packaging	For any question related to the Europractice packaging offer.
Support Foundry	For support on foundry libraries, PDK's (installation, flavors, bugs, ...), LVS

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Release notes

- October 22, 2025
  - Release of v 1.0 2025
- November 21, 2025
  - Release of v1.1 2025
  - Clarification cycle time information slide 8
- December 11, 2025
  - Release of v1.2 2025
  - Clarification shipment date/ final GDS date and others */**/***

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