



# TSMC RUN SCHEDULE 2026

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January 30, 2026 – v1.3b

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# MPW RUN SCHEDULE 2026

N7, N16, 22nm

28nm & 40nm

55nm ~ 0.13um

# MPW RUN SCHEDULE 2026 – N7, N16, 22nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
7nm CMOS Logic or RF FinFET***	April	I0086	TMWB84	15	Dec 23	Feb 6	Mar 11	Apr 5	Apr 7	Aug 6
	The 7nm Cybershuttle deadline(s) for the second half of 2026 will be known in March '26									
16nm CMOS Logic or RF FinFET Compact***	February	I0078	TMWB78	14	Oct 24 (2025)	Dec 4 (2025)	Jan 5	Jan 29	Feb 2	May 1
	April	I0079	TMWB79	14	Dec 23	Feb 6	Mar 11	Apr 5	Apr 7	Jul 4
	June	I0080	TMWB80	14	Feb 25	Apr 2	May 4	May 28	Jun 1	Aug 28
	August	I0081	TMWB81	14	Apr 27	Jun 11	Jul 13	Aug 6	Aug 10	Nov 6
	October	I0082	TMWB82	14	Jun 30	Aug 6	Sep 7	Oct 1	Oct 5	Jan 2 (2027)
	November	I0083	TMWB83	14	Aug 3	Oct 1	Nov 2	Nov 26	Nov 30	Feb 26 (2027)
22nm CMOS Logic or RF ULL (w/ or wo/ ReRam)	March	I0070	TMWB70	15	Nov 25 (2025)	Jan 2	Feb 4	Mar 1	Mar 3	May 30
	April	I0071	TMWB71	15	Dec 23	Feb 13	Mar 18	Apr 12	Apr 14	Jul 11
	May	I0072	TMWB72	15	Jan 26	Mar 13	Apr 15	May 10	May 12	Aug 8
	June	I0073	TMWB73	15	Feb 25	May 1	Jun 3	Jun 28	Jun 30	Sep 26
	August	I0074	TMWB74	15	Apr 27	Jun 5	Jul 8	Aug 2	Aug 4	Oct 31
	September	I0075	TMWB75	15	May 25	Jul 3	Aug 5	Aug 30	Sep 1	Nov 28
	November	I0076	TMWB76	15	Aug 3	Sep 4	Oct 7	Nov 1	Nov 3	Jan 30 (2027)
	December	I0077	TMWB77	15	Aug 31	Oct 2	Nov 4	Nov 29	Dec 1	Feb 27 (2027)

# MPW RUN SCHEDULE 2026 – 28nm & 40nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
TSMC 28nm CMOS Logic or RF HPC/HPC+	February	I0057	TMWB61	15	Oct 24 (2025)	Dec 5 (2025)	Jan 7	Feb 1	Feb 3	Apr 26
	March	I0058	TMWB62	15	Nov 25 (2025)	Jan 2	Feb 4	Mar 1	Mar 3	May 24
	May	I0059	TMWB63	15	Jan 26	Mar 6	Apr 8	May 3	May 5	Jul 26
	June	I0060	TMWB64	15	Feb 25	Apr 3	May 6	May 31	Jun 2	Aug 23
	August	I0061	TMWB65	15	Apr 27	Jun 12	Jul 15	Aug 9	Aug 11	Nov 1
	September	I0062	TMWB66	15	May 25	Jul 10	Aug 12	Sep 6	Sep 8	Nov 29
	November	I0063	TMWB67	15	Aug 3	Sep 11	Oct 14	Nov 8	Nov 10	Jan 31 (2027)
	December	I0064	TMWB68	15	Aug 31	Oct 9	Nov 11	Dec 6	Dec 8	Feb 28 (2027)
40nm CMOS Logic or MS/RF, LP (no triple gate oxide)	January	I0046-LP	TMWB50	12	Sep 24 (2025)	Nov 20 (2025)	Dec 22 (2025)	Jan 15	Jan 19	Apr 4
	February	I0047	TMWB51	14	Oct 24 (2025)	Dec 25 (2025)	Jan 26	Feb 19	Feb 23	May 9
	April	I0048-LP	TMWB52	12	Dec 23	Feb 12	Mar 16	Apr 9	Apr 13	Jun 27
	May	I0049-LP	TMWB53	14	Jan 26	Mar 12	Apr 13	May 7	May 11	Jul 25
	June	I0050-LP	TMWB54	14	Feb 25	Apr 16	May 18	Jun 11	Jun 15	Aug 29
	August	I0051-LP	TMWB55	14	Apr 27	Jun 11	Jul 13	Aug 6	Aug 10	Oct 24
	September	I0052	TMWB56	12	May 25	Jul 16	Aug 17	Sep 10	Sep 14	Nov 28
	October	I0053-LP	TMWB57	14	Jun 30	Aug 13	Sep 14	Oct 8	Oct 12	Dec 28
	December	I0054-LP	TMWB58	14	Aug 31	Oct 15	Nov 16	Dec 10	Dec 14	Feb 27 (2027)
40nm CMOS Logic or MS/RF, GP (no triple gate oxide)	February	I0047	TMWB51	14	Oct 24 (2025)	Dec 25 (2025)	Jan 26	Feb 19	Feb 23	May 9
	September	I0052	TMWB56	12	May 25	Jul 16	Aug 17	Sep 10	Sep 14	Nov 28

# MPW RUN SCHEDULE 2026 – 55nm ~ 0.13um

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
55nm CMOS Logic or MS/RF, GP or LP or ULP	June	I0045	TMWB49	I4	Feb 25	Apr 17	May 20	Jun 14	Jun 16	Aug 27
65nm CMOS Logic or MS/RF, GP or LP***	March	I0031	TMWB40	I4	Nov 25 (2025)	Jan 9	Feb 11	Mar 8	Mar 10	May 22
	April	I0032	TMWB41	I2	Dec 23	Feb 20	Mar 25	Apr 19	Apr 21	Jul 3
	June	I0033	TMWB43	I2	Feb 25	Apr 17	May 20	Jun 14	Jun 16	Aug 28
	July	I0034	TMWB44	I4	Mar 25	May 22	Jun 24	Jul 19	Jul 21	Oct 2
	September	I0035	TMWB45	I4	May 25	Jul 17	Aug 19	Sep 13	Sep 15	Nov 27
	October	I0036	TMWB46	I2	Jun 30	Aug 21	Sep 23	Oct 18	Oct 20	Jan 3 (2027)
	November	I0037	TMWB47	I4	Aug 3	Sep 18	Oct 21	Nov 15	Nov 17	Jan 29 (2027)
90nm CMOS Logic or MS/RF, GP or LP	August	I0030	TMWB38	I4	Apr 27	Jun 19	Jul 22	Aug 16	Aug 18	Oct 23
0.13um CMOS Logic or MS/RF, GP or LP (12-inch)	June	I0026	TMWB32	I4	Feb 25	Apr 3	May 06	May 31	June 02	Aug 03
0.13um CMOS BCD plus (12-inch)	June	I0026	TMWB32	I4	Feb 25	Apr 3	May 06	May 31	June 02	Aug 03

\* Shipment date is an estimation. Additional cycle time of (1~3 weeks) might be required. See shipment guidelines.

\*\* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

\*\*\* 65nm eFuse is only supported in FabI2. Please select the correct shuttle.



# GUIDELINES FOR SCHEDULE 2026



- Single reservation for multiple chips
- No backup reservation
- Provide single GDS with all designs,
  - ▶ Enclosed with TSMC searing + 80um scribe (post-shrink if applicable).
  - ▶ If designs are not identical, put marker in the scribe line.
  - ▶ Add dummies to the scribe line for 12-inch tape-outs.
  - ▶ Exception: multiple reservations accepted for different projects with different metal stacks or far backend.

- The estimated shipment date is applicable for reservations with quantity <200 dies.
- If additional samples are required above 200 dies, additional cycle time of 1~3 weeks might be needed.
- Cycle time estimates are based on typical conditions. Corner wafers or SHDMiM processing requires additional cycle time.
- Optional services adding cycle time
  - ▶ Lead free & copper bumping: 4 days
  - ▶ Extra wafer thinning (thinner than 10mils): up to 12 days
  - ▶ Additional bumped wafer thinning and die saw (each 200 ea.): 5 working days



- To ensure timely inclusion in the TSMC MPW when an IP merge is required, deliver the final GDS 2 weeks in advance to allow sufficient time for integration and validation.
- Why This Matters:
  - ▶ **Complete LVS Setup Required**  
A fully validated LVS setup must be in place before initiating the merge process.
  - ▶ **Ip-transfer**  
Third-party IPs have to be transferred from the vendor to the TSMC merge team, which may introduce delays in the process.
  - ▶ **Increased Complexity with Multiple IP Instances**  
Merging several IP blocks adds significant complexity and increases the risk of integration issues.
  - ▶ **Merge Errors Can Jeopardize the Deadline**  
Errors discovered after merging may delay the process and reduce the likelihood of meeting the MPW schedule. TSMC requests to re-submit the merge even for minor typos or missing files

## Contact our teams through a portal support case:

**Support Tape-out** For support on the tape-out submission

**Support SalesOps** For support on portal, quotations, export documents, purchase orders, and design registration questions

**Support EP packaging** For any question related to the Europractice packaging offer.

**Support Foundry** For support on foundry libraries, PDK's (installation, flavors, bugs, ...), LVS

- January 30, 2026
  - ▶ Release v1.3b 2025
  - ▶ Updated run 10047 40nm CMOS Logic or MS/RF, GP
- January 12, 2026
  - ▶ Release v1.3a 2025
  - ▶ Updated 0.13 UM- one consolidated shuttle in 2026
- January 05, 2026
  - ▶ Release of v1.3 2025
  - ▶ Removed ReRam slide 9
- December 11, 2025
  - ▶ Release of v1.2 2025
  - ▶ Clarification shipment date/ final GDS date and others \*/\*\*/\*\*
- November 21, 2025
  - ▶ Release of v1.1 2025
  - ▶ Clarification cycle time information slide 8
- October 22, 2025
  - ▶ Release of v 1.0 2025



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