



# TSMC RUN SCHEDULE 2026

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January 26, 2026 – v1.3c



# MINI@SIC RUN SCHEDULE 2026

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| Technology  | Month    | Run   | Foundry ref | Fab | Reserve before | Signed quote/PO before | Dry run GDS | Final GDS** | Tape-out | Estimated shipment date* |
|---|----------|-------|-------------|-----|----------------|------------------------|-------------|-------------|----------|--------------------------|
| 16nm RF FinFET Compact (0.8/1.8V)***  | April    | I0084 | TMWB79      | I4  | Dec 23 (2025)  | Jan 6                  | Feb 24      | Mar 24      | Apr 7    | Jul 1                    |
|   | November | I0085 | TMWB83      | I4  | Jul 25         | Oct 1                  | Oct 19      | Nov 16      | Nov 30   | Feb 23 (2027)            |
| 28nm RF HPC Plus (0.9/1.8V, 0.9/2.5V)   | March    | I0065 | TMWB62      | I5  | Nov 25 (2025)  | Jan 2                  | Jan 20      | Feb 17      | Mar 3    | May 24                   |
|   | May      | I0066 | TMWB63      | I5  | Jan 26         | Mar 6                  | Mar 24      | Apr 21      | May 5    | Jul 26                   |
|   | June     | I0067 | TMWB64      | I5  | Feb 25         | Apr 3                  | Apr 21      | May 19      | Jun 2    | Aug 23                   |
|   | August   | I0068 | TMWB65      | I5  | Apr 27         | Jun 12                 | Jun 30      | Jul 28      | Aug 11   | Nov 1                    |
|   | November | I0069 | TMWB67      | I5  | Jul 25         | Sep 11                 | Sep 29      | Oct 27      | Nov 10   | Jan 31 (2027)            |
| 40nm Logic 40LP (1.1/1.8V, 1.1/2.5V)<br>Mixed-Signal/RF 40LP (1.1/1.8V, 1.1/2.5V) | April    | I0055 | TMWB52      | I2  | Dec 23         | Feb 12                 | Mar 2       | Mar30       | Apr 13   | Jun 24                   |
|   | October  | I0056 | TMWB57      | I4  | Jun 30         | Aug 13                 | Aug 31      | Sep 28      | Oct 12   | Dec 23                   |

\* Shipment date is an estimation. Additional cycle time of (1~3 weeks) might be required. See shipment guidelines.

\*\* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

\*\*\* The estimated shipment date for RF FinFET Compact (0.8/1.8V) will be 2 days later.

| Technology  | Month     | Run      | Foundry ref | Fab | Reserve before | Signed quote/PO before | Dry run GDS | Final GDS** | Tape-out | Estimated shipment date* |
|---|-----------|----------|-------------|-----|----------------|------------------------|-------------|-------------|----------|--------------------------|
| 65nm CMOS Logic or MS/RF or LP  | March     | I0038-LP | TMWB40      | I4  | Nov 25 (2025)  | Jan 9                  | Jan 27      | Feb 24      | Mar 10   | May 22                   |
|   | May       | I0040-LP | TMWB42      | I4  | Jan 26         | Mar 13                 | Mar 31      | Apr 28      | May 12   | Jul 24                   |
|   | July      | I0041-LP | TMWB44      | I4  | Mar 25         | May 22                 | Jun 9       | Jul 7       | Jul 21   | Oct 2                    |
|   | September | I0042-LP | TMWB45      | I4  | May 25         | Jul 17                 | Aug 4       | Sep 1       | Sep 15   | Nov 27                   |
|   | November  | I0044-LP | TMWB47      | I4  | Jul 25         | Sep 18                 | Oct 6       | Nov 3       | Nov 17   | Jan 29 (2027)            |
| 0.13µm C High Voltage BCD Plus<br>(1.5/3.3/5/10/12/16/20/24/28/36/VG1.5/3.3/5V) | June      | I0025    | TMWB32      | I4  | Feb 25         | Apr 3                  | Apr 21      | May 19      | Jun 02   | Aug 03                   |

\* Shipment date is an estimation. Additional cycle time of (1~3 weeks) might be required. See shipment guidelines.

\*\* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

# GUIDELINES FOR SCHEDULE 2026

The background features a large, semi-transparent blue sphere with a fine, grid-like texture on the left side. A horizontal line, composed of an orange top segment and a yellow bottom segment, spans the width of the page near the bottom.



- Single reservation for multiple chips
- No backup reservation
- Provide single GDS with all designs,
  - ▶ Enclosed with TSMC searing + 80um scribe (post-shrink if applicable).
  - ▶ If designs are not identical, put marker in the scribe line.
  - ▶ Add dummies to the scribe line for 12-inch tape-outs.
  - ▶ Exception: multiple reservations accepted for different projects with different metal stacks or far backend.

- The estimated shipment date is applicable for reservations with quantity <200 dies.
- If additional samples are required, additional cycle time of (1~3 weeks) might be needed.
- Cycle time estimates are based on typical conditions. Corner wafers or SHDMiM processing requires additional cycle time.
- Optional services adding cycle time
  - ▶ Lead free & copper bumping: 4 days
  - ▶ Extra wafer thinning (thinner than 10mils): up to 12 days
  - ▶ Additional bumped wafer thinning and die saw (each 200 ea.): 5 working days

- To ensure timely inclusion in the TSMC MPW when an IP merge is required, deliver the final GDS 2 weeks in advance to allow sufficient time for integration and validation.
- Why This Matters:
  - ▶ **Complete LVS Setup Required**  
A fully validated LVS setup must be in place before initiating the merge process.
  - ▶ **Ip-transfer**  
Third-party IPs have to be transferred from the vendor to the TSMC merge team, which may introduce delays in the process.
  - ▶ **Increased Complexity with Multiple IP Instances**  
Merging several IP blocks adds significant complexity and increases the risk of integration issues.
  - ▶ **Merge Errors Can Jeopardize the Deadline**  
Errors discovered after merging may delay the process and reduce the likelihood of meeting the MPW schedule. TSMC requests to re-submit the merge even for minor typos or missing files



## Contact our teams through a portal support case:

**Support Tape-out** For support on the tape-out submission

**Support SalesOps** For support on portal, quotations, export documents, purchase orders, and design registration questions

**Support EP packaging** For any question related to the Europractice packaging offer.

**Support Foundry** For support on foundry libraries, PDK's (installation, flavors, bugs, ...), LVS

- January 26, 2026
  - ▶ Release of v1.3c 2026
  - ▶ GDS dry run dates updated
- January 15, 2026
  - ▶ Release of v1.3b 2026
  - ▶ 65 nm Run 10039-LP cancelled
- January 12, 2026
  - ▶ Release of v1.3a 2026
  - ▶ Updated 0.13 UM- only one consolidated shuttle in 2026
  - ▶ Update on 65 nm shuttle availability – added shuttle in May
  - ▶ Run 10039-GP 65 nm changed to 10039-LP
- January 05, 2026
  - ▶ Release of v1.3 2026
  - ▶ Removed ReRam slide 9
  - ▶ Update on 65 nm shuttle availability
- December 11, 2025
  - ▶ Release of v1.2 2026
  - ▶ Clarification shipment date/ final GDS date and others \*/\*\*/\*\*
- November 21, 2025
  - ▶ Release of v1.1 2026
  - ▶ Clarification cycle time information slide 8
- October 24, 2025
  - ▶ Release of v1.0 2026



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