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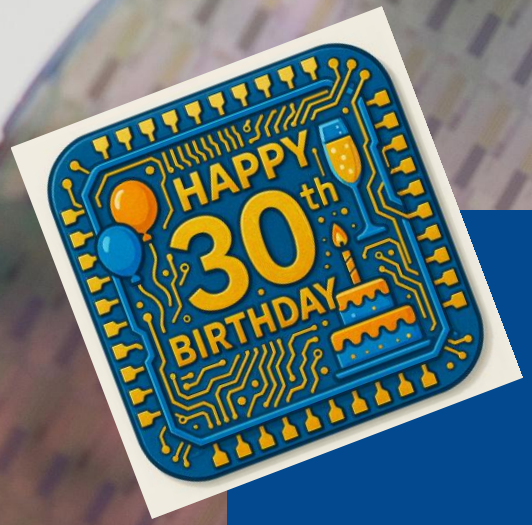

TSMC RUN SCHEDULE 2026

January 05, 2026 – v1.3

MINI@SIC RUN SCHEDULE 2026

Mini@sic RUN SCHEDULE 2026 – 16nm, 28nm, 40nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
16nm RF FinFET Compact (0.8/1.8V)***	April	10084	TMWB79	14	Dec 23 (2025)	Feb 6	Feb 24	Mar 24	Apr 7	Jul 1
	November	10085	TMWB83	14	Aug 3	Oct 1	Oct 19	Nov 16	Nov 30	Feb 23 (2027)
28nm RF HPC Plus (0.9/1.8V, 0.9/2.5V)	March	10065	TMWB62	15	Nov 25 (2025)	Jan 2	Feb 4	Feb 17	Mar 3	May 24
	May	10066	TMWB63	15	Jan 26	Mar 6	Apr 8	Apr 21	May 5	Jul 26
	June	10067	TMWB64	15	Feb 25	Apr 3	May 6	May 19	Jun 2	Aug 23
	August	10068	TMWB65	15	Apr 27	Jun 12	Jul 15	Jul 28	Aug 11	Nov 1
	November	10069	TMWB67	15	Aug 3	Sep 11	Oct 14	Oct 27	Nov 10	Jan 31 (2027)
40nm Logic 40LP (1.1/1.8V, 1.1/2.5V) Mixed-Signal/RF 40LP (1.1/1.8V, 1.1/2.5V)	April	10055	TMWB52	12	Dec 23	Feb 12	Mar 02	Mar30	Apr 13	Jun 24
	October	10056	TMWB57	14	Jun 30	Aug 13	Aug 31	Sep 28	Oct 12	Dec 23

* Shipment date is an estimation. Additional cycle time of (1~3 weeks) might be required. See shipment guidelines.

** Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

*** The estimated shipment date for RF FinFET Compact (0.8/1.8V) will be 2 days later.

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Mini@sic RUN SCHEDULE 2026 – 65nm ~ 0.13nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS**	Tape-out	Estimated shipment date*
65nm CMOS Logic or MS/RF, GP or LP***	March	10038-LP	TMWB40	14	Nov 25 (2025)	Jan 9	Feb 11	Feb 24	Mar 10	May 22
	April	10039-GP	TMWB41	12	Dec 23	Feb 20	Mar 25	Apr 7	Apr 21	Jul 3
	July	10041-LP	TMWB44	14	Mar 25	May 22	Jun 24	Jul 7	Jul 21	Oct 2
	September	10042-LP	TMWB45	14	May 25	Jul 17	Aug 19	Sep 1	Sep 15	Nov 27
	November	10044-LP	TMWB47	14	Aug 3	Sep 18	Oct 21	Nov 3	Nov 17	Jan 29 (2027)
0.13µm C High Voltage BCD Plus (1.5/3.3/5/10/12/16/20/24/28/36/VG1.5/3.3/5V)	April	10025	TMWB33	12	Dec 23	Feb 13	Mar 03	Mar 31	Apr 14	Jun 18
	November	10028	TMWB36	14	Aug 3	Sep 18	Oct 06	Nov 03	Nov 17	Jan 21 (2027)

* Shipment date is an estimation. Additional cycle time of (1~3 weeks) might be required. See shipment guidelines.

** Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

*** 65nm eFuse is only supported in Fab12. Please select the correct shuttle.

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GUIDELINES FOR SCHEDULE 2026

Design registration guidelines

- Single reservation for multiple chips
- No backup reservation
- Provide single GDS with all designs,
  - Enclosed with TSMC sealring + 80um scribe (post-shrink if applicable).
  - If designs are not identical, put marker in the scribe line.
  - Add dummies to the scribe line for 12-inch tape-outs.
  - Exception: multiple reservations accepted for different projects with different metal stacks or far backend.

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Shipment guidelines

- The estimated shipment date is applicable for reservations with quantity <200 dies.
- If additional samples are required, additional cycle time of (1~3 weeks) might be needed.
- Cycle time estimates are based on typical conditions. Corner wafers or SHDMiM processing requires additional cycle time.
- Optional services adding cycle time
  - Lead free & cupper bumping: 4 days
  - Extra wafer thinning (thinner than 10mils): up to 12 days
  - Additional bumped wafer thinning and die saw (each 200 ea.): 5 working days

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IP Merge Guidelines

- To ensure timely inclusion in the TSMC MPW when an IP merge is required, deliver the final GDS 2 weeks in advance to allow sufficient time for integration and validation.
- Why This Matters:
  - **Complete LVS Setup Required**

    A fully validated LVS setup must be in place before initiating the merge process.
  - **Ip-transfer**

    Third-party IPs have to be transferred from the vendor to the TSMC merge team, which may introduce delays in the process.
  - **Increased Complexity with Multiple IP Instances**

    Merging several IP blocks adds significant complexity and increases the risk of integration issues.
  - **Merge Errors Can Jeopardize the Deadline**

    Errors discovered after merging may delay the process and reduce the likelihood of meeting the MPW schedule. TSMC requests to re-submit the merge even for minor typos or missing files

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Questions?

Contact our teams through a portal support case:

Support Tape-out	For support on the tape-out submission
Support SalesOps	For support on portal, quotations, export documents, purchase orders, and design registration questions
Support EP packaging	For any question related to the Europractice packaging offer.
Support Foundry	For support on foundry libraries, PDK's (installation, flavors, bugs, ...), LVS

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Release notes

- October 24, 2025
  - Release of v1.0 2025
- November 21, 2025
  - Release of v1.1 2025
  - Clarification cycle time information slide 8
- December 11, 2025
  - Release of v1.2 2025
  - Clarification shipment date/ final GDS date and others */**/***
- January 05, 2026
  - Release of v1.3 2025
  - Removed ReRam slide 9
  - Update on 65 nm shuttle availability

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