30 years
Special edition
Discover our history!
ACTIVITY REPORT
2025-2026
EUROPRACTICE

The access point for electronic circuits and systems for 30 years

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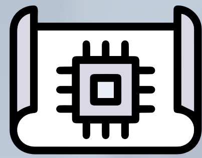
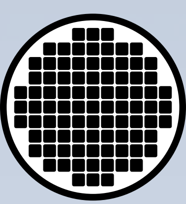
2025 at a glance

753 submitted designs



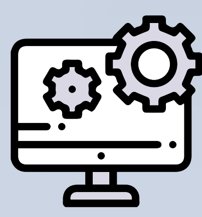
40 training courses

59 webinars on youtube



20 foundries in the technology portfolio

14 design tool vendors



FOREWORD

Dear customers, colleagues and friends,

In 2025, Europractice celebrated three decades of supporting users with easy and affordable access to key services for designing and fabricating electronic circuits and systems. Looking back, we are proud to see how many projects our customers have brought to life through Europractice.

In this edition of our Activity Report, we invite you to explore the **history of Europractice** and its predecessor, EUROCHIP. Through interviews with **Carl Das** (imec) and **John McLean** (UKRI-STFC), you will discover how the first steps were taken to launch this pan-European service—and how it has grown to support more than 600 universities and research institutes.

Last year was special for another reason: the launch of **Europractice 2.0**, a new EU-funded project supported by the Chips Joint Undertaking. This initiative will sustain and extend Europractice services to meet new challenges. Together with **EuroCDP – the EU Chips Design Platform**—we aim to offer complementary services for all European users: Europractice for academia and research, and EuroCDP for startups and SMEs. Our joint ambition is to create a seamless path from academic research to the market.

Europractice MPW services remain open to academic and research institutions worldwide, and we were pleased to see strong results in 2025. Our users submitted **753 designs across 14 foundries**, with TSMC, GlobalFoundries, and IHP leading the uptake. Participation in our training activities was also impressive with 443 delegates attending 40 courses.

We are preparing new initiatives to further lower the barriers to chip design and fabrication. For undergraduate students, we are launching the **ClassIC** initiative—a guided pathway that allows students to design, fabricate, package, and test small, simple circuits with reduced complexity and cost. By combining several student designs on the same die, we aim to give them hands-on experience across key parts of the microelectronics value chain.

We thank all of you—our customers, technology providers, and design-tool suppliers—for being part of this journey.
We look forward to supporting your innovations for the next 30 years.

Your Europractice team at
imec, UKRI-STFC, Fraunhofer IIS, CIME-P, and Tyndall

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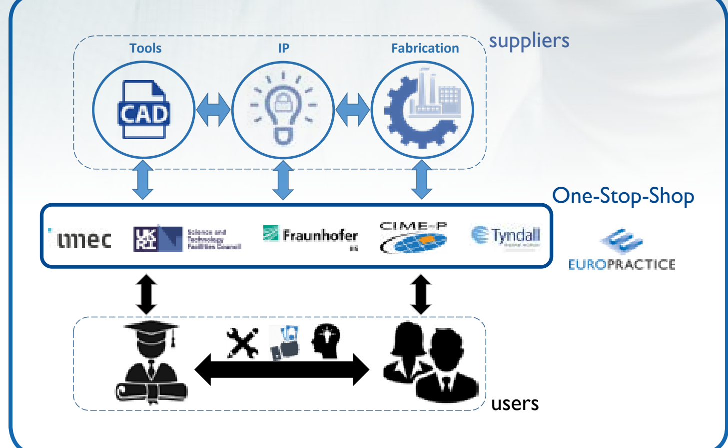
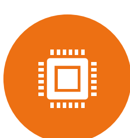
EUROPRACTICE SERVICES

THE ACCESS POINT FOR ELECTRONIC CIRCUITS AND SYSTEMS

For 30 years, Europractice has lowered barriers to a full range of services for designing and fabricating integrated circuits and smart systems. We offer accessible services and strong customer support to our users primarily in Europe – universities, research institutes, and their early-stage spinouts.





FABRICATION SERVICES

Cost-effective fabrication in technologies c leading foundries

DESIGN TOOLS

Affordable access to industry-standard design tools

TRAINING & WEBINARS

Comprehensive training courses on design flows and technologies and free webinars

Europractice acts as a one stop shop, serving as the main interface between users and technology providers. Our suppliers include design tool and IP library vendors, foundries, and assembly and test houses, all offering state of the art, industry grade technologies.

Through this coordinated brokerage service, Europractice supports the growth of a strong microelectronic design ecosystem in Europe. We help universities and research institutes gain affordable, easy access to semiconductor technologies, enabled by negotiated pricing and, importantly, by extensive customer support and comprehensive training.

As a result, Europractice has become a pan European chip infrastructure for design innovation, used by more than 600 academic and research institutions. The service builds on the long-standing experience of five consortium partners: imec, UKRI STFC, Fraunhofer IIS, CIME P, and Tyndall.

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EXTENDING EUROPRACTICE SERVICES

Europractice was launched with the support of the European Commission in 1995 as the successor to EUROCHIP (1989–1995), with the aim of enhancing European industrial competitiveness in the global market. Over the years, the service has evolved significantly, continuously introducing new services and cutting edge technologies in line with global industry trends.

In October 2025, a new project – Europractice 2.0 – started. Funded by Chips JU, it will run for three years to sustain the well established Europractice services and further extend them with new offerings to address emerging challenges and strengthen Europe's semiconductor sovereignty.

Below are some of the key elements that Europractice 2.0 will introduce:

COLLABORATION WITH EUROCDP

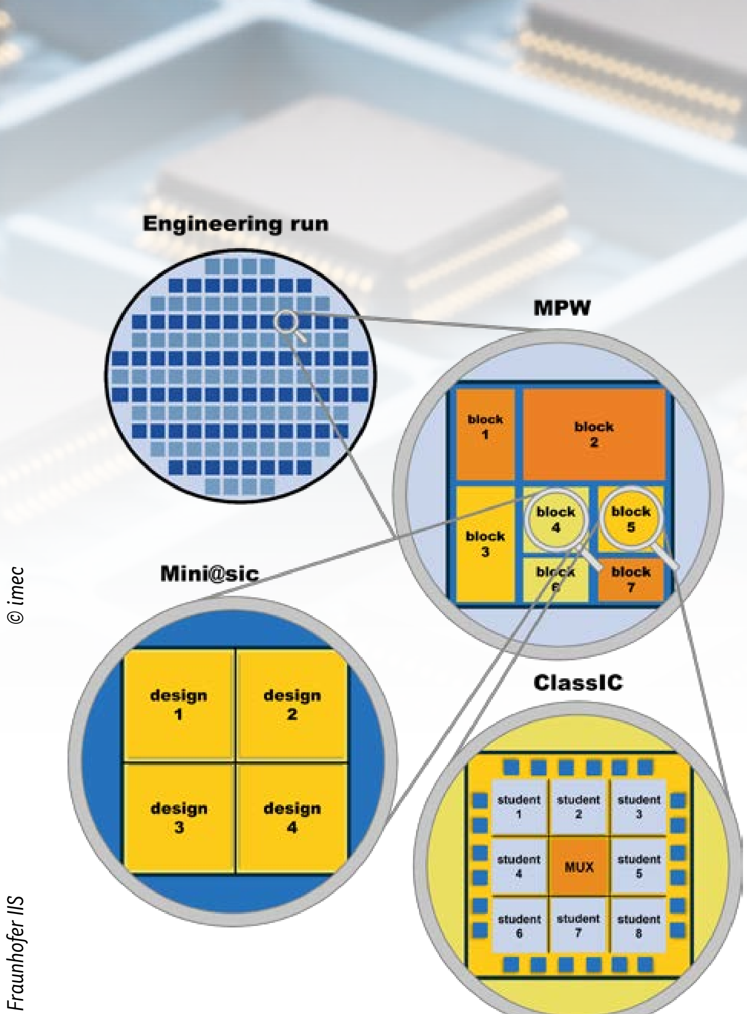
Within Europractice 2.0, we will work closely with the newly launched EU Chips Design Platform (EuroCDP) to ensure complementarity between the two initiatives. Europractice will continue focusing on academia, supporting fundamental research and the training of future engineers, while EuroCDP will concentrate on startups and SMEs. Together, Europractice and EuroCDP will create a clear pathway from education and research to bringing highly innovative products to the market.

DESIGN IP EXCHANGE REPOSITORY

Europractice aims to enhance design efficiency through design reuse by establishing IP exchange repositories. These repositories will allow users to share their IP and access IP contributed by other users. The first repository for freely exchanging microelectronic design IPs has already been created in collaboration with CERN.

HETEROGENEOUS INTEGRATION

Heterogeneous Integration and Chiplet Technologies enable users to combine diverse material platforms and independently optimised device solutions within a single system. Europractice will continue expanding its portfolio to offer technologies that support Heterogeneous Integration. In addition to Micro-Transfer Printing, we now offer four interposer platforms from different providers, each with varying levels of complexity and cost, to better meet user needs.



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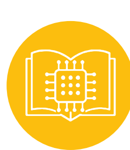
CLASSIC: LOWERING THE BARRIER FOR UNDERGRADUATE STUDENTS

A core mission of Europractice is to help train the next generation of microelectronics engineers. For less experienced users– especially undergraduate students–the step from learning basic concepts to designing and fabricating an integrated circuit can be challenging. To address this, Europractice is developing a new initiative: **ClassIC**.

ClassIC will provide a guided pathway that enables students to design, fabricate, package, and test small, simple circuits with reduced complexity and cost. This will help them develop practical skills through hands-on experience and explore a significant portion of the microelectronics industry value chain.

CAD Tools & PDKs

Students will use design tools and Process Design Kits (PDKs) available via Europractice, including open-source and industry-standard flows.

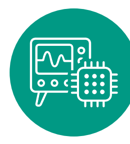


Classware

Europractice will offer modular educational materials, including a step-by-step guide for designing a basic IC. We will also provide pre developed IP blocks that can be incorporated into designs to explore more advanced functionality.

Fabrication

To reduce costs, we will produce a single die–with a common seal ring–that integrates multiple student designed circuits (e.g., operational amplifiers or other IP), each created by a different student.



Testing

To ensure that each circuit can be individually tested, users will have access to several testing options, including multiplexing solutions that allow selective access to each design, as well as dedicated test boards.

We are currently piloting the ClassIC concept with selected universities and plan to launch the full programme by the end of the year.

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AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

Europractice has negotiated lower prices with the major design tool vendors world-wide, as well as with IP and programmable device vendors. Consequently, European academic institutions can access Europractice licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics etc.) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the Europractice service provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current Europractice network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows our customers to participate in EC-funded projects, ranging from IP block and component design to the design of complete systems.

Design tools for academic spinouts

Spinouts of European universities can access certain design tools at low cost via Europractice in order to produce a proof-of-concept IC to demonstrate their IP/product. The resultant IP can then be fully commercialized for an additional agreed fee. The spinout gains access to an industry-standard full IC design flow, suitable for all IC technologies.

Europractice also supports commercialisation of academic designs to facilitate effective innovation. We have mechanisms in place for an academic institute that has developed a design using Europractice tools and subsequently wishes to exploit it commercially, either via a spinout or by transferring the IP to an existing company.

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EASY ACCESS TO PROTOTYPING

Obtaining access to semiconductor fabrication lines is often difficult for academic and research institutions. Their prototype designs typically require only very small production volumes, making it difficult—or simply impossible—to engage directly with large foundries. Even when access is possible, the manufacturing costs can be prohibitively high.

Europractice addresses this barrier by offering cost effective routes to fabrication through Multi Project Wafer (MPW) runs for prototyping and Multi Level Mask (MLM) services for small volume production. These shared cost services drastically reduce expenses and make state of the art technologies accessible to small users.

TECHNOLOGY PORTFOLIO

Today, Europractice provides access to nearly 90 technologies from more than 20 foundries, pilot lines, and other manufacturers. A strong focus is placed on European-based suppliers, as 17 of them have manufacturing facilities in Europe.

Open-source technologies

Europractice now supports the fabrication of designs created with open source PDKs. Users can prototype using platforms such as GlobalFoundries' 180 nm MCU and IHP's SG13C and SG13G2, available through the Europractice service.

MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto the same mask set of a prototype run, known as Multi-Project-Wafer (MPW) run, the high cost of the mask set and the fabrication process is shared among the participating customers.

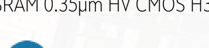
Fabrication of prototypes can therefore be as low as 5% to 10% of the cost of a wafer run for only one dedicated customer. A limited number of IC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time". To achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the designs fabricated for educational purposes are much smaller than the minimum block size on regular MPW runs, the concept of **mini@sic** was introduced in 2003. This solution allows to further lower prototype fabrication costs compared to standard MPW runs. The mini@sic principle is based on the following methodology: Several times per year, a foundry standard MPW block is bought and resold in smaller and cheaper sub-blocks or mini@sics. This program has been extended over the years and currently includes selected technologies from GlobalFoundries, IHP, TSMC, UMC and X-FAB.

TECHNOLOGY PORTFOLIO 2026

ams OSRAM

- ams OSRAM 0.18µm CMOS atC18C 1.8V/3.3V
- ams OSRAM 0.18µm CMOS atC18D 1.8V/5.0V
- ams OSRAM 0.35µm CMOS C35B4C3
- ams OSRAM 0.35µm CMOS C35OPTO
- ams OSRAM 0.35µm HV CMOS H35B4D3
- ams OSRAM 0.35µm HV CMOS H35OPTO



- EM 110nm CMOS ALP011 logic

- GF 180nm MCU (open-source)
- GF SiGe 8XP
- GF 130nm BCDlite-Gen2
- GF 55nm BCDlite 55nm BCDlite
- GF 45nm SPCLO Si-Photonics
- GF 45RFSOI
- GF 45RFE
- GF 28nm SLPe
- GF 22nm FDSOI
- GF 12nm LP+

- IHP SG25H7_EPIC (BiCMOS + Photonics)
- IHP SG25 PIC (Photonics)
- IHP BEOL SG13
- IHP SG13C 0.13µm SiGe:C (open-source)
- IHP SG13S 0.13µm SiGe:C
- IHP SG13S + MEMRES Module + RDL
- IHP SG13SCu FEOL + Cu BEOL option
- IHP SG13G2 0.13µm SiGe:C (open-source)
- IHP SG13G2 0.13µm BiCMOS/CMOS
- IHP SG13G2 0.13µm SiGe:C + RDL
- IHP SG13G2Cu FEOL + Cu BEOL option
- IHP SG13G3 0.13µm SiGe:C
- IHP SG13G3Cu 0.13µm SiGe:C

- ST 28nm CMOS28FDSOI
- ST 28nm CMOSP28FDSOI
- ST 55nm BiCMOS055X
- ST 65nm CMOS065
- ST 90nm C090D
- ST 130nm HCMOS9A
- ST 130nm BiCMOS9MW
- ST 0.16µm BCD8sP
- ST 0.16µm BCD8s-SOI

- TSMC 0.13µm BCD+ (12")
- TSMC 0.13µm CMOS Log/MS/RF (G, LP)
- TSMC 90nm CMOS Log/MS/RF (G ,LP)
- TSMC 65nm CMOS Log/MS/RF (G, LP)
- TSMC 55nm CMOS Log/MS/RF (G, LP, ULP)
- TSMC 40nm CMOS Log/MS/RF (G, LP)
- TSMC 28nm CMOS Log/RF HPC/HPC+
- TSMC 22nm CMOS Log/RF ULL (ReRAM)
- TSMC 16nm CMOS Log/RF FinFET Compact
- TSMC 7nm CMOS Log/ RF FinFET

- UMC L180 Logic GII, MM/RF
- UMC L110AE Log/MM/RF
- UMC L65N Log/MM/RF (LL)
- UMC 40N Log/MM – LP
- UMC 28N Log/MM – HPC

- X-FAB XH035 0.35µm HV
- X-FAB XH035 Noble Metal
- X-FAB XH018 0.18µm HV NVM E-Flash
- X-FAB XT018 0.18µm HV SOI
- X-FAB XS018 0.18µm OPTO
- X-FAB XP018 0.18 µm NVM
- X-FAB XR013 0.13µm RF SOI/XIPD
- X-FAB XT011 0.11µm HV SOI
- X-FAB XMB10 MEMS
- X-FAB XG035 0.35µm GaN-on-Si

- AMF Si-Photonics

- CEA-leti Si-Photonics Si-310
- CEA-Leti SiN-Photonics Si_3N_4-800
- CEA-Leti MAD300 22nm NVM
- CEA-Leti Lumik

- CN Si-Photonics 220 passives/actives
- CN Si-Photonics 340 passives
- CN Si-Photonics 500 passives
- CN SiN-Photonics
- CN Suspended-Si
- CN Ge-on-Si
- CN Si-Photonics Visible SiN 200

- 4H-SiC CMOS High Temperature Technology

- Graphenea PF1 – General
- Graphenea PF2 – Biosensing
- Graphenea PF3 – HKMG

imec

- imec GaN-IC on SOI 100V/ 650V
- imec Si-Photonics Passives+
- imec Si-Photonics iSiPP50G
- NanoIC imec P-PDKs: N2, A14, eDRAM

- Glass microfluidics

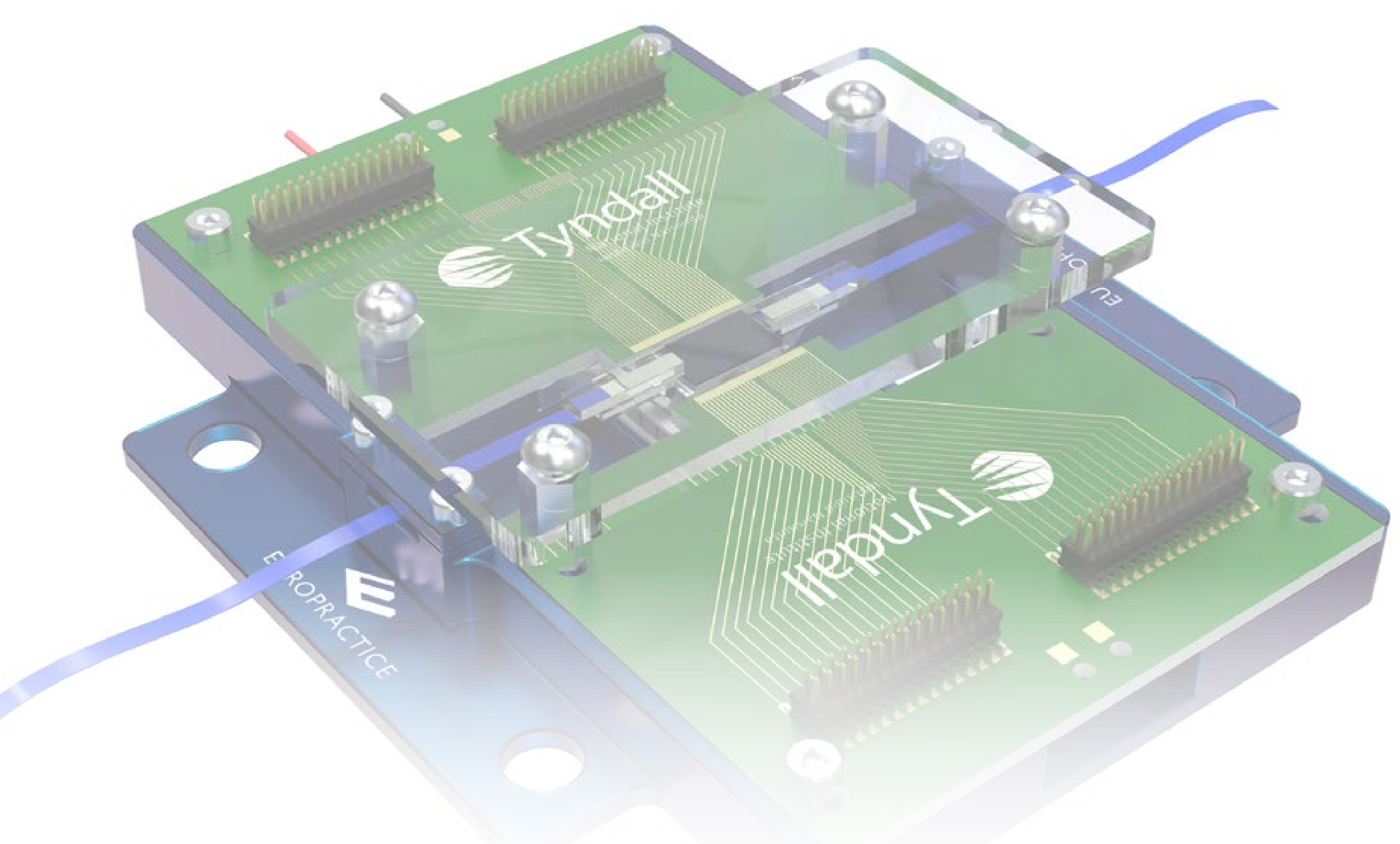
- Pragmatic FlexIC Platform Gen 3

- Science MEMS Poly
- Science MEMS SOI
- Science MEMS Piezo

- SINTEF Thin-Film PiezoMEMS

- Glass-Photonics IC ioNext-NIR
- Glass-Photonics IC ioNext-VIS
- Glass-Photonics IC WAFT

- UMS GH25 0.25µm GaN HEMT
- UMS GH15 0.15µm GaN HEMT
- UMS PH10 GaAs pHEMT
- UMS BES|GaAs pHEMT
- UMS ULRC-20|GaAs



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MULTI-LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi-Level Mask (MLM). With this technique the available mask area (for example 20mm × 20mm field for stepper equipment) is typically divided in four quadrants (4L/R : four layers per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is therefore reduced by a factor of four. By adapting the lithographical procedure, it is possible to use one mask four times for the different layers by using the appropriate quadrants. This technique allows to significantly decrease the mask costs.

The advantages of using MLM single user runs are:

- lower mask costs
- an MLM run is organized for one customer
- it can be scheduled for any date since it does not depend on regular MPW runs
- a customer receives a few wafers, resulting in a few hundreds of prototypes

The MLM technique is preferred over MPW runs when the chip area becomes large and when the customer would like to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low-volume production.

MLM runs are available for technologies from IHP and X-FAB.

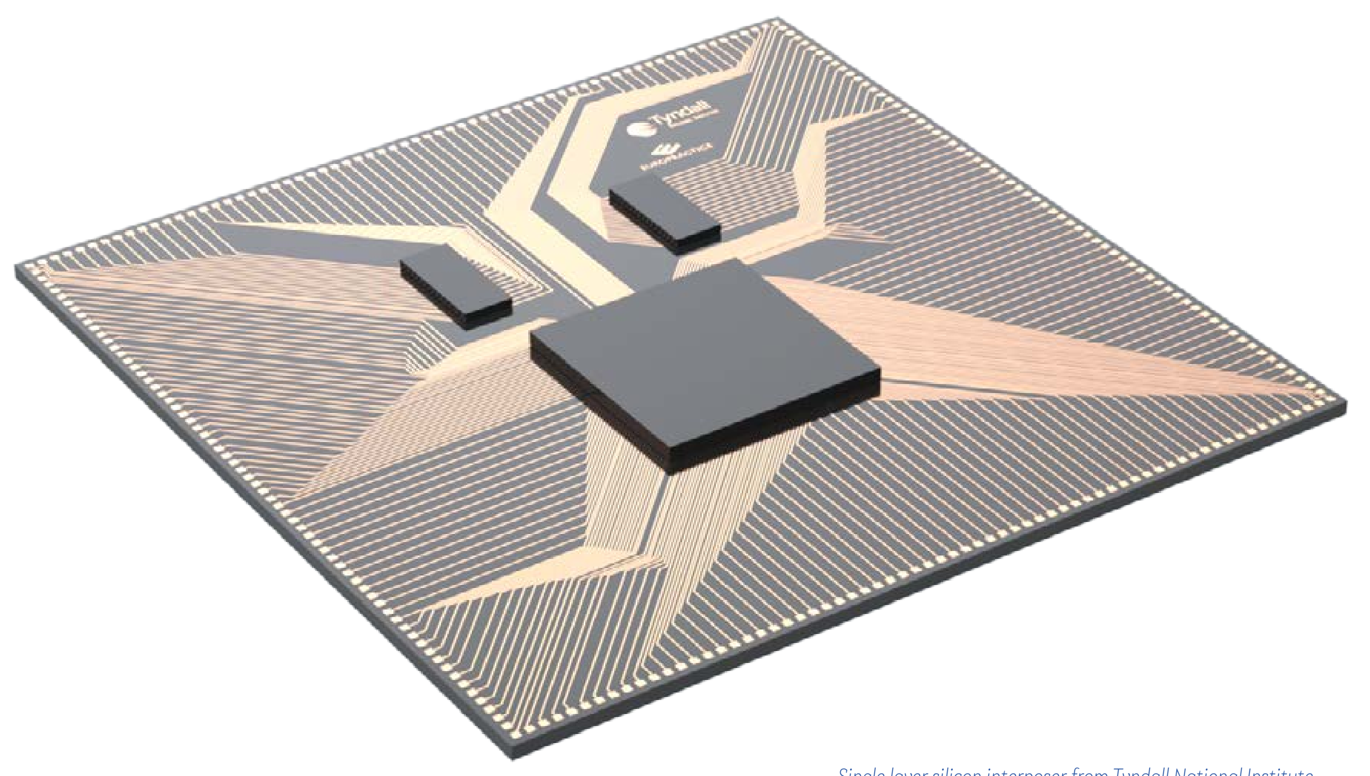
PACKAGING

Prototypes fabricated through Europractice are delivered unpackaged and untested as standard. For customers requiring packaged solutions, we provide a cost-effective, flexible, and coordinated packaging service through industrial-qualified packaging houses. A broad range of ceramic and plastic packages is available, including DILs (Dual-in-line), PGAs (Pin Grid Array), and QFNs (Quad-Flat No-leads). In addition to standard options, Europractice offers customized solutions and supply chain management to meet specific customer needs.

MULTI-PROJECT PACKAGING

Following the introduction of Multi-Project Packaging (MPP) for Photonic Integrated Circuits (PICs), Europractice continues to expand this service. Similar to MPW runs, MPP follows a scheduled approach to PIC packaging, leveraging standardized photonic package designs and processes. The service supports PICs requiring fiber coupling via grating couplers, edge couplers, or single-lensed fibers.

By using standardized packages and scalable processes, such as those defined in our Photonics Packaging Design Rules, MPP reduces cost barriers and turnaround times for PIC packaging while providing a path to volume production. This approach enables Europractice users to access advanced photonic packaging without prohibitive costs.



Single layer silicon interposer from Tyndall National Institute.

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CHIPLETS & SYSTEM INTEGRATION

The demand for advanced packaging and system integration remains strong, driven by applications requiring higher functionality in system-on-chip (SoC) and system-in-package (SiP) solutions. Europractice is expanding its portfolio to enable users to realize complex multi-technology devices that scale from prototypes to volume manufacturing.
Our offering includes specialized processes, such as 2.5D/3D integration of electronic and photonic ICs through die stacking techniques, using pick-and-place, flip-chip, BGAs, Cu pillars, wafer-level fan-out packaging, and silicon interposers.

Micro Transfer Printing (MTP) is a key technology for **Heterogeneous Integration**, allowing devices to be transferred from their native substrate to a different host material at die or wafer level, supporting scalability to high-volume production. In 2025, we strengthened our optical chiplet integration capabilities with etched-facet InP lasers and high-speed photodiodes printed onto silicon substrates. Users can evaluate these transfer-printable lasers on a standard silicon submount or provide their own compatible platform.

Interposers

Interposers continue to play a critical role in chiplet-based architectures, enabling high-performance interconnections between multiple chiplets. Europractice offers interposer technologies from leading manufacturers, such as GlobalFoundries, ams OSRAM, and IHP, in addition to the custom silicon interposer offered by Tyndall, to support users in adopting chiplet-based designs.

In 2025, we have introduced a single-layer silicon interposer solution for integrating multiple electronic ICs on a common silicon platform. This service includes customized tracking layout design, fabrication of the silicon interposer, and design and fabrication of a standard PCB. Manufactured in Tyndall's cleanroom on 100 mm wafers, each interposer measures 30mm × 30mm × 0.5mm and supports up to 260 DC-only connections via 1 µm gold-metallized tracks. This fabrication service complements our Electronic IC Integration onto Silicon Interposers and Module Packaging service, delivering a complete solution for advanced electronic integration.

TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

Europractice provides training courses targeting academic staff and PhD students from European universities and research institutes. Unlike training courses which address single topics or individual design tools, the Europractice training courses typically address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow.

Since the courses are based on the Europractice design tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the Europractice infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants have an opportunity to extensively practice the concepts described in lectures, and have access to experts who can answer questions about the concepts, design tools or technology processes discussed on the course.

Where a design flow is well supported by multiple vendors and/or processes, multiple course variants are offered that reflect the typical practice within European industry.

Over the last year, 40 courses provided training to 443 delegates, with 198 of these delegates being PhD students, many of whom will go on to become future industry and academic leaders.

A highlight of 2025 was the second edition of the Europractice Summer School. This was a comprehensive one-week-long training event that introduced participants into the world of IC design. We were delighted to welcome more than 100 participants who joined us at imec in Leuven, Belgium.

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WEBINARS

To introduce the constantly growing service portfolio and share valuable technology insights, Europractice regularly develops and hosts highly successful webinars. These online events usually include informative presentations given by experts from world-leading companies, foundries or academic institutions, followed by a short Question & Answer session. All webinars are free of charge and open to a broad audience with different backgrounds.

In the past year, we hosted several webinars. Here are some highlights:

Introduction to X-FAB technologies

In this six-webinar series, X-FAB experts present the key features of selected processes available through Europractice. Each session focuses on one technology—from sensors to photonics and GaN—its unique capabilities, and the applications it enables.

New services in Europractice

We regularly hosted webinars introducing new technologies and services added to the Europractice portfolio, including Micro Transfer Printing, Chiplet Integration, SINTEF's PiezoMEMS, and Pragmatic Semiconductor's next generation FlexIC platform.

59 videos with our recorded webinars are available on the official YouTube channel of Europractice Services, covering different technologies: Microfluidics, MEMS, Flexible Electronics, Graphene, Silicon-Photonics, advanced Photonics packaging and more.

Europractice webinars remain highly popular. Last year, the live-stream sessions were attended by over 100 delegates each.

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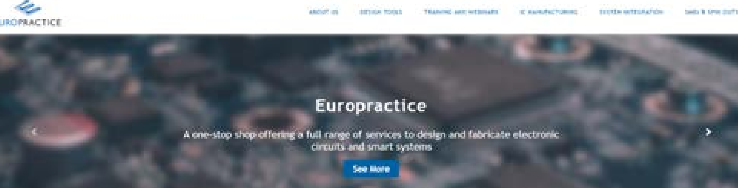
COMMUNICATION AND OUTREACH

At Europractice, we use a wide range of communication channels to increase awareness about our services and deliver the latest updates to both existing and potential users. Among online platforms, our web portal and social media channels play a primary role.

WEB PORTAL

The **General Portal** europractice.com is the main entry point for Europractice services, where you can find all the information you require.



For further details on one of the aspects of our portfolio, the portal will redirect you to:

- **Design Tool & Training website** europractice.stfc.ac.uk with the latest information related to Europractice membership, purchase of design tool licenses, upcoming training courses and webinars;
- **Technology & Fabrication website** europractice-ic.com with detailed information on the MPW offer, run schedules, and pricing.

SOCIAL MEDIA

We are happy to see that our Europractice community on LinkedIn and YouTube is growing. Following our accounts is a great way to stay informed about the latest service portfolio additions and share your experience with Europractice.

On LinkedIn, we do not just publish announcements of new technologies and services, but we also give visibility to our customers by publishing their testimonials and technical user stories. At the beginning of 2026, our LinkedIn community counted nearly 5.500 followers.

The YouTube channel Europractice Services gives a great opportunity to watch our webinar recordings that cover a wide technology range. In February 2026, the channel had approximately 110K views and more than 2.2K subscribers.

LinkedIn announcement of our workshop at ESSERC 2025

Europractice book display at ISSCC 2025

Europractice team at EFECS 2025

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CONFERENCES AND EXHIBITIONS

Every year, the Europractice team participates in various scientific conferences, industrial trade shows and fairs to present our services to existing customers and to attract new prospects.

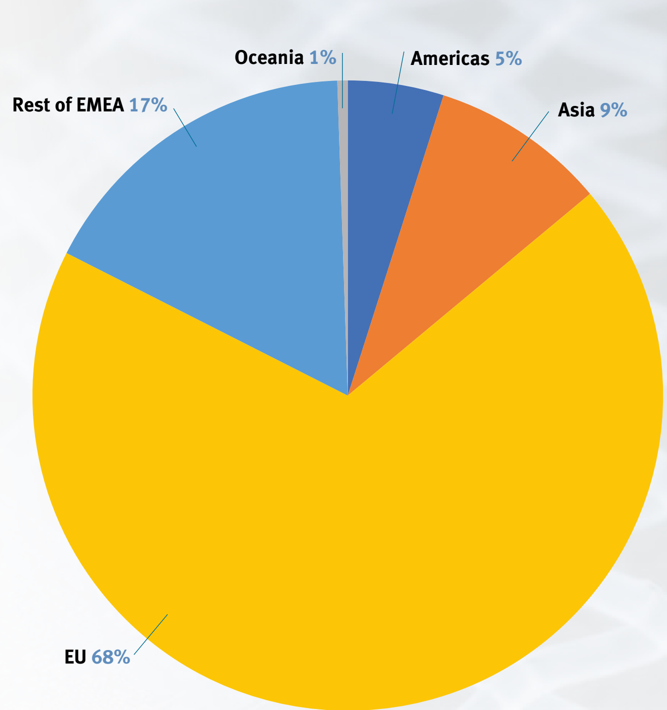
In 2025, we were present at more than 20 events. For priority events, our consortium members delivered talks and staffed dedicated booths using promotional material designed in the well-recognisable bright-colour palette of Europractice.

We also continued organizing Europractice workshops at prominent European conferences. At ESSERC 2025, we hosted a second edition of the workshop "Tips and Tricks for a Successful Multi-Project-Wafer (MPW) Chip" to give a hand to less experienced MPW users.

In 2026, we will attend at least the following conferences and fairs:

SMACD 2026	Dresden, Germany	29 June - 2 July
ESSERC 2026	Palma de Mallorca, Spain	7-10 September
PRIME 2026	Berlin, Germany	20-23 September
EFECS 2026	Helsinki, Finland	December 2026
ISSCC 2027	San Francisco, US	14-18 February 2027

RESULTS 2025: MPW PROTOTYPING



Geographical distribution of MPW designs in 2025

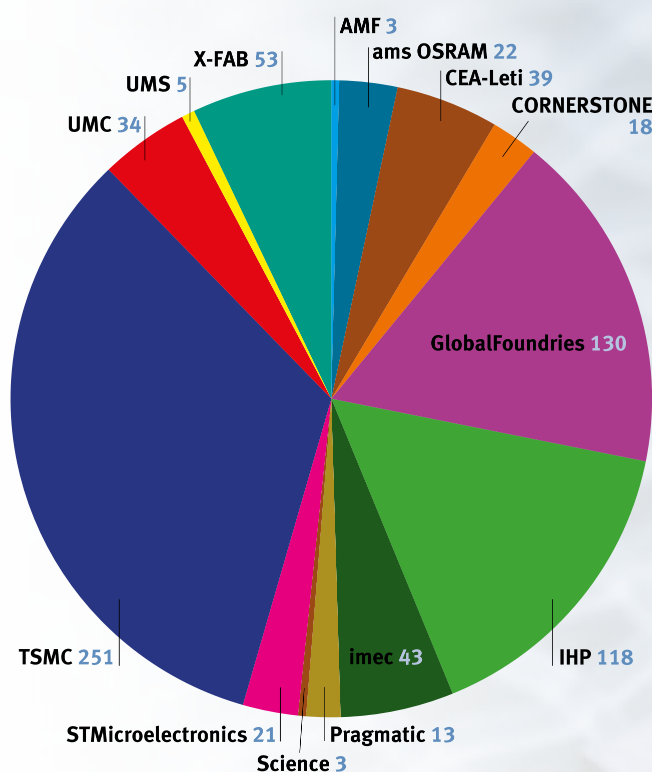
EUROPRACTICE MPW SERVICES

In the constantly evolving semiconductor landscape in Europe, the scope of Europractice services continues to adapt. Europractice Multi-Project Wafer (MPW) services will focus on supporting the following groups of users, in line with our mission to advance microelectronics education and research and to train the next generation of engineers:

- Europractice member institutions—universities and research institutes within the EU and the wider EMEA region (Europe, Middle East, and Africa). This remains our core audience.
- Academic and research institutions worldwide.

At the same time, European SMEs and startups will be supported through the recently launched EU Chips Design Platform (EuroCDP), ensuring that all customer groups in Europe receive tailored and appropriate services.

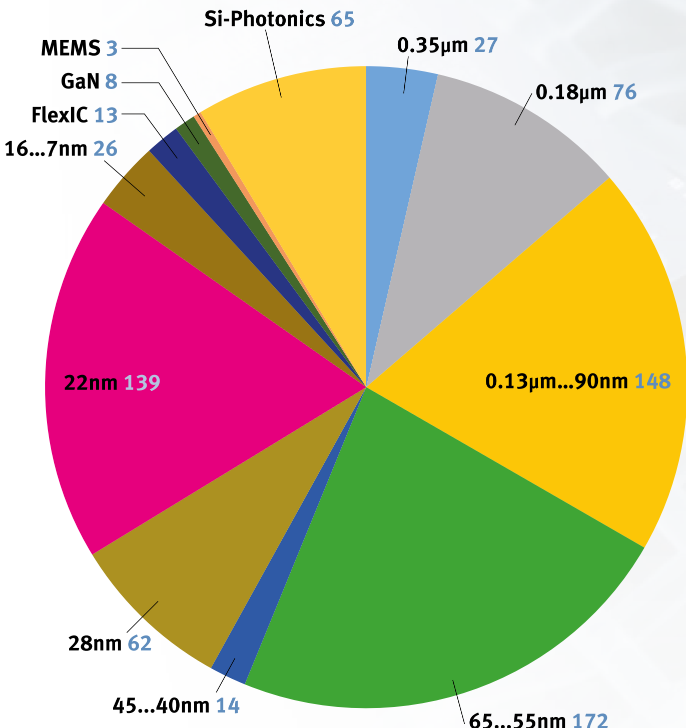
In line with this focus, **753 designs were fabricated through Europractice MPW services in 2025** by users from academic and research institutions worldwide. The majority came from Europe: **85%** of all designs originated from Europractice member institutions in the EU and the rest of the EMEA region. A smaller share of users came from Asia (**9%**), the Americas (**5%**), and Australia (**1%**), indicating continued global interest while maintaining a strong European focus.



Number of fabricated designs in 2025 per foundry

ACCESS TO MULTIPLE FOUNDRIES

In 2025, Europractice users fabricated designs in **14 different foundries**. The top three by the number of submitted designs remained unchanged from the previous year: TSMC, the global industry leader; GlobalFoundries, with its widely adopted 22FDX technology; and IHP, whose open-source PDKs continue to gain traction. These were followed by the European foundry X-FAB and the research centres imec and CEA-Leti, which also attracted a steady number of academic designs.



Number of fabricated designs in 2025 per technology (node)

UNPARALLELED TECHNOLOGY MIX

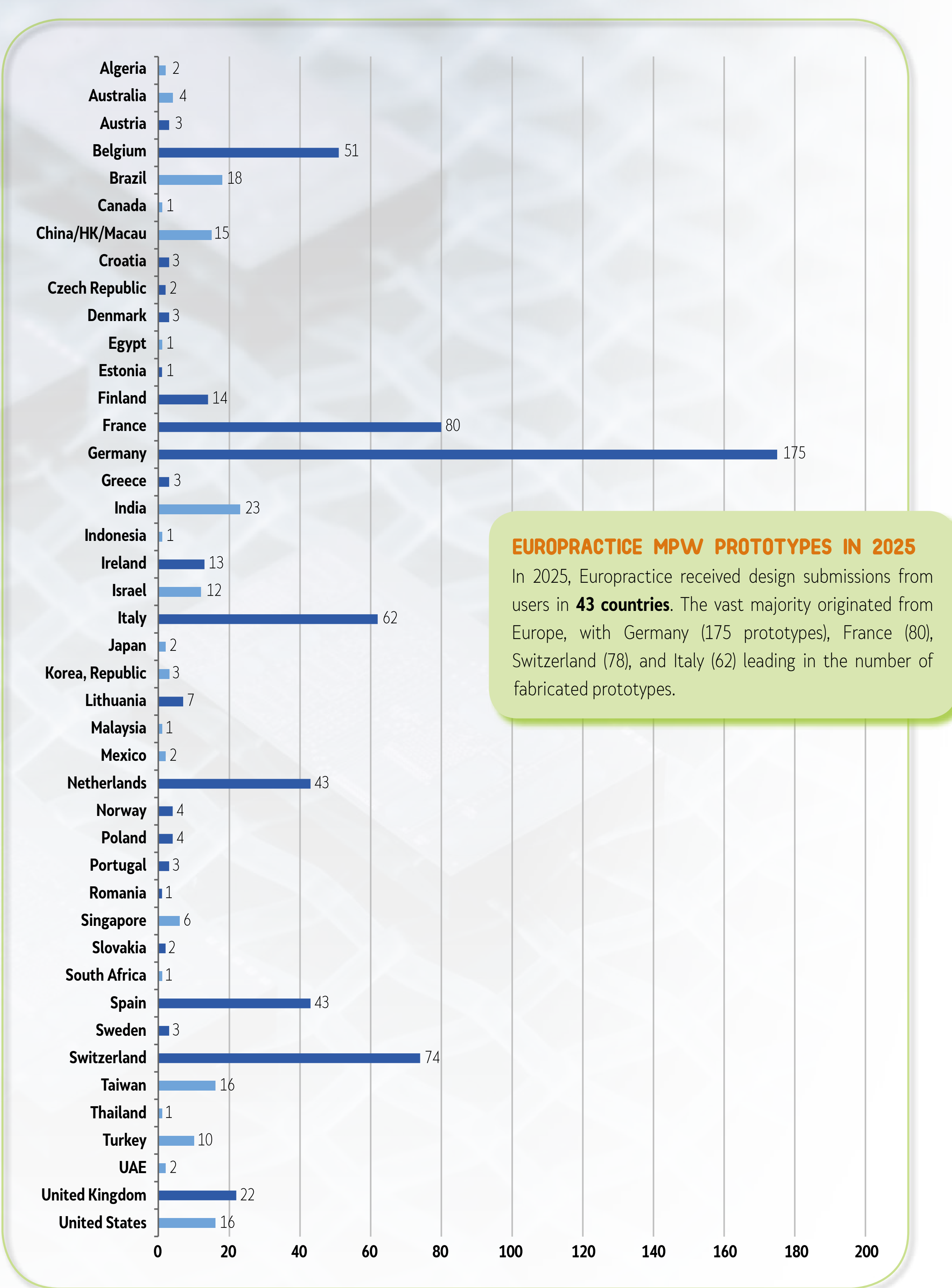
Europractice lowers the barrier for accessing a very diverse range of technologies, spanning advanced nodes, mature nodes, and More-than-Moore platforms.

One third of Europractice users still rely on mature, cost-effective technologies with nodes between **0.11µm and 0.35µm**.

The second most frequently used group includes nodes **from 28 nm to 22 nm**. The strong growth in 22-nm uptake is driven not only by GlobalFoundries' 22FDX technology (95 submitted designs) but also by the introduction of CEA-Leti's MAD300 (Memory Advanced Demonstrator) platform, which enables the integration of Resistive RAM (OxRAM) at the back-end-of-line on GF's 22FDX process (39 submitted designs). Designs in the 28-nm range are mainly implemented in TSMC's HPC(+) technologies.

Between these two categories, the **65 nm** technology and its associated nodes remain an important option, with 172 prototypes fabricated.

Europractice continues to support users transitioning to advanced nodes. In 2025, four universities prototyped for the first time in the smallest node offered by Europractice: **TSMC's 7nm FinFET**.



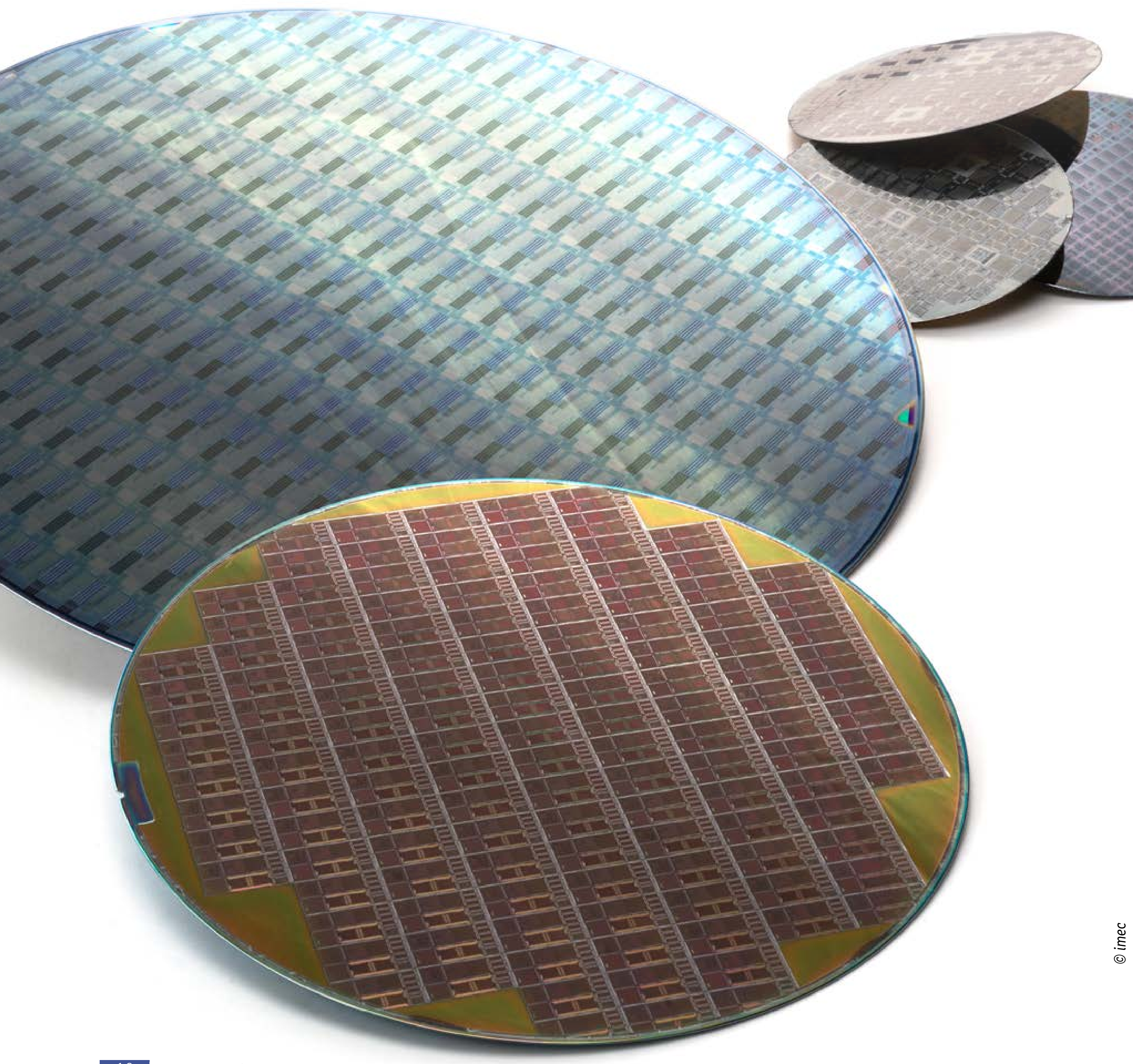
EUROPRACTICE MPW PROTOTYPES IN 2025

In 2025, Europractice received design submissions from users in **43 countries**. The vast majority originated from Europe, with Germany (175 prototypes), France (80), Switzerland (78), and Italy (62) leading in the number of fabricated prototypes.

HOW DID EUROPRACTICE BEGIN 30 YEARS AGO?

We spoke with Carl Das and John McLean, who were there from the very beginning and helped launch and shape Europractice services.

Join us for a three decade dive into our history.



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From EUROCHIP to Europractice: Pioneering Affordable Access to Chip Design and Fabrication in Europe

You might have heard about the EU Chips Act – Europe's joint effort to increase its sovereignty and competitiveness on the global semiconductor market. A key part of achieving this ambitious goal is training the engineers of tomorrow, who are essential to sustaining an advanced microelectronics ecosystem. But this priority is not entirely new. In the past, Europe already undertook initiatives to strengthen microelectronics education and research across the continent. Without those early efforts, Europractice – with its current scale, broad offer, and large user base – would not be possible.

Our story begins in 1989, when the EC launched the VLSI Design Training Action to help European universities train students in VLSI design. Carl Das was at the heart of these events. He was one of the founders of the fundamental service that, to this day, continues to lower the barrier to chip design and fabrication, enabling microelectronics research and education across Europe. Of course, we are talking about Europractice – but not only. In the beginning was EUROCHIP.

Carl Das studied electrical engineering at KU Leuven, where he specialized early in the emerging domain of microelectronics. He joined INVOMEC (later part of imec) in 1984. Four years later, Carl took on responsibility for the Foundry Working Group within the EUROCHIP initiative, coordinating fabrication services for European academic users. Since 1995, he has served as Chairman of Europractice, guiding the long-term development of the service and helping establish its role as a key European framework for accessible microelectronics design and prototyping.

Carl, our story begins more than three decades ago. Take us back in time. What did microelectronics education and research look like at the end of the 1980s?

Carl Das: At that time, Silicon Valley was the centre of rapid microelectronics innovations. Some of my European colleagues would go there, complete their PhD, and then return to teach at local universities. They sometimes had to teach a completely new course every year – that is how quickly things were evolving. Overall, Europe faced a serious challenge. Universities simply didn't have access to modern IC design tools or affordable ways to fabricate chips. Industry was warning that without proper training, Europe risked falling behind. The European Commission responded with the VLSI Design Training Action, and EUROCHIP became its flagship program.

How did EUROCHIP address this challenge?

Carl Das: The idea was simple but ambitious: select 50 universities and provide them with a lecturer post, state-of-the-art IC CAD tools, affordable MPW prototyping services, and IC testing possibilities. This was a bold move to ensure Europe could compete globally in microelectronics.

EUROCHIP was a collaborative effort of several existing MPW centres in Europe. GMD in Germany coordinated the service together with imec in Belgium, RAL in the UK, DTU in Denmark, CMP in France, and later CNM in Spain. This network gave the program real strength and ensured universities could access industrial-grade resources.

The offer was comprehensive: four major CAD packages for IC design, standard cell libraries, and three CMOS technologies (3µm, 2µm CMOS), complemented by comprehensive training courses. The first designs were taped out as early as 1990—a big milestone that showed the concept worked.

And the results were beyond expectations. In addition to the 50 universities that could benefit from EUROCHIP services for free, demand exploded—another 68 universities joined on a pay-as-you-use basis, and by 1995 around 400 institutions were actively designing ICs. This was the first time universities from all over Europe could work with the same industry-standard tools and technologies—a true game-changer for microelectronics education that prepared thousands of students for careers in industry. In addition, students and researchers from different universities could easily collaborate on European-funded research projects using the same CAD tools and technologies.

It laid the foundation for Europractice, which took the vision even further. Without EUROCHIP, Europractice as we know it today would not exist.

A EUROCHIP training poster.

EUROCHIP was clearly a success. How did it evolve into Europractice?

Carl Das: By 1995, EUROCHIP had achieved its mission–hundreds of universities were designing chips, and Europe had a strong educational infrastructure. But the landscape changed quickly. Universities wanted access to newer, more advanced technologies, while small companies and startups were asking for low-cost prototyping and small-volume production. They had ideas, but not the budgets for full commercial pricing.

Therefore, the objective was to broaden the scope: keep supporting universities but also open the door to industry.

At the end of the EUROCHIP phase, the ChipShop consortium was already offering similar services to industry, especially SMEs. When the European Commission launched the next call, the goal became to bring both worlds together. Partners from the ChipShop consortium joined forces with the EUROCHIP partners, and that is how EUROPRACTICE was formed – a service that could support both academia and industry.

Who were the partners in the new Europractice consortium?

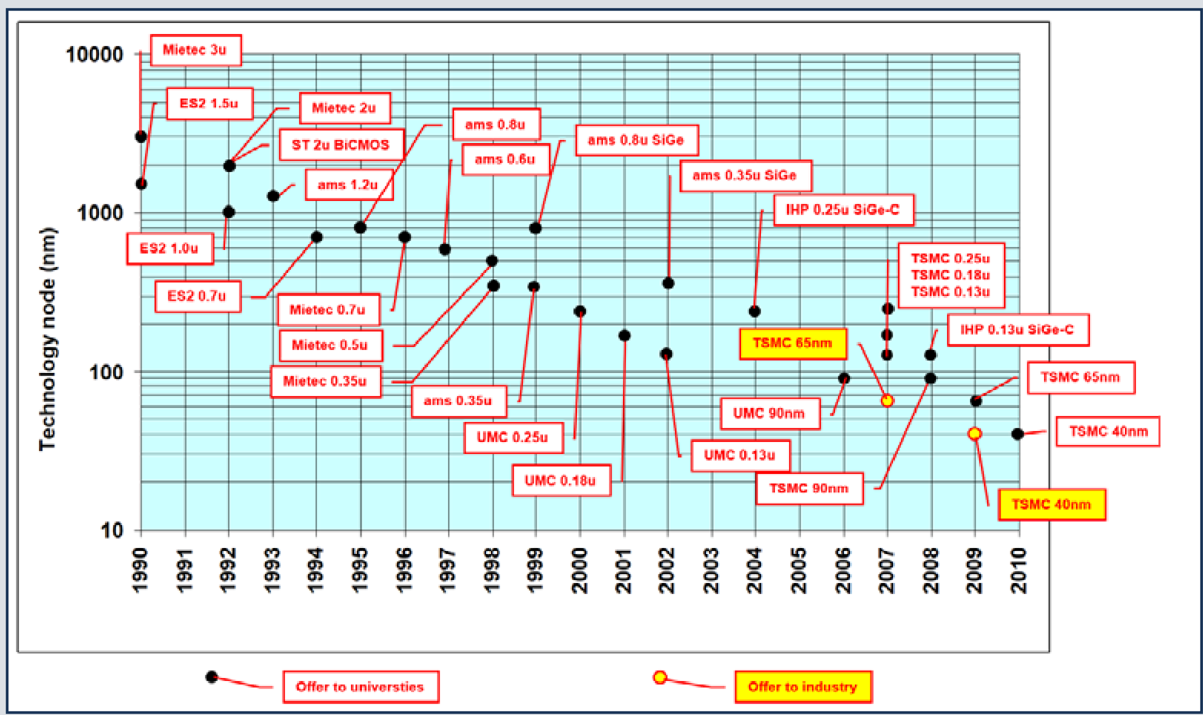
Carl Das: The new consortium combined the long-standing academic coordinators with partners who had industrial experience. At first, the core EUROCHIP partners, imec and RAL, joined forces with Fraunhofer IIS in Germany, Nordic VLSI in Norway, and Delta in Denmark. Later, by 2000, as the business model evolved, the operational consortium stabilised around imec, Fraunhofer IIS, and RAL. Broadly speaking, the first two partners focused on fabrication services, while RAL supported users with design tools and training.

How did you work on expanding the fabrication technology portfolio?

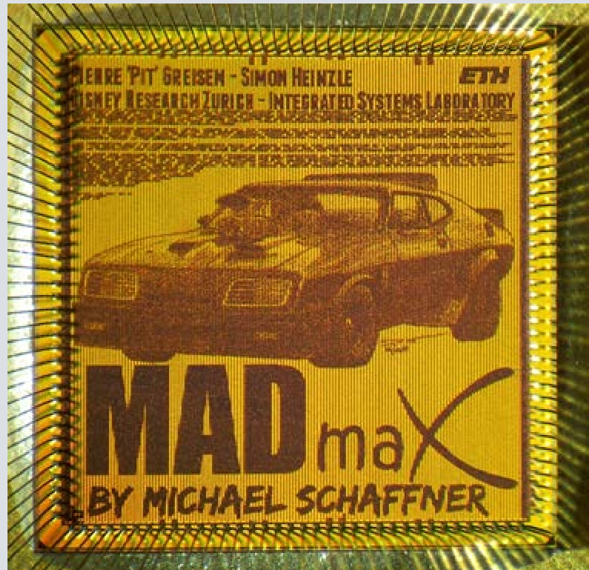
Carl Das: With Europractice, the technology offering became much broader: Universities needed access to more advanced nodes, and companies needed technologies suited for real products.

In the first years of Europractice, we started by extending the portfolio with 0.8 µm down to 0.25 µm CMOS, and then further into BiCMOS, SiGe, high-voltage options, and other specialised processes. We also introduced FPGA and MEMS technologies. Readers today may smile at calling these technologies 'advanced'. But back in the day, they were considerable steps forward.

We always prioritised European foundries where possible. But then something remarkable happened: both the leading Taiwanese foundries, TSMC and UMC, approached us. They saw the value in enabling European universities and SMEs to use their technologies. TSMC reaching out was truly significant – an acknowledgment that the European academic and SME ecosystem mattered globally.



Early evolution of the technology portfolio (1890-2010) with the focus on European academia.



Example of a chip fabricated at ETH Zurich in 2012, using the UMC 65nm technology, accessed via Europractice.

Utilising new technologies is not trivial. Did users receive help adopting advanced solutions?

Carl Das: Absolutely. As soon as we introduced 90 nm and below, it became clear that cost was not the only barrier – design know-how was just as important. Many universities lacked experience with deep-submicron design rules or new verification flows.

To help them, the European Commission funded dedicated training actions. IDESA focused on deep-submicron IC design challenges and provided hands-on tutorials using the very tools and technologies available via Europractice, while STIMESI played a similar role for MEMS, offering short courses at universities across Europe to teach the practical aspects of microsystems design and fabrication.

These projects ensured that universities weren't just accessing advanced technologies for the time – they were actually capable of successfully designing in them.

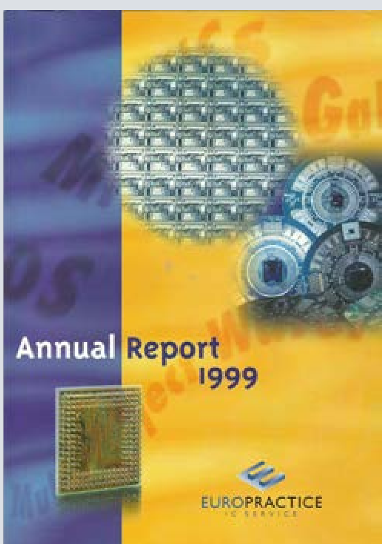
And to lower barriers even further for prototyping in advanced technologies, you introduced mini@sic – correct?

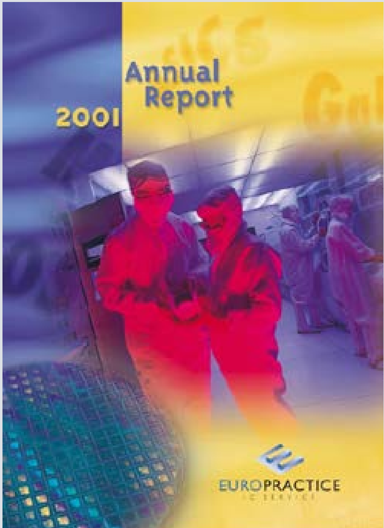
Carl Das: Yes. Even with training and subsidies, deep-submicron MPW participation was still expensive for many universities. The minimum block sizes offered by foundries were simply too large, and therefore too costly.

So we introduced the mini@sic concept: we subdivided the minimum MPW block into several smaller blocks, allowing universities to buy just a fraction of the usual area. That made advanced, more expensive technologies suddenly accessible to a much wider group of users. And the effect was immediate – design submissions increased noticeably as soon as mini@sic was introduced.

mini@sic is, of course, only one example. Would you say that the core concepts you introduced early on still define Europractice today?

Carl Das: If you look at Europractice today, the principles are exactly the same as in 1989: make cutting edge microelectronics accessible, affordable, and easy to use for every university and research institute in Europe. The technologies have changed beyond recognition – and we certainly no longer work with punch cards – but the impact remains just as big: a single, integrated one stop shop that allows students, researchers, and innovators to design the chips of the future with the same tools and flows used in industry.





Europractice activity reports - a long-standing tradition.

Building Pan-European Design-Tool and Training Services to Empower the Engineers of Tomorrow

Training the next generations of microelectronics engineers is one of Europe's strategic priorities. To prepare students for an industry defined by rapid innovation cycles, it is essential to give them access to the full design to fabrication journey: the possibility to create their own integrated circuits, to test ideas in silicon, and to work with the same tools and technologies used in leading semiconductor companies. Only then will the graduates be equipped with the skills and confidence the market expects. This mission has always been at the heart of Europractice.

From the very beginning, achieving this ambition required close collaboration among the consortium partners, each assuming clear responsibilities within the broader service. UKRI STFC, a major UK research organisation, became the home of Europractice's design tool service and the lead partner for training activities. John McLean was there from the early days of EUROCHIP (1989–1995) and later throughout Europractice (1995 – 2020), navigating complex technical and logistical challenges and helping build the pan European infrastructure that still supports thousands of students and researchers today. We spoke with him about this challenging yet rewarding journey.

John McLean holds a PhD in computer aided design of digital systems from Heriot-Watt University. He joined the Rutherford Appleton Laboratory, part of UKRI-STFC, in 1979 and became a member of the EUROCHIP Executive Board in 1989. Throughout his career, he led the design tool activities of both EUROCHIP and Europractice, building a service that provided universities with secure, affordable access to industry-standard EDA tools and in-depth training courses. John retired in 2020 and was awarded an OBE in recognition of his contributions.

Members of the EUROCHIP consortium: Etienne Bourdeaudhui (imec), Bernard Courtois (CMP), John McLean (RAL), Augustin Kaesser (GMD), Ole Olesen (DTU)

Today, hundreds of European universities and research institutes use design tools licensed via Europractice. How did such a fundamental service begin?

John McLean: In the 1980s, many countries had their own national schemes to support microelectronics education, but each operated in isolation. It quickly became obvious that this fragmented landscape could not deliver the scale Europe needed. Universities lacked access to industry-standard EDA tools, and without those, it was impossible to bridge the widening gap between academic teaching and industrial practice – a concern shared across Europe at the time. This is what motivated the creation of EUROCHIP and later Europractice.

From the very beginning, the design-tool strategy was clear: provide academic and research institutions with the best-in-class software that is often only available to leading commercial organisations. Over the decades, this principle remained unchanged. What did change – dramatically – were the tools themselves. The tools we deal with today are orders of magnitude more complex and address technologies thousands of times more dense than what existed 30 years ago.

Europractice currently distributes around 65,000 design-tool license bundles every year – an impressive scale. How did you manage this in practice?

John McLean: Each Europractice member institution typically needs many different tools, often for large groups of students and researchers. Once you start serving hundreds of institutions, you quickly learn that individually tailoring licenses for each one is impossible. That is why, from the earliest days, we introduced vendor-specific bundles: a curated set of the most widely used modules from a given EDA provider.

Less commonly used or commercially sensitive tools were provided separately. This arrangement protected the interests of the vendors – who were understandably cautious about distributing their most high-end technologies too broadly – while making sure that institutes that needed advanced capabilities could access them.

And there was another guiding principle: continuity. If a university invested in an IC bundle years ago, we made every effort to ensure that – as long as they maintained annual support – this bundle would evolve over time. For instance, the same bundle could be used in the mid-1990s to design a 3µm IC and today to target advanced FinFET nodes – because the content kept evolving with the industry. This stability was essential. It reflected the fact that most users were building long-term research and teaching programs – and they needed tools that could grow with them.

Back in those early days, the logistics must have been very challenging.

John McLean: Indeed, the logistics were extraordinary – and almost unimaginable today. Everything was still distributed physically. For a single university, we would ship around ten large boxes filled with paper manuals, training materials on about 20 VHS tapes, and software on sets of roughly 100 CDs. Imagine repeating this for hundreds of Europractice member institutions every year!

At UKRI-STFC, we stored such vast quantities of manuals and media that the fire officer would warn us about the sheer volume of boxes stacked in the building.

And the distribution challenges didn't end there. In some regions, university networks simply weren't ready for large electronic downloads. I remember once we had to give a training course abroad, where they could not find the necessary number of required Sun workstations in the country. So we ended up loading the machines into a van in the UK and driving them across Europe. It was the only way to ensure the course could run.

It sounds almost comical today, when everything is downloadable, but that's what it took at the time to guarantee that every university, no matter where it was, had access to the same tools and training.

CDs distributed to Europractice members with design tool compatible design kits.

You mentioned training. Has it been part of Europractice from the beginning?

John McLean: Not exactly. In the early years, Europractice focused on providing access to design tools and IC fabrication. Training, at that stage, was largely handled by individual universities or by national schemes. It worked for a time, but as design tools and technologies became more sophisticated, it became clear that this model was no longer feasible.

Academic staff found themselves spending too much time trying to keep pace with rapidly evolving tool functionality, while new researchers often struggled to navigate complex design flows involving multiple EDA tools. Meanwhile, our support team kept receiving the same technical questions from different users each year. For the sake of the users – and our own sanity – we needed to find a more coordinated approach.

Is this when Europractice training courses were introduced?

John McLean: Exactly. We tackled the problem from two directions. First, we negotiated access to the EDA vendors' online training materials for Europractice users – something that took time, diplomacy, and quite a bit of security work behind the scenes.

Second, we started developing our own design-flow training courses. These courses combined lectures with extensive

Europractice hosts booths at major conferences to engage with professors and students. Shown here at MEMS2020: Pieter Claes and Romano Hoofman (imec) and John McLean (RAL).

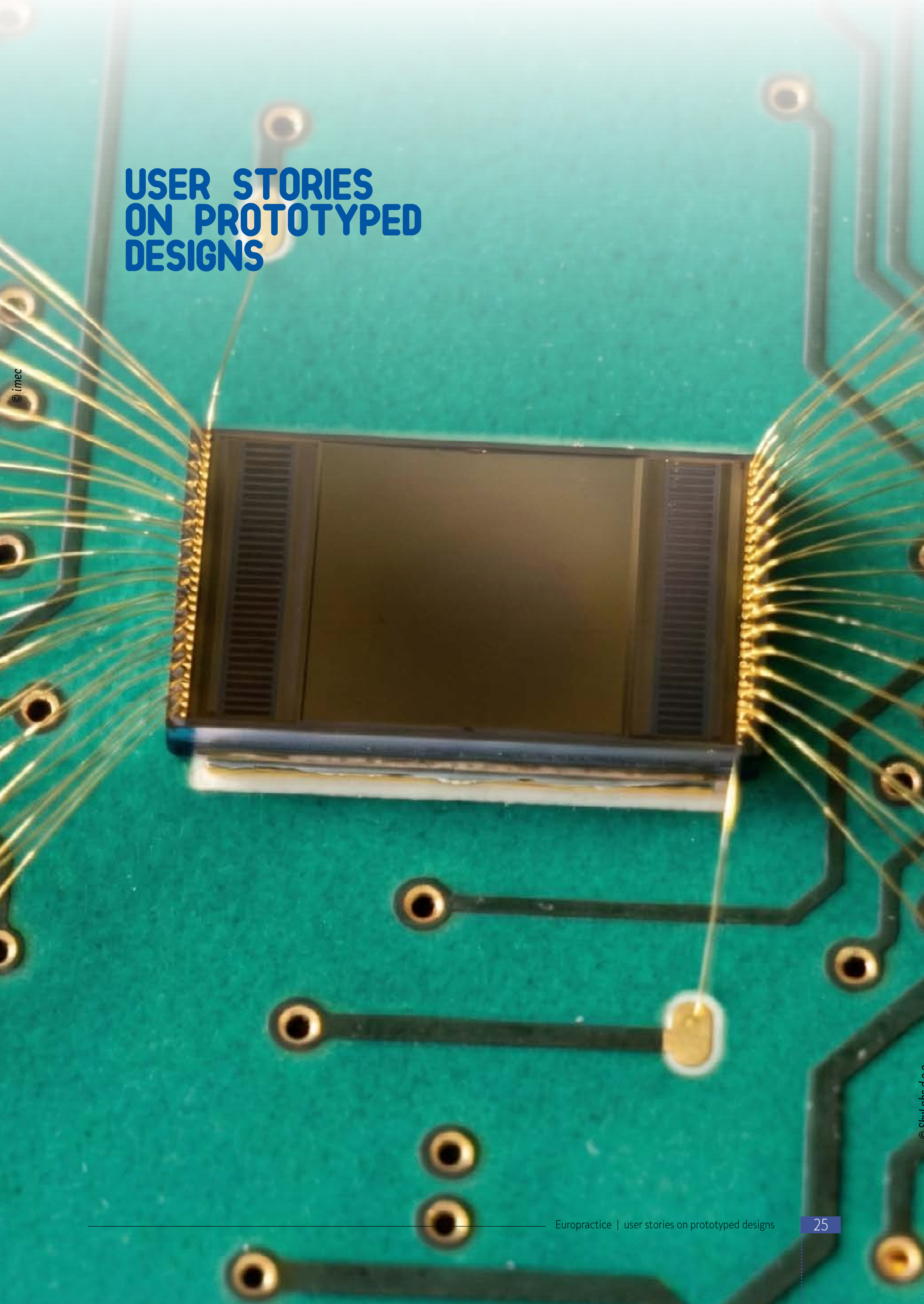
practical sessions and reflected the reality that modern design flows often require tools from multiple vendors to work together within a single foundry PDK. Our intention was to guide users through the complete flow – not just tool by tool, but across the interfaces where problems most often arise. Each course was built around the tools and PDKs available in the Europractice portfolio, ensuring direct relevance to academic design work.

More than 100 lecturers attend Europractice training activities annually. Could you tell us a bit more about this so-called 'Train-the-Trainer' concept?

John McLean: From the beginning, we noticed that many course participants were lecturers or professors. They typically returned to their institutions and passed on what they had learned to their own students, which multiplied the impact far beyond what our team could achieve directly. This natural amplification effect became the foundation of the Train-the-Trainer model. To further support it, we introduced very low-cost training licenses.

In many ways, this mirrors the broader Europractice philosophy we adopted from the start: identify the leverage point where our efforts can generate the greatest impact with the limited resources we have. Today's persistent demand for well-trained microelectronics engineers is not a sign of failure – it is a result of the growth of a sector that has expanded rapidly over the past decades. Europractice has played an important role in enabling that growth by ensuring that universities can educate engineers who are ready to contribute from day one.

Early Europractice Microelectronics Design training delivered by STFC at Slovak Technical University in Bratislava.



USER STORIES ON PROTOTYPED DESIGNS

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Fully Integrated Autonomous K-Band Complex Permittivity Sensor SoC for Ultra-Low-Power Biomedical Monitoring

Institute for CMOS Design, Technische Universität Braunschweig, Germany

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E-mails:	a.dossanov@tu-braunschweig.de, v.issakov@tu-braunschweig.de

Technology:	GF 22nm FD-SOI 22FDX
Die Size:	~ 2mm × 1mm (total area ≈ 1.98 mm²)
Design Tools:	Cadence Virtuoso
Application Area:	Medical / Health

Introduction

Continuous monitoring of physiological and biochemical parameters is a key requirement for next-generation biomedical and implantable systems. Microwave dielectric sensing has emerged as a promising technique due to its ability to characterize material properties with high sensitivity using compact sensor structures. However, most previously reported dielectric sensors rely on external power management, data conversion, and digital processing, which significantly limits autonomy, miniaturization, and energy efficiency.

The main motivation behind this work was to address the challenge of fully integrating all essential system components—sensor, power management, data conversion, and digital control—on a single chip while achieving ultra-low-power operation suitable for long-term autonomous use. In particular, the goal was to enable complex permittivity sensing without external electronics, targeting future implantable biomedical monitoring applications.

Description

The presented chip is a fully integrated system-on-chip (SoC) featuring a K-band (≈22–25 GHz) complex permittivity sensor implemented in GlobalFoundries' 22 nm FDSOI CMOS technology. The SoC integrates a dielectric sensor front-end, a 10-bit ultra-low-power SAR ADC, a programmable NanoController acting as a software-defined finite-state machine, and a complete power management unit (PMU).

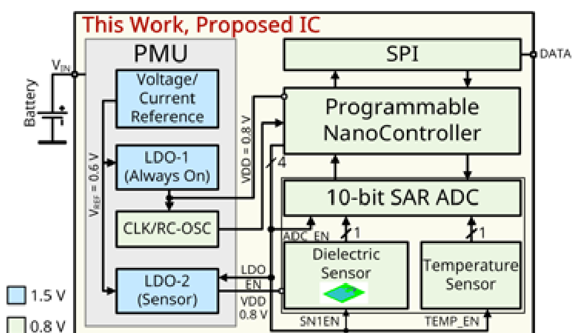

Fig.1: IC block diagram

The dielectric sensor is oscillator-based and employs an interdigitated capacitive sensing structure exposed to the material under test. Variations in the real and imaginary parts of permittivity are translated into frequency shifts and output power changes, which are converted into DC voltages using an on-chip mixer and power detector. The sensor output is digitized by the SAR ADC, optimized using a monotonic capacitor switching scheme for reduced dynamic power consumption.

A key innovation of this work is the integration of an ultra-low-power NanoController, which sequentially enables system blocks, stores measurement data in on-chip SRAM, and allows programmable measurement timing. The PMU includes two capacitor-less LDOs and an ultra-low-power voltage/current reference, enabling autonomous operation from a battery supply.

Results

The fabricated chip occupies a total area of approximately 1.98 mm², with the dielectric sensor itself occupying 0.6 mm². Measurement results demonstrate successful sensing of complex permittivity using isopropanol, ethanol, and methanol as materials under test. Clear and repeatable voltage shifts corresponding to changes in real and imaginary permittivity were observed.

The SoC achieves an average power consumption of only 14.3 µW per 10-minute measurement cycle, enabling operation for more than 400 days from a 100 mAh battery. Compared to state-of-the-art solutions, this work demonstrates the highest reported integration level for an implantable microwave dielectric sensor while significantly reducing system-level power consumption.

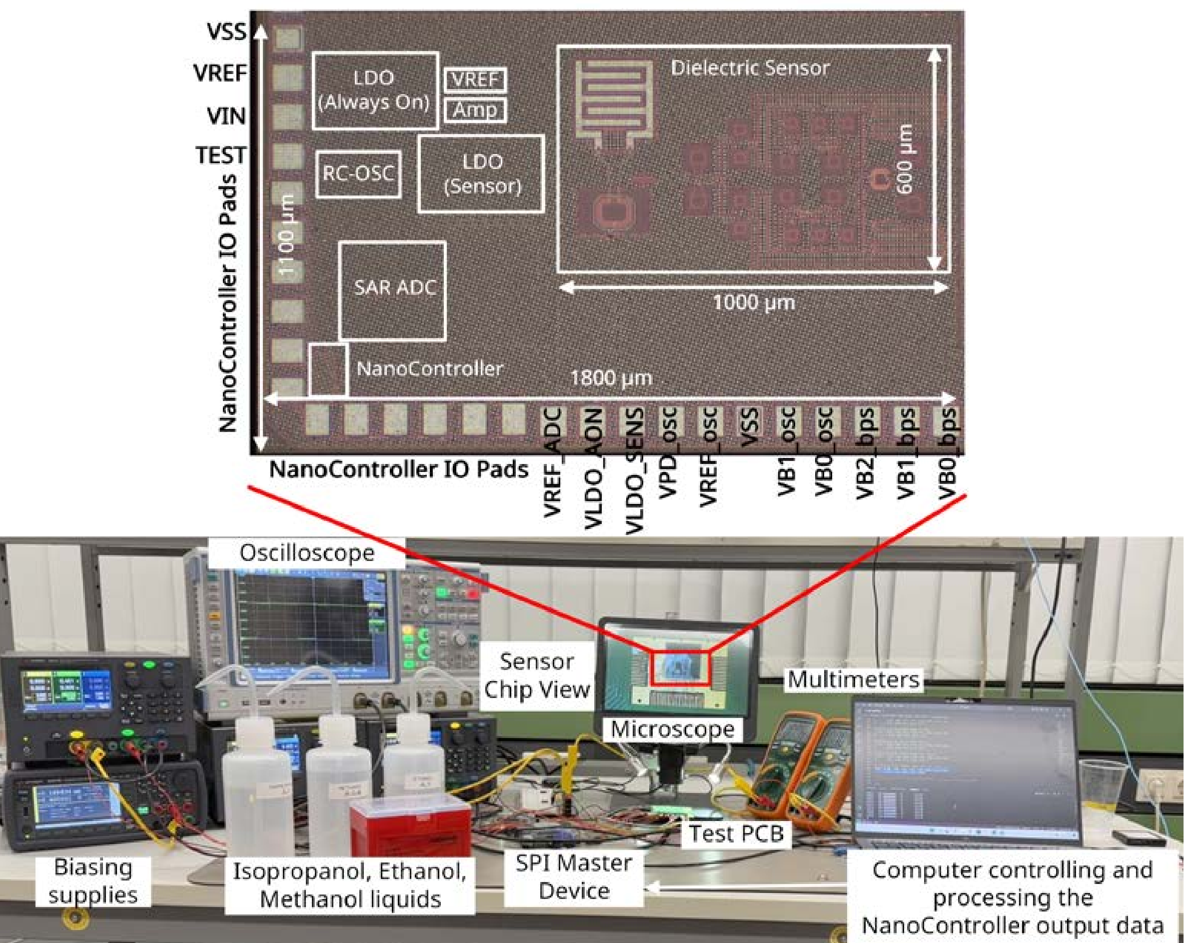

Fig.2: Chip measurement setup

Why Europractice?

Europractice services were essential for accessing advanced 22 nm FDSOI CMOS technology and professional EDA tools that would otherwise not be available in an academic environment. The program enabled cost-effective prototyping, multi-project wafer access, and reliable fabrication through an industrial-grade process. The support provided by Europractice was instrumental in successfully realizing and validating this highly integrated research prototype.

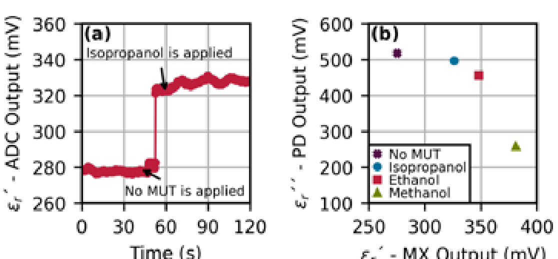

Fig.3: Measurement results

Acknowledgements

This work was supported by UNLOOC (HORIZON-KDT-JU-2023-IA-101140192), BMBF HOLODEC (16ME0704), and the GlobalFoundries University Program.

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A. Dossanov et al., “Fully-Integrated Autonomous K-Band Complex Permittivity Sensor in 22 nm FDSOI for Biomedical Body Parameter Monitoring Applications,” 2025 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA, USA, 2025, pp. 275-278, doi: 10.1109/RFIC61188.2025.11082827.

Wideband RF Front-End in 28-nm FD-SOI Using a Harmonic-Rejection N-Path Mixer for Low-Power and Low-Complexity Architecture

Université Grenoble Alpes, Grenoble Institute of Technology, Laboratoire TIMA, Grenoble, France

Contact:	Fadel Mohsen
E-mail:	fadel.mohsen@univ-grenoble-alpes.fr
Technology:	ST 28nm FD-SOI
Die Size:	1.2mmx1.2mm
Design Tools:	Cadence Virtuoso
Application Area:	IoT

Introduction

To address the limitations of traditional and standard N-path mixers regarding filtering efficiency and power consumption, a new Harmonic Rejection 4-Path Mixer (HR-4PM) architecture has been proposed. While previous topologies improved harmonic suppression at the cost of increased complexity, this new approach utilizes an innovative effective local oscillator (EFLO) design to minimize RF amplifier stages. By leveraging precise duty cycles and phase delays, the architecture successfully rejects up to the 6th harmonic using only four paths, offering a streamlined solution for high-performance RF front-ends.

Description

The fabricated IC is a complete RF front-end where the received signal is amplified by an LNA. This LNA is loaded by eight differential amplifiers that feed the passive mixer. To compensate for mixer losses, the output signal is subsequently amplified by a baseband amplifier. The mixer is controlled by accurate phases generated via a digital block to achieve specific duty cycles and phase delays. The designed RF front-end achieves 40 dB conversion gain, 8.5 dB noise figure, and harmonic rejection levels of 41 dB and 47 dB for the third and fifth harmonics, respectively, while consuming only 15 mW. These results outperform many state-of-the-art solutions in terms of energy efficiency and harmonic suppression.

Results

The circuit was recently received, and the measurement process is currently underway.

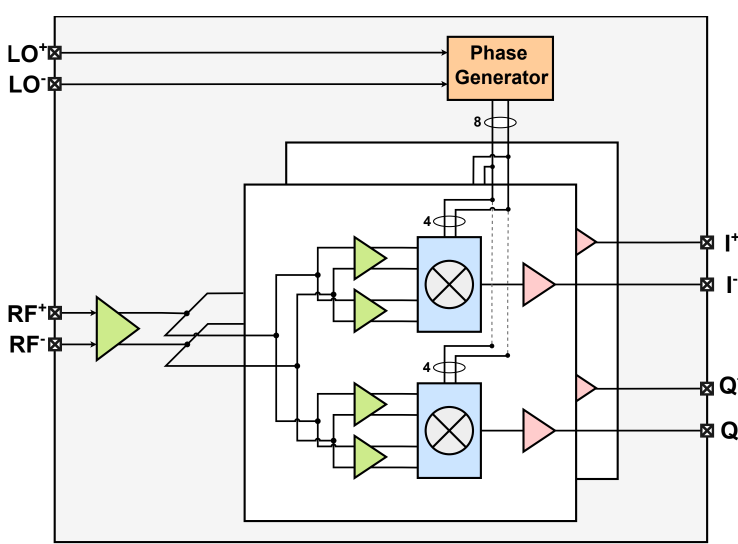

Fig.1: Simplified block diagram of the proposed RF front-end.

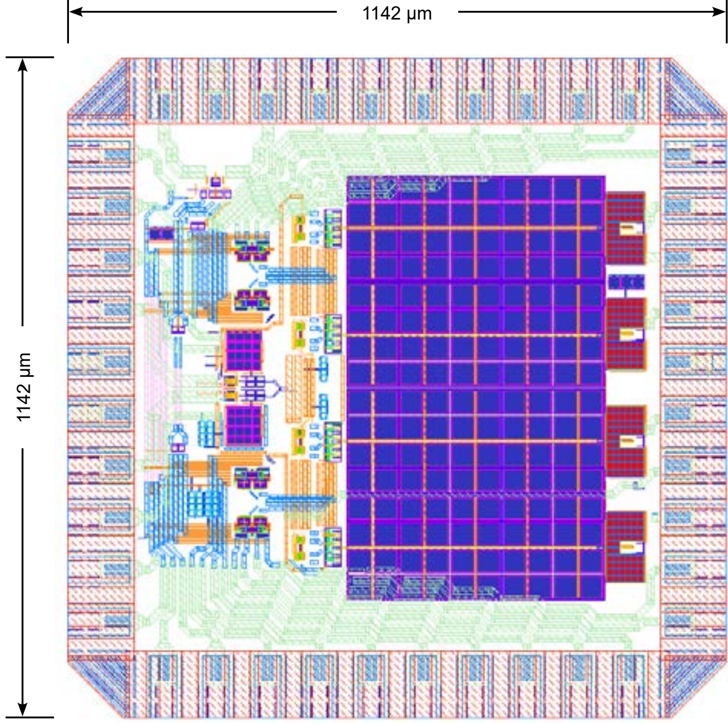

Fig.2: Layout of the full receiver, ready for packaging, in 28 nm FD-SOI CMOS technology from STMicroelectronics.

Why Europractice?

For several years, Grenoble INP has leveraged Europractice services through CIME-P. This collaboration is primarily motivated by the access it provides to STMicroelectronics' fabrication capabilities, specifically the 28nm FD-SOI technology.

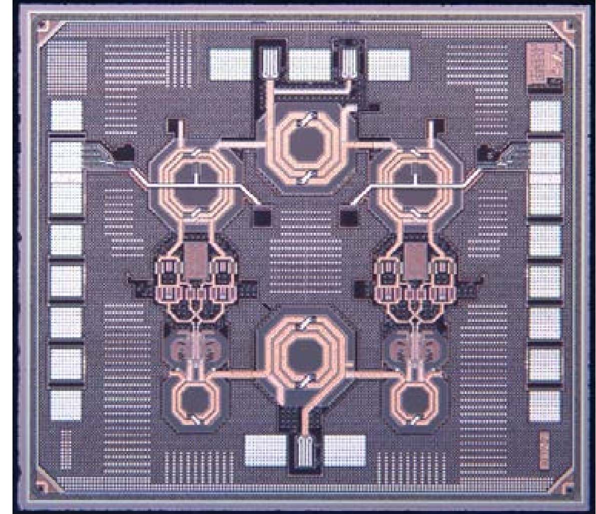

Fig.1: Micrograph of the fabricated die.

B55X Balanced Power Amplifier for 5GNRU FR1 - 6G FR3 applications

IMS Laboratory, University of Bordeaux, CNRS, Bordeaux INP, France

Contacts:	Paul Rezette, Nathalie Deltimple, Eric Kerhervé
E-mail:	nathalie.deltimple@ims-bordeaux.fr
Technology:	STMicroelectronics 55nm BiCMOS55X
Die Size:	1.17mm x 1.33mm
Design Tools:	Cadence Virtuoso
Application Area:	Datacom / Telecom

Introduction

The Frequency Range 3 (FR3) band offers an ideal coverage/data-rate compromise for extending modern cellular applications, motivating the expansion of 5G NR into unlicensed bands (5G NR-U) and future 6G uses. These applications require integrated power amplifiers in phased-array systems MIMO small cells, with active load-pull robustness, linearity and low cost. As BiCMOS technology allows to combine CMOS transistors for digital functions integration and bipolar transistors for analog and power functions, this technology is particularly relevant for targeted application. This work is in the frame of the Horizon Chips JU SHIFT project, which aims to develop innovative semi-conductor technologies and to target telecommunications applications, such as wireless 5GNR (Beyond 5G) and 6G network access, ultra high-speed optical links between servers, satellite telecommunications and Earth observation.

Description

The designed and fabricated device is a balanced power amplifier (PA), implemented in BiCMOS 55nm from STMicroelectronics (B55X). The targeted applications are 5GNR-U and 6G, and the BPA will operate in the 6.4 to 8.4 GHz band. The BPA relies on power cells, baluns and hybrid couplers. The two cascode differential power cells relies on stacking and combining bipolar transistors with high breakdown voltage and high current density. The amplifying stage included neutralization technique both capacitive and inductive in order to overcome the bandwidth/efficiency compromise. The two hybrid couplers are based on original transformers which allows to control the central frequency and decrease the losses.

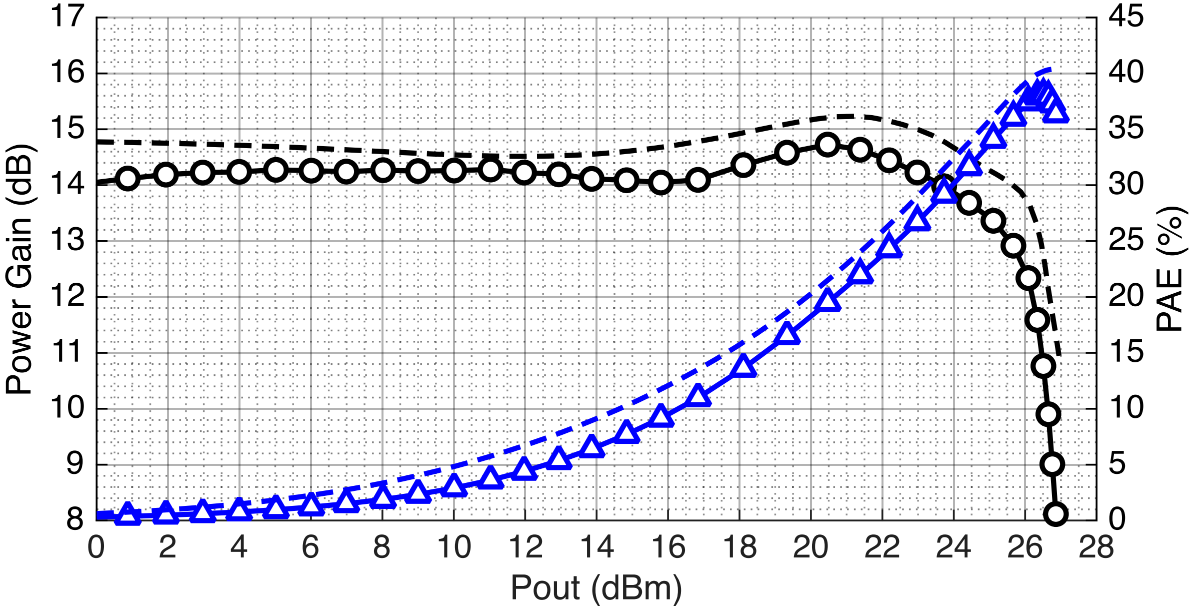

Fig.2: Measured output power, power gain, and poweradded efficiency.

Results

The Balanced PA die area is $1.56mm^2$ including pads (Fig.I). The BPA has been measured under CW and modulated signal conditions. S-parameters measurements help us to verify the agreement with the electrical and EM simulations with small signal gain equal to 14.5dB and good input/output matching network (S11/S22 below -10dB) in the 6-10 GHz bands (BW=50%). On the overall band, the BPA exhibits a saturated output power between 25.8 and 27.1 dBm, a OCP1dB between 24.6 and 25.8 dBm and a peak PAE between 23 and 38 %. The BPA presents also interesting performances at 8dB power back-off, as the PAE8dB OBO is between 10.8 and 15.5% on the overall band. Then 5G-NR FR2-1 TDD modulated signals were applied for contiguous multi-carrier signals (2/4/8-CC) of 400 MHz, 256-QAM, 1.8 Gb/s, with spacing of 60 kHz, and a PAPR of 11.8/11.7/12.0 dB with an RMS EVM of -30 dB (Fig.2). These results are in line with the state-of-the-art on RF PA, knowing that 55nm MOS transistors are available in this technology for digital function integration.

Why Europractice?

Europractice gives us access to the ST B55X technology and provides the tools to design our circuits. They offer quick and helpful support during the tape-out process, which is a real added value for the success of the project.

Acknowledgements

This work is in the frame of the SHIFT project, supported by the Chips Joint Undertaking and its members under grant agreement n° 101096256, including the top-up funding by French BPI. The authors would like to thank STMicroelectronics and CIME-P for chip manufacturing and Rohde & Schwarz for the measurements.

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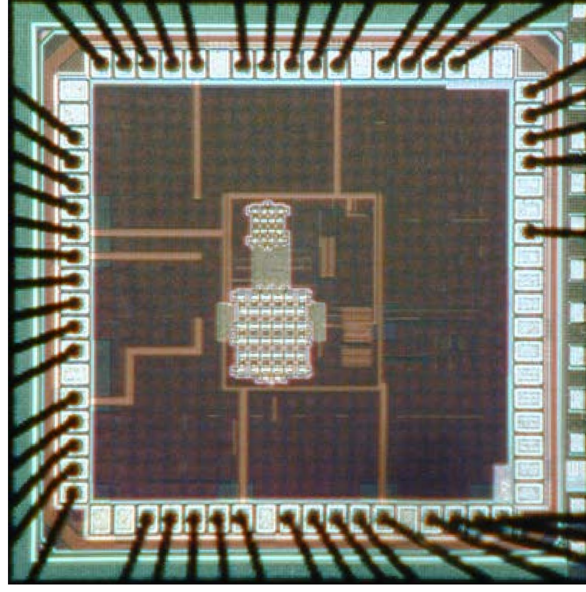

Fig.1: Test chip Microphotograph

A Microbolometer-Based Time-to-First-Spike Pixel for Infrared Imaging

CIME Nanotech, Grenoble, France

Contact: Ayoub Talbi
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Technology: ST 130nm HCMOS9A
Die Size: 1.467mm x 1.467mm
Design Tools: Cadence Virtuoso, Siemens Calibre
Application Area: IoT

Introduction

The decision to develop this device stems from the limitations of traditional frame-based infrared (IR) imaging, which suffers from high power consumption, excessive data redundancy, and high latency. While Time-to-First-Spike (TFS) encoding has successfully addressed these issues in visible light spectrum sensors using photodiodes, no implementation had yet extended this neuromorphic paradigm to uncooled microbolometers for thermal imaging. This research addresses that gap by proposing the first TFS pixel architecture based on a thermal sensor, aiming to enable low-power, event-driven IR sensing suitable for autonomous robotics, surveillance, and embedded vision systems.

Description

The designed device is the first implementation of a TFS pixel for infrared imaging that utilizes a thermistor-modeled microbolometer as the primary sensing element. This architecture transitions thermal imaging from traditional frame-based readout to a neuromorphic, event-driven scheme.

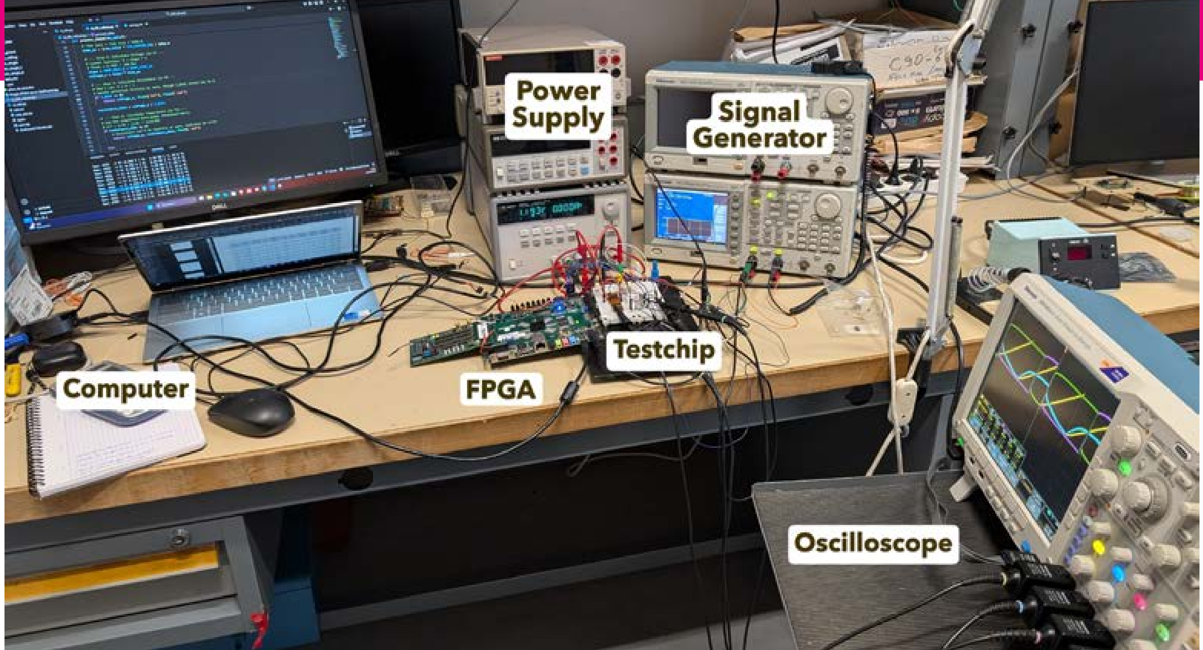

Fig.2: Experimental Setup

Core Mechanism:

- Sensing: The thermistor is modeled as a temperature-dependent resistor that converts incident IR radiation into a measurable change in resistance.
- Voltage Generation: A bias current is applied to the sensing element to generate a temperature-dependent voltage.
- Temporal Encoding: A comparator matches this voltage against a reference ramp.
- Spike Triggering: When the crossing occurs, the pixel "spikes," and a C-element ensures a reliable asynchronous handshake with the digital readout.
- Digitization: The time elapsed from the ramp start (latency) is captured by a Time-to-Digital Converter (TDC) to provide a digital output.

Implementation:

The proof-of-concept test chip was fabricated in ST 130nm CMOS. It integrates a single pixel for electrical characterization and a 3x3 pixel array to validate various readout strategies, such as global and rolling shutter modes.

Results

The research advances the state of the art by demonstrating the first successful modeling and simulation of a TFS encoding scheme for thermal sensors.

- Performance: Preliminary simulations confirm that temperature can be accurately encoded as spike latency, where higher temperatures result in shorter integration times.
- Efficiency: The architecture naturally suppresses spatial redundancy because pixels responding to similar IR radiation spike simultaneously, significantly reducing data bandwidth and power consumption compared to frame-based systems.
- Market Application: This technology is positioned for the "neuromorphic thermal imaging" market, providing a high-dynamic-range, low-latency solution for power-constrained applications such as autonomous robotics, smart building, and industrial monitoring.

Why Europractice?

The Europractice team provided essential support for this project by facilitating access to the 130nm CMOS technology of STMicroelectronics used for the ASIC design. Their services encompassed the necessary design tools, packaging, and manufacturing for the proof-of-concept test chip.

Acknowledgements

This work has been supported by the Association Nationale de la Recherche et de la Technologie (ANRT, No. 2024/0233) in the framework of a PhD thesis conducted in collaboration with Orioma and the TIMA laboratory.

Special gratitude is extended to the following individuals for their contributions to the project, from initial architecture to the final tapeout and test (listed in alphabetical order): Abdelhamid Aitoumeri, Antoine Abisset, Francois Berthollet, Laurent Fesquet, Marco Passy, Mohamed Akrarai, Mohammadreza Dolatpoor, Robin Rolland, Skandar Basrour, Etienne Leheurteux, Jean-Daniel Peyrard, Victorien Brecte

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TriglaV, a Fault-tolerant SoC for High Energy Physics Environments

CERN, Geneva, Switzerland

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Technology:	28nm RF/HPC+ CMOS
Die Size:	1mm x 2mm
Application Area:	High Energy Physics (HEP)

Introduction

Historically, ASICs for High-Energy Physics (HEP) relied on fixed-function digital logic with minimal configurability. However, future particle physics experiments will require increased data throughput, radiation levels, and operational complexity. This is shifting the demand toward modular, software-programmable System-on-Chip (SoC) architectures capable of reliable performance in harsh environments.

The SOCRATES project (SoC RAdation-tolerant Eco-System) was initiated to address this emerging need. Built using SOCRATES' automated platform for generating fault-tolerant SoCs, we developed the TriglaV ASIC manufactured in advanced 28nm bulk CMOS technology. The goal was twofold: First, to validate the SOCRATES design flow for radiation-tolerant SoCs as silicon prototype. The second was to experimentally prove that a RISC-V–based microcontroller-class SoC can operate robustly under the severe Total Ionizing Dose (TID) and Single-Event Effects (SEE) conditions expected in next-generation particle accelerators.

Description

TriglaV is a 32-bit RISC-V-based SoC and its architecture follows that of a basic modern microcontroller system, centring around a triplicated Ibex RV32IMC core, 64 kB of foundry SRAM, and a low-latency interconnect that links all major components. The system also incorporates common peripheral interfaces such as I²C, UART, and JTAG, enabling programming, configuration, and debugging.

A distinguishing feature of TriglaV is the extensive fault-hardening to protect against high rates of SEEs present in particle physics environments. Nearly all logic, combinational paths, and sequential elements are protected using Triple Modular Redundancy (TMR). Memory structures and data paths incorporate Hamming-based Error Correcting Codes (ECC), while a dedicated Memory Scrubbing and Protection Unit (MSPU) continuously scans the SRAM to correct SEUs and prevent the accumulation of multi-bit upsets. Physical layout techniques further reduce vulnerability, with spacing rules ensuring that a single particle strike cannot simultaneously corrupt multiple elements of a TMR set.

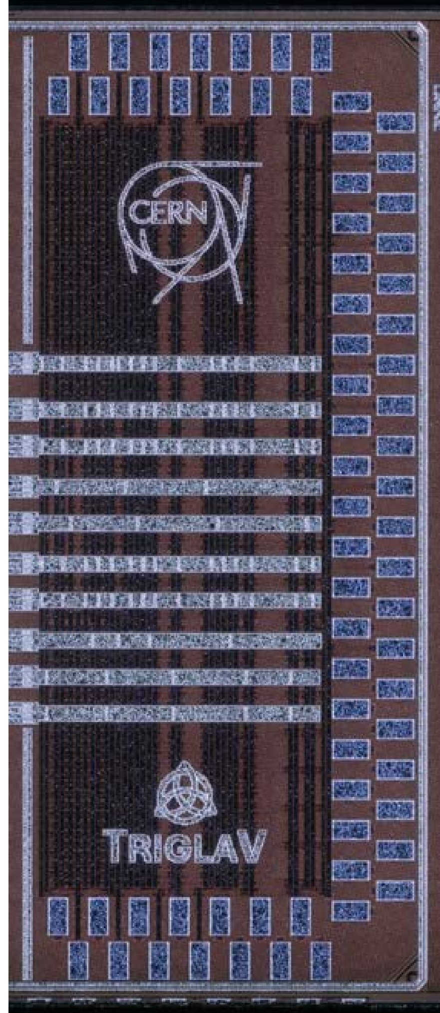

Fig.1: Microscope image of TriglaV with a 1mm x 2mm silicon area.

The resulting ASIC occupies roughly 2 mm² of silicon. Power consumption remains modest: at the nominal 250 MHz frequency and 0.9 V supply, the chip draws approximately up to 69 mW.

Results

TriglaV was subjected to comprehensive irradiation campaigns, including heavy-ion testing and high-dose-rate x-ray irradiation, to assess its robustness. During heavy-ion irradiation at UCLouvain, TriglaV showed SEU sensitivities consistent with expectations for the underlying technology. Thanks to the extensive use of TMR and ECC, the majority of radiation-induced upsets were correctly mitigated. Furthermore, the scrubbing mechanism for the foundry

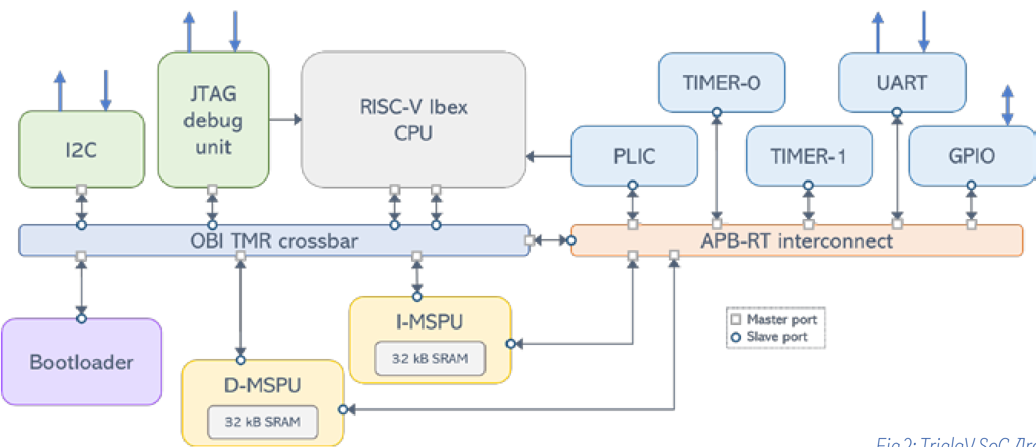

Fig.2: TriglaV SoC Architecture.

SRAMs proved effective even at high ion energy levels. Complementing the SEE study, TriglaV also underwent x-ray TID irradiation at CERN up to a cumulative dose of 1 Grad. Throughout the test, the device maintained full functionality across an operating voltage range of 0.8V to 1V and at frequencies up to 300 MHz. This result confirms the strong TID robustness of the underlying technology.

By validating both the SOCRATES design flow and the feasibility of hardened microcontroller-class SoCs using the 28 nm process, the project takes a significant step toward bringing modern, flexible computing architectures into the front-end electronics of HEP detectors. While some specific vulnerabilities were identified during testing, they are being further investigated and will guide refinements in future designs. Overall, TriglaV highlights the potential for software-programmable SoCs to replace traditional fixed-function ASICs in demanding scientific environments, opening the door to more adaptable, intelligent detector and accelerator instrumentation in the years ahead.

Why Europractice?

Within the framework of ASIC design for particle-physics instrumentation, CERN and its collaborating institutes and universities tape out more than 40 ASICs per year through the Europractice service. Europractice IC Services provides access to cutting-edge semiconductor technologies from the world's largest dedicated independent foundry, TSMC. In the absence of this service, projects such as the TriglaV ASIC would simply not have the possibility to access or exploit advanced technologies like the 28nm process. Equally important is the high-quality technical support that Europractice engineers provide throughout the design and tape-out phases.

Developing complex ASICs requires state-of-the-art EDA tools for design, implementation, and verification at both the component and system levels. Europractice's software service is an indispensable asset for ASIC development at CERN and its partner institutions, offering a broad suite of advanced EDA tools and ensuring coherence across distributed design teams.

Custom microelectronic components implemented in advanced technologies are essential building blocks of today's sophisticated scientific instruments. The services provided by Europractice enable a large community of physicists and engineers at CERN and across dozens of collaborating institutes to access state-of-the-art EDA tools, advanced CMOS processes, and centralized, high-quality technical support—making the construction of these unique scientific instruments possible.

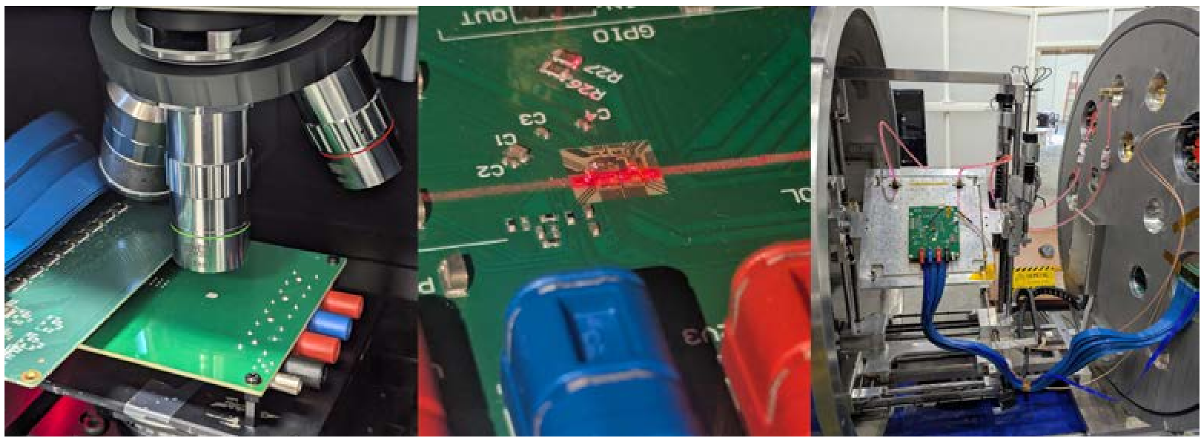

Fig.3: Extensive irradiation testing scenarios of the TriglaV chip bonded on a carrier board.

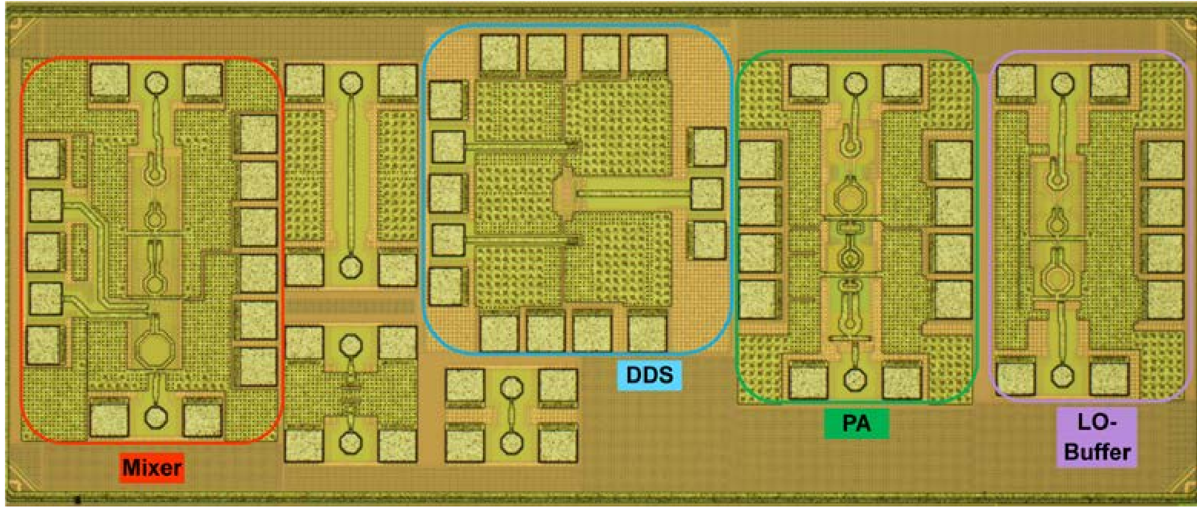

Fig.1: Micrograph of the fabricated breakout circuits

Breakout Circuits for novel DDS-based D-Band Transmitter

Friedrich-Alexander-Universtität Erlangen-Nürnberg, Germany

Contacts:	Tianzhu Huang, Alexander Schönecker
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Technology:	TSMC 28nm CMOS RF HPC+
Die Size:	1mm x 2.5mm
Design Tools:	Cadence Virtuoso
Application Area:	Datacom / Telecom

Introduction

The emergence of the next-generation 6G communication standard is bringing unprecedented demands for high-performance transceiver architectures. At the same time, radar and sensing applications are rapidly expanding into areas such as smart-city infrastructure, automotive safety, and environmental monitoring. In this context, the D-band (110–170 GHz), with its exceptionally large available bandwidth, has become a highly promising frequency range that enables both ultra-high-data-rate communication and enhanced sensing capabilities. Fully exploiting these advantages requires transceiver systems that can support diverse, reconfigurable, and multifunctional waveforms to handle the dual demands of communication and sensing. Direct digital synthesis (DDS) offers a compelling approach in this regard, providing fine-grained signal control and highly flexible waveform generation, making it particularly well-suited for next-generation D-band transceiver designs.

Description

As the first tape-out of the proposed system, we have designed and fabricated breakout circuits for all essential transmitter components, including the DDS with SPI interface, LO buffer amplifier, up-conversion mixer, power amplifier, and on-chip calibration structures. The DDS enables software-defined, flexible generation of chirps for FMCW radar as well as QAM-modulated signals for high-speed communication. The up-conversion mixer and power amplifier are engineered to deliver wide bandwidth, high linearity, and excellent power efficiency in the D-band, which are key requirements for high-performance JCAS systems.

Results

The circuits are still undergoing comprehensive measurements. Preliminary data indicate that the PA achieves a small-signal gain of 26.6 dB with a wide 3-dB bandwidth of 32 GHz, covering more than 50% of the available D-band spectrum. The up-conversion mixer exhibits a conversion gain of 2 dB and an RF bandwidth of 30 GHz. These broadband characteristics demonstrate the feasibility and strong potential of the circuits for future D-band JCAS systems.

Why Europractice?

We use Europractice because of its simple and reliable access to advanced semiconductor technologies, mature PDKs, and broad EDA tools. Its technical support greatly facilitates our research and prototyping process, enabling quick implementation of innovative designs.

Acknowledgements

The authors would like to thank the financial support by the Federal Ministry of Research, Technology and Space (BMFTR) of Germany in the project “ATTRACTS” (grant number: 16ME0971). The work contributes to the research within the 6G-Valley innovation cluster.

A Single-Photon Counting X-ray Detector with a 25 mm Pixel Pitch

AGH University of Krakow, Poland

Contacts:	Pawel Grybos, Rafal Kleczek, Piotr Kmon, Piotr Otfinowski
E-mail:	pawel.grybos@agh.edu.pl
Technology:	TSMC 40nm
Die Size:	3.2mm x 4.8mm
Design Tools:	Cadence Virtuoso, Spectre, Siemens Calibre
Application Area:	PhotonCounting Detectors

Introduction

The current research efforts on the Single Photon Counting (SPC) Hybrid Pixel Detectors (HPD) follow several different directions. One of them is the operation with higher photons' flux intensities and better spatial resolution at the same time. The use of pixels with smaller dimensions allows for an increase in both the HPD count rate performance and spatial resolution. Usually, the pixel pitch in SPC hybrid detector systems is in the range of 100 μm down to 50 μm, however we made an important step forward reducing the pixel pitch down to 25 μm.

Description

This story reports on the design and tests of a new integrated circuit operating in the SPC mode, called PIX25, with a pixel matrix of 128 x 128 pixels and a pixel pitch of 25 μm. The pixel matrix operates in two phases, i.e. in the acquisition phase (each pixel processes the input pulses individually) and the counting phase (pulses with an amplitude above set threshold are counted by each pixel). Additionally, to very small pixel size the PIX25 IC offers:

- ultra-fast signal processing, precise gain and offset trimming block working in each pixel independently,
- operation with the detector collecting holes or electrons,
- built-in chip testing block for evaluation of analog parameters of the pixel,
- wide range of bias control to set-up the trade-off among power consumption, count rate, and noise for a desired application,
- high reconfigurability of the readout matrix, i.e. the IC can be connected to sensors with a pixel pitch that is a multiplication of 25 μm.

The limited silicon area per pixel required a simplified readout architecture of analog front-end electronics, with a significant power limitation per pixel, keeping at the same time low noise, and fast signal processing (high count rate performance) with a pixel-to-pixel mismatch reduction.

Results

The p-type silicon sensors with 150 μm was bump-bonded to PIX25 IC (Fig.1).The example of tests with full field uniform X-ray illumination are shown in Fig.2. A lead test pattern was placed in front of the detector to check the visual resolution. The inset plots in each image show the cross-section of the images along the direction perpendicular to the lines of the test pattern - 20 lp/mm is visible. The proposed IC is a strong candidate for the new generation of 3D high-granularity X-ray hybrid detectors, as illustrated schematically in Fig.3. In such 3D hybrid pixel detector architecture, a thick sensor is partitioned into multiple layers with fine pixel pitch, each equipped with an independent, thinned ReadOut IC (ROIC) that is effectively transparent to X-rays. This approach enables efficient X-ray

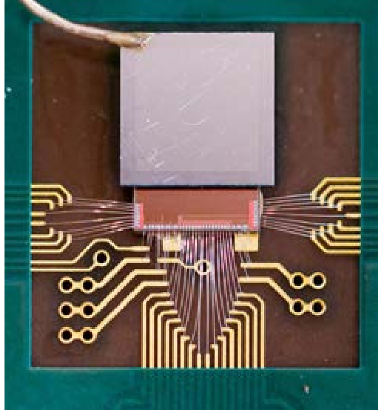

Fig.1: Photo of PIX25 IC bump-bonded to silicon pixel detector

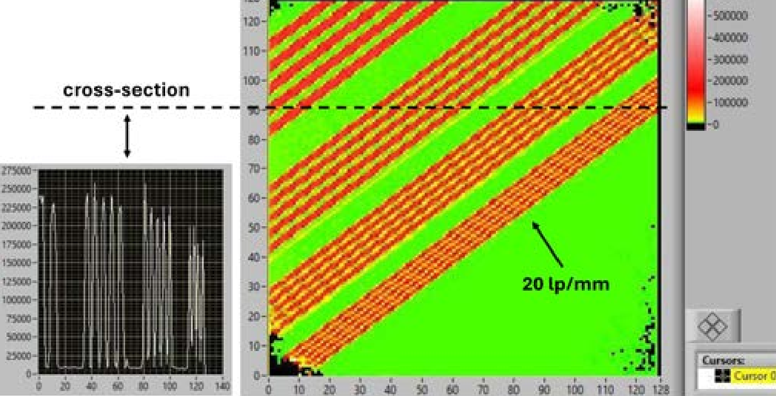

Fig.2: Example of X-ray image taken with a lead test pattern

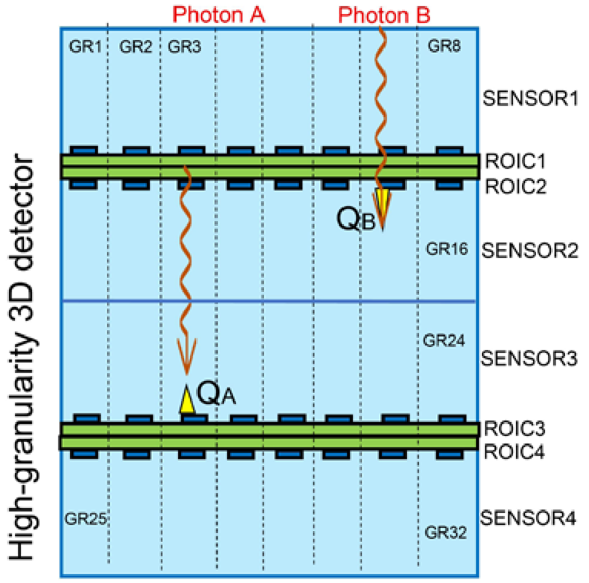

Fig.3: 3-D high-granularity hybrid pixel detector.

absorption while improving intrinsic spatial resolution by mitigating charge-sharing effects.

Why Europractice?

AGH University has benefited from the Europractice offer for many years, with a lot of successful tapeouts. Europractice offers affordable fabrication of our prototypes on MPW and mini@sic runs and provides access to a wide variety of design tools. It is an essential partner in our research.

Acknowledgements

This work has been supported by the National Science Center, Poland under project no. 2023/51/B/ST7/01782

Fig.1: HEEPidermis system-level diagram.

HEEPidermis: a versatile SoC for BioZ recording

Embedded Systems Laboratory (ESL), EPFL, Lausanne, Switzerland

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E-mail:	juan.sapriza@epfl.ch

Technology:	TSMC 65nm LP MS/RF
Die Size:	1.5mm x 1.5mm
Design Tools:	Siemens Questasim, Synopsys Design Compiler, Cadence Innovus, Cadence Virtuoso, Synopsys VCS
Application Area:	Medical / Health

Introduction

Biological impedance (BioZ) is an information-packed modality that allows for non-invasive monitoring of health and emotional state. Currently, most research involving tissue impedance is based on bulky or fixed-purpose hardware, which limits the scope of research and the possibilities of experiments.

Description

HEEPidermis [1] integrates all the blocks needed for tissue impedance measurement, including two 8-bit, arbitrary-signal current DACs (iDACs), two VCO-based ADCs [2], and a RISC-V CPU to enable on-chip feature extraction for closed-loop operation. The design builds on the X-HEEP [3] open-source platform, extending its baseline MCU with tightly coupled custom peripherals and analog macros. The CPU coordinates the system, while X-HEEP's DMA automates data movement and processing between IPs. An event-based sub-sampler [4] improves storage and energy efficiency for long-term recording. Designed for versatility, the front-end supports multiple sensing modalities, and the CPU can adapt the operating point on the fly to maintain high sensitivity across a wide range of skin impedances. Beyond the on-chip ADCs (which can be used on their own or together in pseudo-differential mode), HEEPidermis can read data from external ADCs through SPI or decimate 1-bit data from external Delta-Sigma ADCs.

Fig.2: The fabricated chip. "HEEPidermis" is a play on words between X-HEEP: the platform it is based on, and "epidermis": the surface of the skin, where BioZ can be measured.

Results

HEEPidermis allows stimulation of the tissue, recording of long-term variations and complex data processing all under a 100µW budget. The digital back-end can operate from 10s kHz to 10s MHz, in the range 0.7-1.2V.

Why Europractice?

Europractice has made this project possible by helping us acquire EDA tool licenses, access to technology design kits, participation in their mini@sic MPW program, and through their hands-on courses. Their support was instrumental in the preparation, execution and later debugging of the design.

Acknowledgements

This work was supported in part by the Swiss NSF Edge-Companions project (GA No. 10002812), and in part by the Swiss State Secretariat for Education, Research, and Innovation (SERI) through the SwissChips Research Project. This research was partially conducted by ACCESS – AI Chip Center for Emerging Smart Systems, supported by the InnoHK initiative of the Innovation and Technology Commission of the Hong Kong Special Administrative Region Government.

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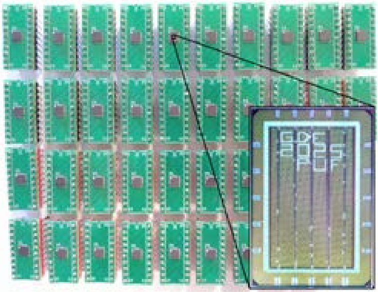
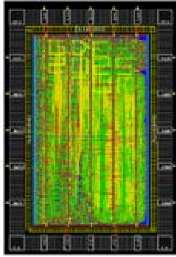

Fig.1: File: Full ASIC Design.

GenGARO-PUF: From FPGA to ASIC

Group of Electronic Design (GDE), University of Zaragoza, Spain

Contacts:	Abel Naya, Raúl, Aparicio-Téllez Miguel Garcia-Bosque, Santiago Celma
E-mail:	abeln@unizar.es

Technology:	TSMC 65nm Low Power MS/RF
Die Size:	1.5mm x 2mm
Design Tools:	Cadence Genus, Innovus, XCelium Logic Simulator
Application Area:	Security / Privacy

Introduction

One of the research areas in our group focuses on the design and implementation of hardware security primitives, which also includes Physically Unclonable Functions (PUFs) for security and device identification purposes. After a successful design and implementation of a PUF based on nonlinear oscillators in FPGA [1], the next challenge was to implement the design on ASIC.

Description

The chip consists of four main components:

1. One circuit with 256 Generalized Galois Ring Oscillators (GenGAROs) with 3 gates (type A), 256 GenGAROs with 11 gates (type B), and a 256-bit output comparing the bias of the oscillators. Oscillators are always active. Each bank produces a weak PUF with 128-bit responses derived from non-overlapping pairwise comparisons.
2. A second circuit with the same 512 oscillators but with an additional gate each to enable/disable them independently, and which outputs the bias directly (512*30=15360 bits). Based on the measured bias values, the PUF response is generated externally. In order to avoid having too many pins, special logic was introduced to be able to switch between both designs. The inputs and outputs were also developed using shift registers, with an additional output pin to ensure the input bits are being saved correctly. Furthermore, the ASIC incorporates two additional test circuits:
3. A sequence of ten 'not' gates directly connected to two pins to test if the chip works, and check whether a small periodic signal could be amplified.
4. An independent (albeit with the ability to be enabled/disabled) and stable ring oscillator directly connected to a pin, to test if our measurement devices are able to read this type of signals, and to check the difference between the simulated signal and the real one.

Results

To test the chips, 50 of them were packaged and mounted on custom PCBs. This allowed us to easily measure the output of each chip, for later analysis. The bias obtained on the second circuit (with the enable/disable characteristic) yielded notable results, obtaining almost perfect PUF characteristics both for uniqueness (inter-chip hamming distance >49%), reliability (>98.8%), uniformity, and resistance to modelling attacks.

A paper is expected to be published in the following months with the results of these experiments, and future designs are expected to be fabricated for future related work.

Why Europractice?

Europractice provides us with a streamlined way to fabricate designs. Special mention to the new and improved page to specify the bonding diagram, which greatly simplifies the final step of the process.

Acknowledgements

This work was supported by Universidad de Zaragoza (UZ2024-IyA-01), Agencia Estatal de Investigación (PID2024-157204OA-I00), and Diputación General de Aragón (DGA) fellowship to Raúl Aparicio-Téllez.

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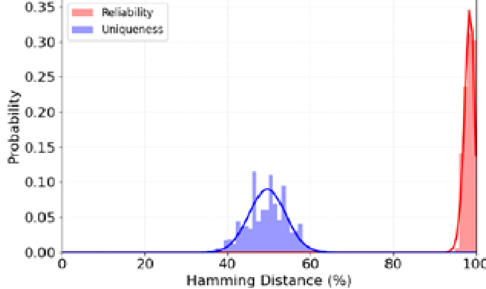

Fig2: Uniqueness and reliability distributions of the PUF of 3-stages with enable.

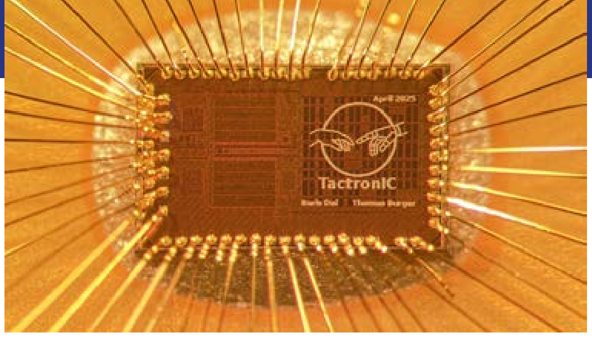

Fig.1: Chip micrograph of TactronIC

System-on-Chip Design for a Capacitive Tactile Sensor for Robotic grippers

ETH Zurich, Switzerland

Contacts:	Baris Dal, Thomas Burger
E-mail:	baris.dal@iis.ee.ethz.ch
Technology:	TSMC 65nm
Die Size:	1.2mm x 2mm
Design Tools:	Cadence Virtuoso, Innovus, Synopsys
Application Area:	Manufacturing / Industry 4.0

Introduction

Robotic systems primarily rely on visual information to perceive and manipulate objects, whereas humans have remarkable manipulation dexterity through the sense of touch. In situations where vision becomes unreliable, such as environments with occlusion or low lighting, the performance of the robotic systems deteriorates significantly. To enhance the manipulation capabilities of robotic grippers, a capacitive tactile sensor [1] is employed. This sensor features a dense array of 1 sensor/mm^2 on a flexible substrate and exhibits a capacitance change with respect to the applied force, enabling a tactile resolution comparable to that of human touch. However, the sensor also introduces a substantial amount of parasitic capacitance and noise. Therefore, to accurately read this high-density capacitance array, a dedicated capacitance-to-digital converter (CDC) circuit, TactronIC, is proposed.

Description

The proposed system comprises a Finite State Machine (FSM) that sequentially reads each capacitance in the 12 x 12 array, a switched-capacitor integrator circuit and a 13-bit Successive Approximation Register (SAR) ADC. The architecture includes programmable gain and multiple operating modes, and supports a refresh rate of 8 kHz with a sampling frequency of 1.152 MHz. To mitigate DC offsets and low-frequency noise in the sensor readings, correlated double sampling (CDS) is employed. Since CDS requires differential measurements, the sensor is driven with an AC excitation, enabling two sequential samples-one with a high input level and one with a corresponding low level-within each sampling period. The resulting differential signals are digitized using a merged capacitor switching charge redistribution scheme. Additionally, a novel charge-compensation technique is introduced to reduce the impact of bond-wire parasitics and to lower the reference-buffer power consumption.

Results

The die micrograph of the chip, shown in Fig.1, is characterized using off-chip capacitors whose values are measured with Keysight E4980AL LCR meter. Fig.2 presents the measurement results together with fitted lines for the four gain configurations covering an input capacitance range of 2.5 pF to 10 pF in 2.5 pF increments. Each gain stage exhibits a correlation coefficient(R) of 0.999. Moreover, the converter achieves a resolution of 1.22 fF with an RMS noise of 488 aF at a 1µs conversion time. The measurement results confirm the simulation predictions, demonstrating that the design goals were successfully achieved.

Why Europractice?

Europractice provides universities and academic institutions with a cost-effective means of accessing state-of-the-art technologies for integrated circuit manufacturing. Moreover, its team is consistently supportive and highly responsive, delivering exceptional technical guidance throughout every stage of the tape-out process. Without these services, we would face significant obstacles in developing new ideas or conducting advanced research.

Acknowledgements

The authors gratefully acknowledge the Microelectronics Design Center at ETH for their valuable help with the tape-out, and Aldo Rossi for bonding the chips. This work has been supported by an Internal ETH grant for the "TACTFUL" project.

References

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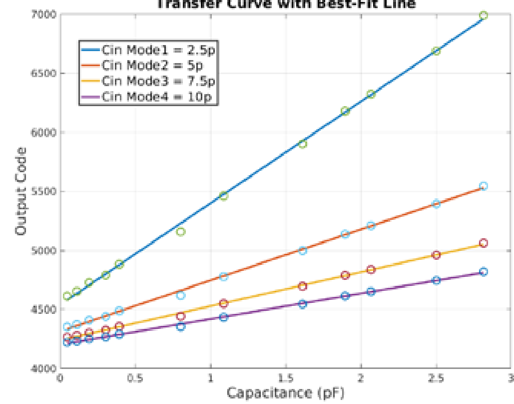

Fig.2: The transfer characteristic of the CDC with fitted lines

Integrated Inductors for Autonomous Energy Harvesting System

Department of IC Design and Test, Institute of Electronics and Photonics, Slovak University of Technology in Bratislava, Slovakia

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Technology:	UMC 65nm (mini@sic)
Die Size:	1.872 mm x 1.872 mm
Design Tools:	Cadence Virtuoso, ANSYS Electronics Desktop
Application Area:	Energy

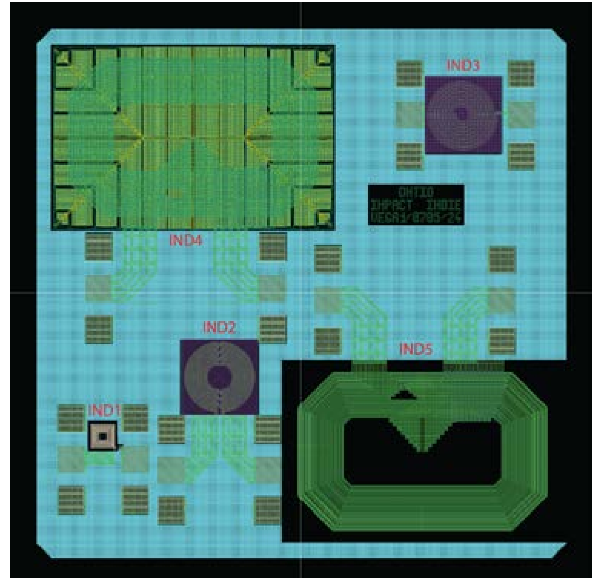

Fig.1.: Layout of the fabricated inductors.

Introduction

Power management is an essential part of every electronic device. Even though voltage converters are well-known circuits, continuous improvements in conversion efficiency, power throughput, size scaling, and cost are still being pursued. Inductive voltage converters offer higher power throughput and wider conversion ratios at higher efficiencies compared to their capacitive-only counterparts. However, inductive components in fully integrated form remain the bottleneck in these designs, especially in standard bulk technologies. In our effort to enhance efficiency of fully integrated inductive voltage converters for low-power applications, we designed and fabricated a set of standard PDK inductors along with two custom-designed inductors in a standard 65 nm UMC technology.

Description

The fabricated chip consists of five inductors designed to serve as the main energy-storage elements in a switched-mode voltage converter. The goal for each structure was to achieve the best possible frequency characteristics for the intended use that includes the highest inductance (L), the highest quality factor (Q), and the lowest series resistance (Rs) in the frequency range up to VHF band (<300 MHz). For inductors available in the PDK (one square inductor - IND1, and two circular inductors - IND2, IND3), this meant designing them with the largest diameter and widest traces allowed by the DRC. The individual turns were then connected in series or in parallel to obtain optimal L while maintaining reasonably low Rs. The same principle was applied to the two custom-designed inductors (irregular octagons - IND4, IND5), which were further enhanced using advanced layout techniques (e.g. tapering, slicing, and equal path-length routing) to suppress parasitic effects such as eddy currents and the skin effect. Although these two structures were identical in geometry, one included a Patterned Ground Shield (PGS) to reduce power dissipation caused by parasitic capacitance between the inductor and the substrate. Beneath the PGS, an integrated capacitor, using native NMOS transistors, was implemented and provided a capacitance of 1.6 nF for further improvement of the voltage converter density.

Results

The comparison of five inductors was performed by simulations results from Cadence Virtuoso and ANSYS Electronics Desktop. Obtained results were then compared to the results of measurement of fabricated prototypes that confirmed suitability of custom designed inductors for intended purpose in voltage converter and significant improvement compared to the inductors available in PDK. The simulated and measured frequency characteristics are shown in Fig.3. (omitting IND1 characteristics due to heavy distortion of simulated results from the measurement and from other inductors). The inductor structure with PGS

and integrated capacitor was used in the first prototype of the energy harvesting system based on solar cell and boost voltage converter. This first prototype system provides stable output voltage of 1.5 V up to 0.5 mA and successfully operates with the maximum power conversion efficiency of 40%.

Why Europractice?

Europractice is one of the most efficient, valuable and cheapest ways to fast prototype integrated circuits for European research-based environments. For university research in our case, Europractice was definitely the choice. Europractice, in particular with the support of imec to check physical design errors and for general support for fabrication, enables well-controlled design time, efficiency and support during all prototyping phases. With the parallel providing of design tool service, Europractice represents a unique, and well consolidated means for the European researchers to make their application-specific designs come true on silicon.

Fig.2.: Photo of fabricated chip samples.

Acknowledgements

This work was supported in part by the Slovak Research and Development Agency under grants APVV-23-0071, VV-MVP-24-0313 and VEGA 1/0705/24.

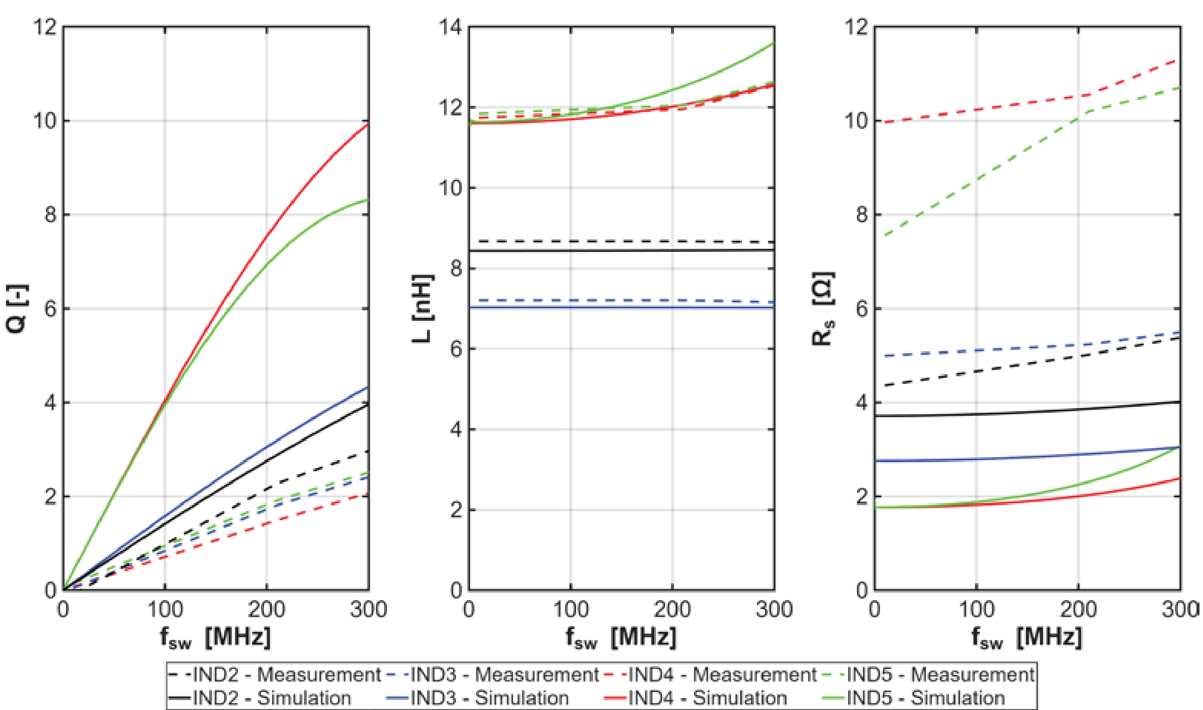

Fig.3.: Frequency characteristics of the fabricated inductors.

3D-integration of an electronic-photonic co-design

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Technology:	X-FAB XH018
Die Size:	1.52mm x 1.52mm (mini@sic)
Design Tools:	Cadence: Virtuoso, Genus, Innovus
Application Area:	Datacom / Telecom

Introduction

Scope of this design is addressing the issue of scalability in the problem of real-time reconfiguration of programmable photonic integrated circuits (PICs), a class of devices that implements arbitrary linear functions directly in the optical domain, ideally enabling “computing at the speed of light”. PICs, usually implemented as matrices of interferometers, become programmable only when they are provided with an electronic control layer, which drives actuators on the silicon photonic die in order to both set the desired working point and stabilize it against time-varying fluctuations (ageing, temperature, turbulence affecting the input signal...). As PICs grow in complexity, a scalable architecture is needed for the controller, somehow shifting the “application-specific” paradigm from photonics to electronics and reducing the cost in terms of area and power, compared to board-based solutions [1,2].

Description

In this design, we propose a 3-channel integrated controller, suitable for performing on/off switching of photonic devices. The ASIC closes three independent feedback loops around the interferometers of the PIC: light is sensed with a photodiode integrated close to the waveguides, and the working point is set by driving two thermal actuators. The ASIC exploits the dithering lock-in technique [3] to precisely steer the optical power towards the desired output of the interferometer, without requiring any prior calibration. The electronic channel features a custom-designed 10-bit, 117 ksps ΣΔ-converter to feed the photogenerated current to the digital circuitry that implements the control algorithm. The operation of the driving stage relies on a delay-locked loop cell to drive the actuators with a 10 MHz PWM signal, with 9-bit resolution, corresponding to a minimum time step of 200ps.

To push electronic-photonic integration further, ASIC and PIC are assembled in a flip-chip arrangement (Fig.1). Distributing the pads all over the ASIC eases the shoreline limitation that arises with wire-bonding as the number of photonic devices increases: if the electronic channel matches the size of the interferometer, the controller modular architecture can ideally be replicated seamlessly.

Results

The PWM-based driving stage implements a linear-by-design relation between the digital input fed to the DAC and the phase shift induced in the waveguides, the latter being proportional to the heat dissipated by the actuators. In continuous-time actuation schemes, a quadratic distortion is instead present between the applied voltage and the

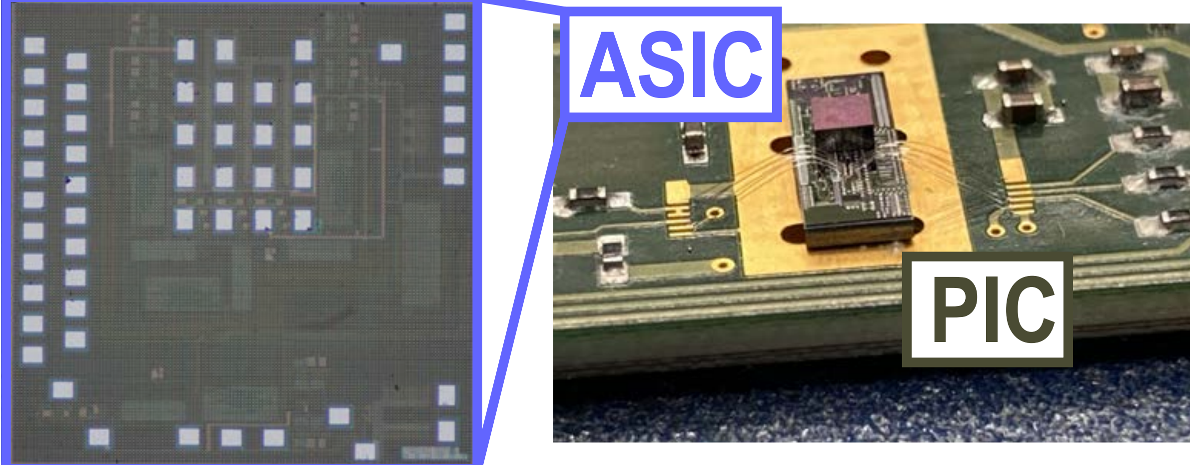

Fig.1: ASIC micrograph and 3D-integration of PIC (below, glued to PCB) and ASIC (flipped onto the PIC).

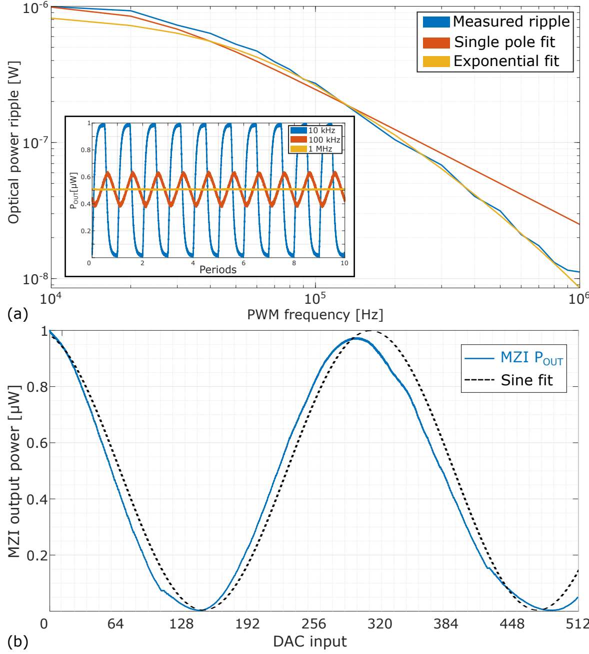

Fig.2: (a) Evaluation of the output thermal ripple and (b) characterization of a MZI.

resulting phase shift, causing an overall behavior of the control loop that depends on actuators bias.

Fig. 2a shows the evaluation of the residual thermal ripple on the optical output power as a function of PWM frequency, demonstrating an exponential-like heat low-pass filtering action by the silicon crystal and justifying the selected frequency; Fig. 2b, instead, displays a DC sweep of a Mach-Zehnder interferometer (MZI) output power with respect to the control variable determined by the digital algorithm, correctly deriving a sinusoidal function, not affected by distortion.

Why Europractice?

Through Europractice, we accessed X-FAB's mini@sic runs, providing tailor-sized, modularly scalable dies for our applications. Also, a comprehensive CAD suite lets researchers work with professional-grade software.

Acknowledgements

The Authors acknowledge PoliFAB, the micro and nano fabrication facility of Politecnico di Milano, for wire-bonding the chiplet and XGLab S.R.L. for the ball-bonding operation.

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Hybrid Stimulation for a Visual Prosthesis

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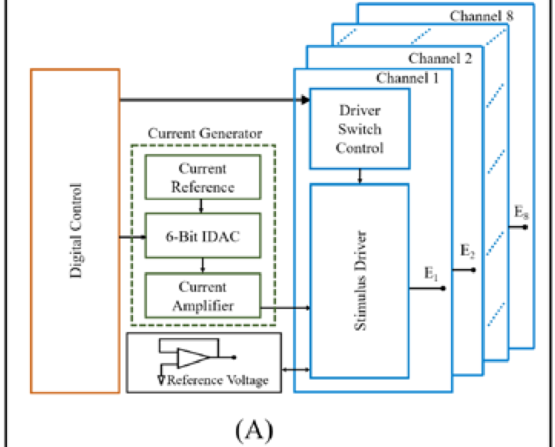
Technology:	X-FAB XT018
Die Size:	1.520mm x 1.520mm
Design Tools:	Cadence Virtuoso
Application Area:	Medical / Health

Introduction

Advancements in neural stimulation are essential for improving the precision and efficiency of visual cortical prostheses, which currently struggle with limited spatial resolution, non-specific activation, and high-power consumption [1]. Electrical stimulation activates broad neuron groups, while optical stimulation suffers from shallow penetration and higher power demand. To overcome these limitations, this chip uses a multipolar hybrid approach that combines layer-specific electrical and optical stimulation with polarity switching, selective electrode routing, and subthreshold control. This coordinated strategy activates only the intended cortical columns, enabling higher spatial resolution, improved neural specificity, and reduced power consumption. The proposed design has been implemented in a fabricated chip, demonstrating an efficient microelectronic solution for visual restoration, pending in-vivo evaluation.

Description

This project focuses on designing the stimulator circuits within an implantable closed-loop SoC for neurostimulation, with the fabricated prototype emphasizing the core electrical and optical subsystems (Fig. 1A and 1B). The chip, fabricated in XFAB SOI 0.18 μm (XT018), integrates 14,509 devices within a 2.31 mm² area (1520 μm × 1520 μm). The electrical subsystem includes eight stimulation channels driving electrodes E1–E8, each with its own switch control and stimulus driver. A dedicated digital control block determines the required current level, controls the global current generator, and manages timing, channel selection, polarity switching, and stimulus sequencing. A buffer sets the defined reference voltage. The optical subsystem is designed with four driver channels for LEDs LED1–LED4, with its own



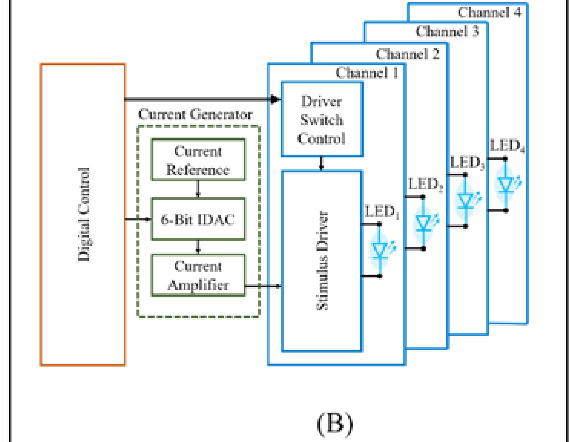


Fig.1: Hybrid stimulation system for visual prosthesis. (A) Block diagram of the implemented eight-channel multipolar electrical stimulator subsystem. (B) Block diagram of the implemented four-LED optical stimulator subsystem.

shared current generator and buffer, controlled by a dedicated digital block, differing only in the internal stimulus driver design. The digital block also handles timing, channel selection, and stimulus sequencing. As a hybrid strategy, the system applies subthreshold electrical and optical stimuli—below standalone activation thresholds—so neurons fire only when both inputs overlap spatially and temporally, enabling fine-tuned stimulation, improved selectivity, and reduced power consumption[2].

Results

The successful fabrication of the hybrid stimulation chip on X-FAB (Fig.2) demonstrates the feasibility of integrating all digital control logic and both stimulation subsystems into a single 2.31 mm² die. Prototypes received from Europractice were tested in the lab, confirming reliable operation with a 5 V supply. Measurements showed the electrical drivers deliver biphasic currents (cathodic and anodic phases) with different loads, showing that the current remains stable under varying conditions, as designed in the chip, under the control of the custom digital block (Fig.3), while the optical subsystem maintained stable anode–cathode voltages relative to the specified reference voltage (2.5 V) under active and inactive conditions (Fig.4). These results align with pre-silicon simulation data, indicating that the core stimulator subsystems, managed by the digital control block, function as intended and are ready for the next phase of detailed testing and integration into a complete system for in-vivo studies.

Why Europractice?

Access to advanced semiconductor fabrication processes such as XFAB SOI 0.18 µm (XT018) is typically challenging for academic research groups. Europractice provided essential, cost-effective, and timely access to the X-FAB foundry through the mini@sic runs. This support greatly reduced risk during the prototyping phase of this complex hybrid stimulation design. Without Europractice, the financial and logistical barriers to fabricating and testing the chip would have been prohibitive, and their assistance accelerated the research timeline by several months.

References

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[2] Abdo E.A., Yakovlev A., Degenaar P. Multipolar Hybrid Stimulation for Visual Prostheses: Enhancing Resolution and Specificity. Annual Int. Conf. IEEE Eng. Med. Biol. Soc., vol. 2025, pp. 1–7. 2025. https://doi.org/10.1109/EMBC58623.2025.11254606.

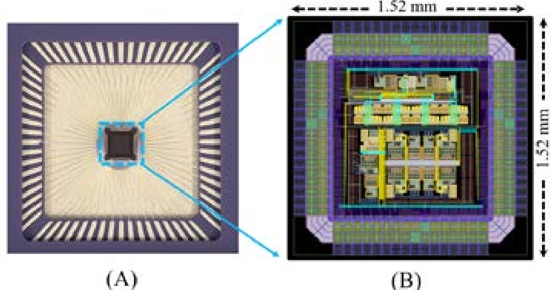

Fig.2: (A) Fabricated hybrid stimulation chip (B) Chip layout.

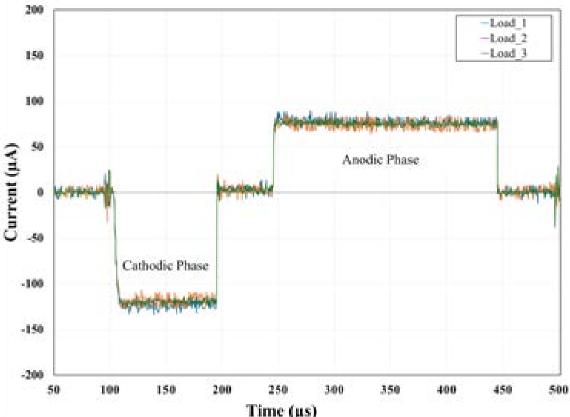

Fig.3: Electrical stimulation: Biphasic currents under varying loads, managed by the digital control block.

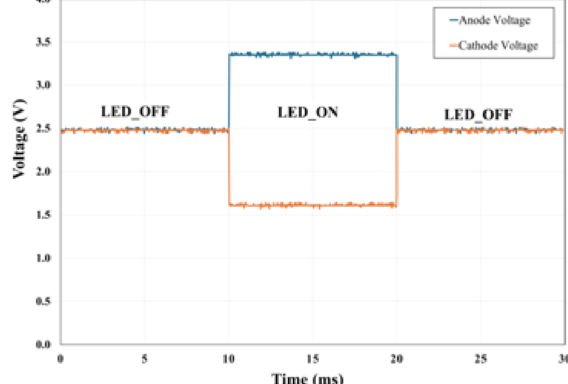

Fig.4: Optical stimulation: Anode–cathode voltages of an LED under active and inactive conditions relative to the specified reference voltage (2.5 V).

Digital GaN and SiC Gate Driver With On-Chip Burst-ADC Switching Transient Monitoring for Closed-Loop Drive Profile Optimization

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Contacts:	Erik Wehr, Kenny Vohl, Tom Herzog, Leon Weihs, Tobias Zekorn, Ralf Wunderlich, Stefan Heinen
E-mail:	mailbox@ias.rwth-aachen.de

Technology:	X-FAB XT018
Die Size:	3mm x 3.1mm
Design Tools:	Cadence Virtuoso, Spectre, PVS DRC/LVS/PEX, Genus, Innovus, Xcelium
Application Area:	Automotive / Transport

Introduction

The superior switching performance of wide-bandgap semiconductors enables more efficient and highly compact power converter systems. However, the fast switching transients lead to increased overshoots and electromagnetic emissions (EME), limiting the achievable performance gains in many applications.

Compared to conventional gate drivers, active gate driving with an optimized drive profile achieves a significant improvement of the inherent trade-off between switching loss and overshoot/EME. This approach can effectively maximize the performance gain of wide-bandgap devices. However, selecting the optimal drive profile is challenging due to its sensitivity to operating condition variations.

Description

The designed digital gate driver IC enables a closed-loop drive profile optimization that adaptively adjusts the gate drive profile depending on the operating condition of the power transistor. As shown in Fig.2, it integrates a programmable current-source/sink-based gate driver stage together with a high-speed burst-mode ADC that monitors the switching transients of the power transistor's terminal voltages, providing the feedback for closed-loop optimization.

Drive profiles with up to 32 segments and a timing resolution of 150 ps can be programmed via SPI. The current resolution is 40 mA with a maximum drive current of ±5 A.

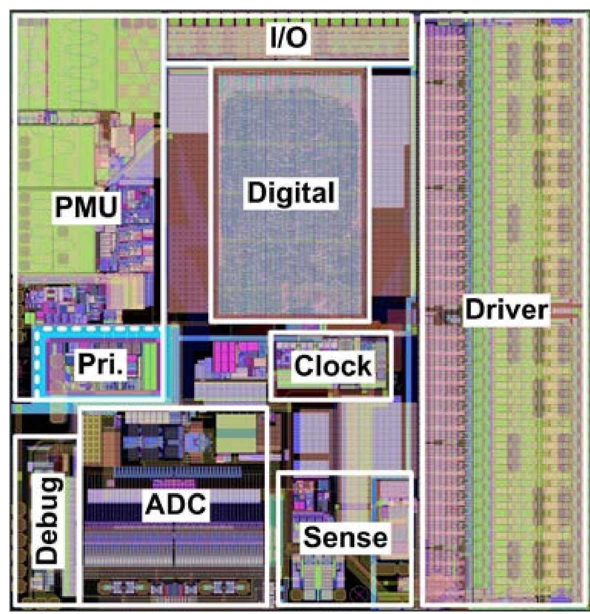

Fig.1: Layout of the digital gate driver.

The architecture of the gate driver stage is designed for a wide supply voltage range from 5 V to 25 V and is therefore able to drive both SiC and GaN transistors.

The feedback path consists of capacitive voltage dividers that scale down the terminal voltages of the power transistor to the ADC input range, followed by the burst-mode ADC that digitizes the switching transient waveforms. The key metrics of the switching transients, such as overshoot as well as di/dt and dv/dt slew rate, can be extracted and used as feedback to iteratively adapt the drive profile. The burst-mode ADC uses 32 parallel track-and-hold channels to capture the switching transients with a burst sampling rate of 2.5 GS/s. During the idle time between the switching events, an 8-bit noise-shaping SAR ADC sequentially converts the captured samples.

To realize the timing resolution of 150 ps in 180 nm HV CMOS technology, an 8-phase interleaved timing architecture is implemented using an 8-phase PLL clock synthesizer with background phase skew calibration.

Results

Fig.3 shows a simulation of a GaN switching waveform. The burst-mode ADC accurately captures the drain voltage transient, enabling extraction of the dv/dt slew rate, as well as ringing frequency and amplitude from the digitized waveform. Based on this information, the gate drive profile can be iteratively adapted to maintain optimal switching performance.

Characterizing the prototyped IC within a power converter system will provide further insight into the operation and achievable performance gain of the proposed digital gate driver.

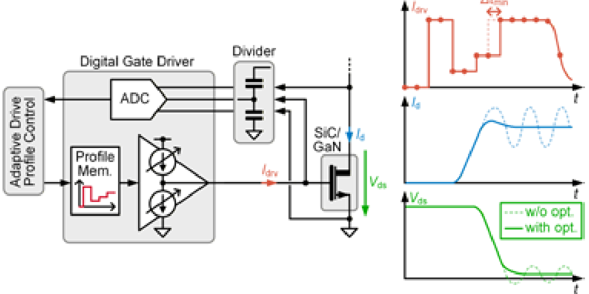

Fig.2: System overview of the digital gate driver.

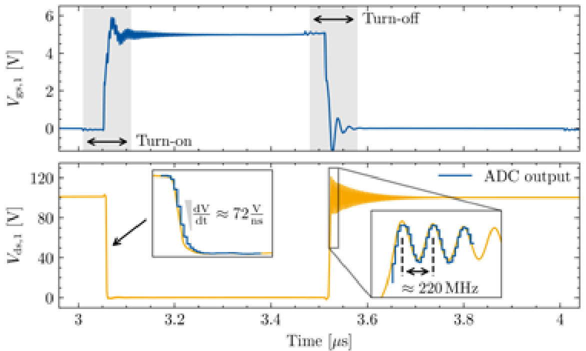

Fig.3: Simulated switching transient monitoring with burst-mode ADC [2].

Why Europractice?

The Europractice mini@sic and MPW programs offer an invaluable platform for silicon prototyping for universities and research institutions. The fast and cost-effective access to state-of-the-art fabrication technologies and EDA tools provides essential support for the progress and success of microelectronics research.

Acknowledgements

We would like to express our gratitude to Europractice and imec for providing a state-of-the-art prototyping platform and for their excellent support during this tapeout and throughout the last years.

This research was supported through the projects EVoReso (Grant No. 19I22013D) and HiPower 5.0 (Grant No. 101194250).

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FASXCAM - Fast Soft X-ray Camera

Czech Technical University in Prague, Czech Republic

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E-mail: zdenko.janoska@fjfi.cvut.cz

Technology: X-FAB XT018
Die Size: 4000μm × 6878μm
Design Tools: Cadence
Application Area: High Energy Physics (HEP)

Introduction

This ASIC design, named Fasxcam (Fast Soft X-ray Camera), addresses the critical need for monitoring high-temperature plasma and other time-varying soft X-ray sources. Fasxcam is a monolithic active pixel sensor developed for ultra-fast soft X-ray sensorics for spectral monitoring of high-temperature plasmas, for imaging and advanced dosimetry, designed in 180 nm high voltage (HV) silicon on insulator (SoI) CMOS technology (Fig.1). The primary function is to study spectrally resolved emission in the energy range of 4 to 20 keV, which is particularly important for analyzing impurities emissions like that of Wolfram. The Fasxcam is engineered to measure the energy of each detected quantum and offers operational flexibility through two modes: a Frame mode and a Rolling shutter mode.

Description

The Fasxcam sensor has a core resolution of 64×64 pixels. This design employs a large, thick pixel size of 60×60 μm to enhance sensitivity and detection efficiency. The system is engineered for precise spectral monitoring, covering an energy range from 4 keV to 20 keV with a high energy resolution of 300 eV, enabling the measurement of the energy of each detected quantum within every pixel.

The chip incorporates an 8-bit output Successive Approximation Register (SAR) ADC, utilizing a Capacitor Array Structure (CDAC) for efficient conversion. This architecture supports a maximum frame rate of 15 kHz. The sensor operates on a low power supply of 1.8 V, drawing approximately 20 mA, resulting in a low power consumption of only 36 mW

Data communication relies on LVDS for high-speed clock and data transmission, supporting a clock frequency up to 400 MHz, while control signals use standard 1.8 V logic. The pixel logic is designed to be highly functional, capable of

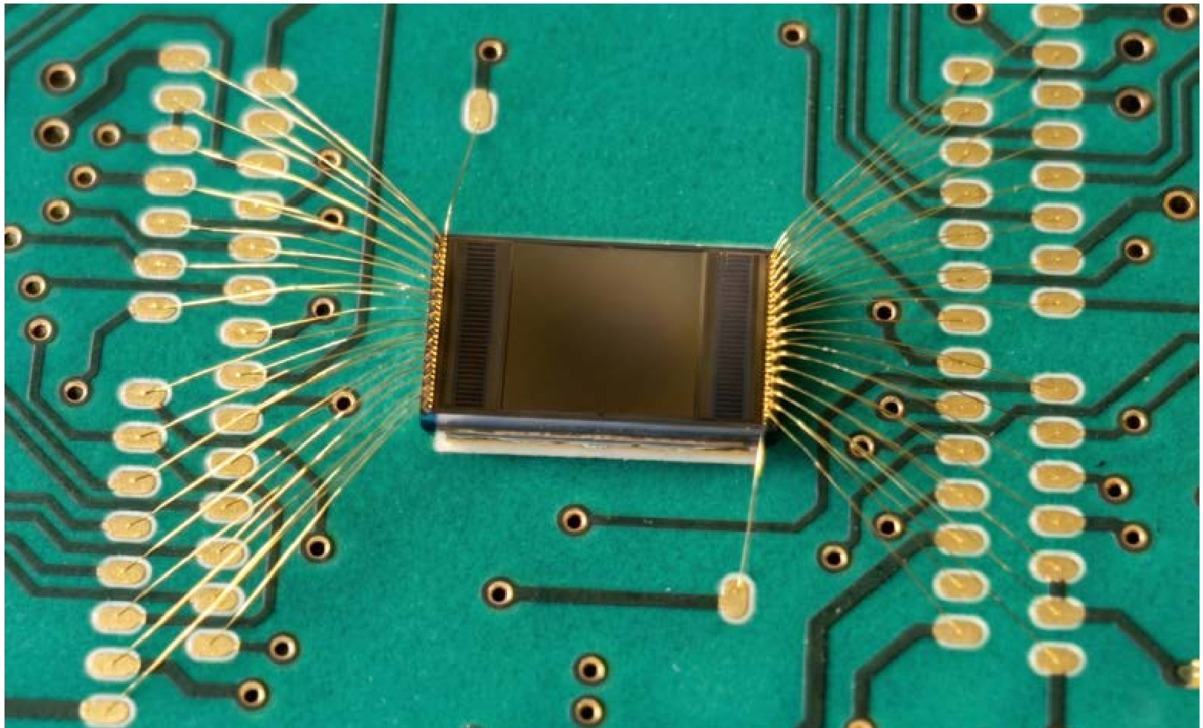

Fig.1: FASXCAM sensor assembled on PCB.

detecting a hit and holding the maximum value (peak energy) registered during the exposure time, with a corresponding digital output.

Results

A comprehensive testing program was conducted on the prototype and preliminary samples to validate the ASIC's performance and stability.

Fig.2 shows the standard deviation of 32,000 frames of video to demonstrate hit distribution when observing the week α emitter on air. The emitter has energy above 20 keV, causing pixel saturation for every hit.

Fig.3 shows the measured spectrum of the ^{55}Fe emitter with the peak at energy 5.89 keV, calculated from 10,000 frames with an exposure time of 10 ms for a 60 V bias voltage, after pixel calibration.

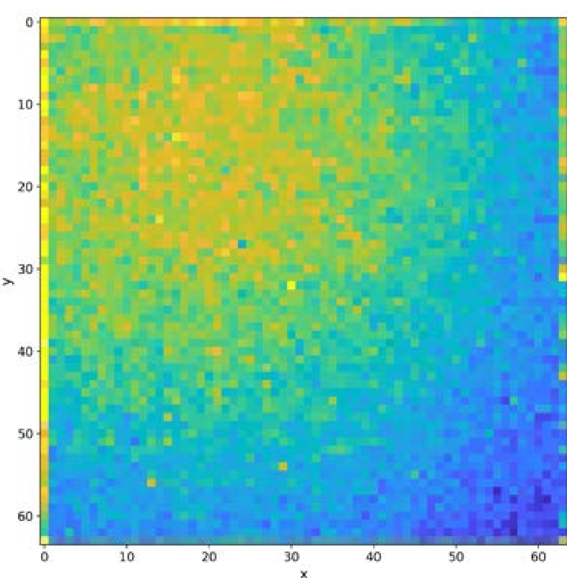

Fig.2: Standard deviation of 32k frames observing the weak α emitter, showing hit distribution.

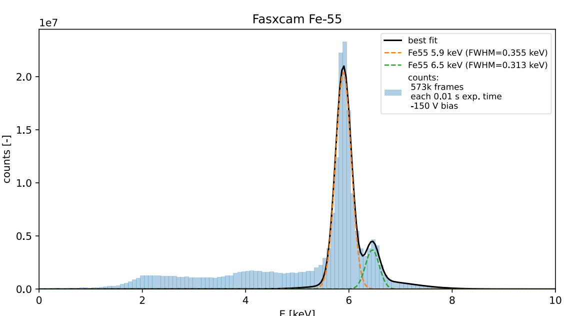

Fig.3: Spectrum of 55Fe emitter.

Why Europractice?

Our research group has maintained a successful and enduring collaboration with Europractice over several years. This partnership is vital to our design pipeline, as imec consistently provides exceptional technical support, which is absolutely crucial for the successful submission and realization of our integrated circuit designs. Furthermore, imec's team offers highly responsive and qualified assistance with all necessary administrative processes, streamlining our workflow significantly. Thanks to our long-standing engagement with Europractice, we benefit from privileged access to a wide range of advanced semiconductor technologies at an affordable and accessible price point.

A wide Dynamic Range Programmable Gain Interface for SiPM based Bio-photonics capture In-Vivo

MCCI, Tyndall National Institute, Ireland

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E-mail:	Daniel.ohare@mcci.ie

Technology:	X-FAB XT018
Die Size:	1mm x 1.4mm
Application Area:	Medical / Health

Introduction

Research carried out in the Bio-Photonics group in Tyndall National Institute has demonstrated the efficacy of combining autofluorescence with diffuse reflectance spectroscopy, to offer a multimodal approach for more accurate tumour margin detection [1]. However, the benchtop system needed to be miniaturised to create a system that is easy to use in surgical operating theatres and to enable in-vivo tumor margin detection. As part of the EU MedPhab pilot line project a miniature device is created. The device is designed as an interface to a Silicon Photomultiplier (SiPM). The complete device will combine a high Dynamic range current to digital converter and a voltage multiplier to provide the 30V reverse bias required by the SiPM. XT018 enables the realisation of both functions.

Description

Bio-Photonics use the interaction of light with tissue to investigate tissue composition and properties. Previous studies have established that Silicon Photomultipliers (SiPMs) are highly suitable for high-sensitivity and in-vivo Bio-Photonics applications, enabling detection of optical power theoretically as low as 1 pW.

The signal produced by the SiPM is a current, generated proportionally to the amount of light detected by the sensor. Traditional signal chains employ a transimpedance amplifier (TIA) to convert the input photocurrent into a voltage signal, which is then filtered and digitised by a conventional ADC. In contrast, direct conversion analogue front-ends eliminate the voltage conversion step, enabling direct current-to-digital conversion. This approach reduces the number of stages in the signal chain, reducing the noise and power consumption.

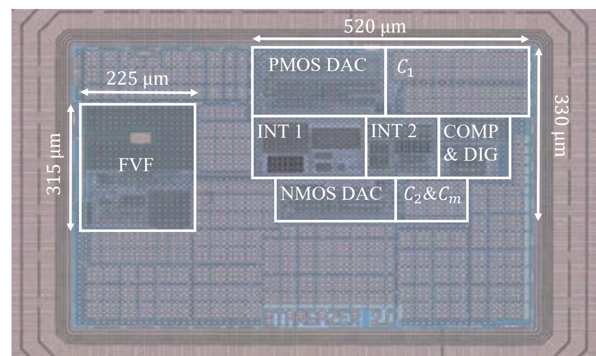

Fig.1: Die photograph showing the main circuits.

A Flipped Voltage Follower (FVF) is used as a current buffer amplify or attenuate the SiPM photocurrent, followed by a current-input Delta-Sigma (ΔΣ) modulator. The FVF acts as a variable gain stage to increase the dynamic range of the converter. The FVF has three modes and can attenuate the input current by factors of 1, 10 and 100 and amplify the current by a factor of 10. The FVF is followed by a 2nd order continuous time ΔΣ modulator used as a current to digital converter. The modulator employs the Cascade of Integrators with Feed- Forward and Feedback (CIFF-B) loop filter topology. This work occupies an active area of 0.23 mm^2, 0.07 mm^2 of which is the FVF and 0.16 mm^2 is the modulator.

Results

Two type of measurements were performed, electrical and optical measurements.

A. Electrical Measurements:

Electrical measurements were conducted by injecting a sinusoidal current with varying amplitude at 1.2kHz into the FVF input. The system achieves a dynamic range of 114 dB across different FVF gain modes, with input currents spanning from 4.8 nA to 2.5 mA. Within a signal bandwidth of 30 kHz, the AFE can achieve a peak SNDR of 59.5 dB, at a FVF gain of 1, resulting in an ENOB of 9.6 bit. Pronounced harmonic distortion is caused by both DAC mismatch and the single-ended nature of the modulator. The noise floor of the system is measured at −100.4 dB, translating to a total input-referred noise of 91.1 pA/√Hz across the bandwidth.

B. Optical Measurements:

Preliminary results from the full system were obtained using an OnSemi MicroFC-10010 SiPM. Measurements were taken with an optical fibre directed at the SiPM. The incident light, generated by a 470 nm fibre-coupled

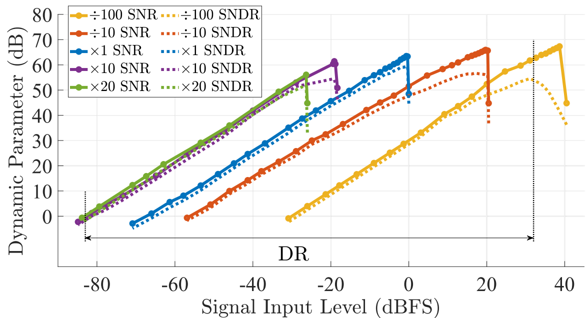

Fig.2: Electrical measurement results.

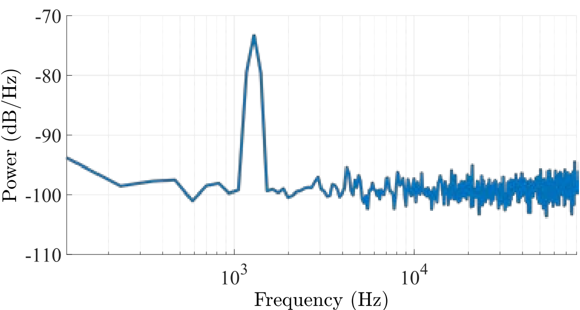

Fig.3: Optical measurement results.

LED, was attenuated using a combination of neutral density filters. Measurements have shown that light signals as low as 50pW can be resolved by the system.

Why Europractice?

Europractice gives research institutes like Tyndall a lower cost way to access advanced CMOS technologies. The MPW and mini@sic programmes give access to small area for quick low cost prototyping. The Europractice team members like Karthik Muga provide patient technical support and guidance to solve the DRC / chip finishing rules and help us get on the tapeout shuttles.

Acknowledgements

This work was funded by the EU MedPhab Pilot line project [2] and Microelectronic Circuits Centre Ireland [3].

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Entangled-photons optimisation in a tuneable resonator

University of Sheffield, the UK

Contact:	Imad I. Faruque
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Technology:	CORNERSTONE Si-Photonics 340nm SOI
Die Size:	5mm x 5mm
Design Tools:	Luceda
Application Area:	Quantum Technologies

Introduction

Quantum technology is a strategic research area worldwide, with the UK funding 5 national quantum hubs ranging from computing, communication, imaging, sensing and metrology. Quantum photonic integrated circuits is playing a key role in the national quantum mission, often requiring an optimised entangled photon-pair sources. This device has the tuneability to optimise the brightness of the source.

Description

The device design is very similar to classically well-known racetrack resonators with tuneable coupling regions implemented by a Mach-Zehnder interferometer.
The key difference for the quantum regime is the operational parameters (tuning parameters) of the coupling regime, which maximises the photon-pair generation extraction.

Results

The results confirm the theory that by tuning the coupling regime, we can significantly enhance (almost an order of magnitude) the photon-pair detection rate with lower signal-to-noise ratio. Thus, future more complex circuits can be built with these high brightness devices. Also, the simplicity and well-known classical design enable replicability without needing special fabrication needs.

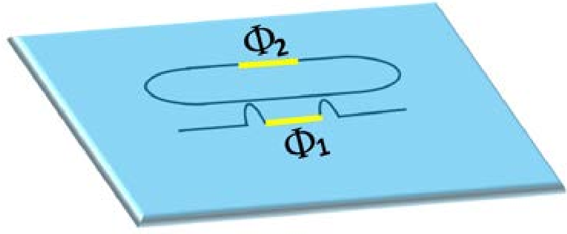

Fig.1: Micro resonator with tunable light coupling to optimise the brightness.

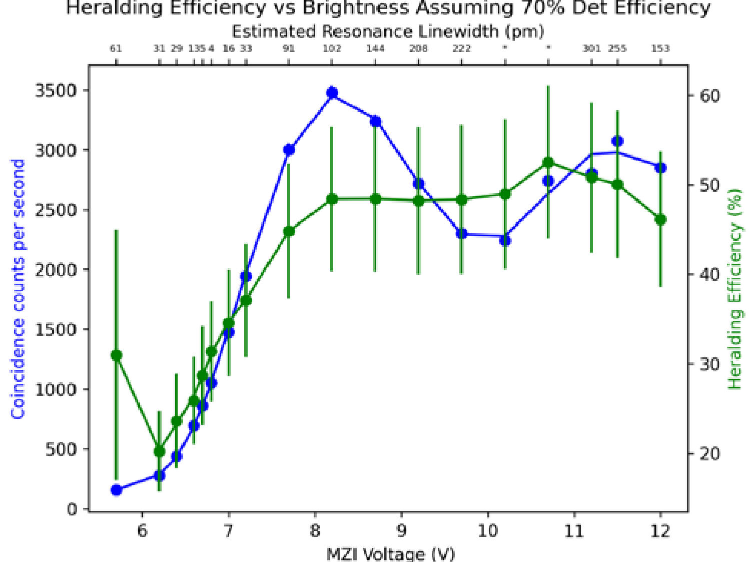

Fig.2: Coincidence rate and heralding efficiency as a function of MZI voltage.

Why Europractice?

Accessing CORNERSTONE, part of the Europractice offer, was important because of the technology portfolio that enables our work. With the CORNERSTONE Photonics Innovation Centre (C-PIC) programme, the MPWs were affordable, opening up the opportunity for us to develop our research prototypes. The processes used in fabrication are industry standard, allowing our research to move from hero experiments to scale-up ready development. The Open Platform also allows us to further our impact and reach, as we can share our published research designs in the public PDK, enabling the global scientific community to build on our learnings and accelerate the route to successful designs.

References

Nathan Moses, Siddarth Joshi, Alex Clark, and Imad Faruque "Optimising heralding efficiency and brightness of a micro-ring resonator by tuning coupling regime", Proc. SPIE 13376, Quantum Sensing and Nano Electronics and Photonics XXI, 1337605 (21 March 2025); https://doi.org/10.1117/12.3041869

Silicon Photonics for Optical Detector Readout

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Contacts:	Marc Schneider
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Technology:	imec Si-Photonics iSiPP50G
Die Size:	10.45mm x 5.15mm
Design Tools:	Synopsys OptoDesigner
Application Area:	High Energy Physics (HEP)

Introduction

Detectors for particle physics and photon science deliver ever increasing volumes of data, which have to be transferred from harsh radiation environments to the data acquisition system in a radiation-free zone. Silicon photonic modulators in the detector volume are promising transmitters, able to deliver high bandwidths, to reduce power requirements, and to survive the conditions inside a detector. Additionally, wavelength division multiplexing (WDM) increases the transmission bandwidth of a single fiber, reducing the total fiber count for a detector.

Description

We already designed several silicon photonic chips in the past, but the COTTONTAIL chip (Fig. 1) was the first in imec's iSiPP50G technology. Besides several test structures, it includes different types of compact Mach-Zehnder modulators (MZM) with pn-junctions in push-pull configuration in the gaps of a single coplanar transmission line. Additionally, thermal modulators were added to some of the modulators for efficient working point control. Those modulators were also used in two WDM systems with four modulators and optical (de)multiplexers. The (de)multiplexers were realized as planar concave gratings (PCG), which offer very low losses and good channel separation. While the current WDM systems require only four wavelength channels, for which the PCGs are rather small, we also realized 8-channel and 32-channel PCGs for the C-band around 1550 nm.

Components of our own design use the majority of the available chip area, but we also included ring modulators and several Ge-photodiodes from the process design kit (PDK). Especially the ring modulators are interesting, as they offer a very high bandwidth while using up very little space, and they can be cascaded to WDM systems without additional optical (de-)multiplexers.

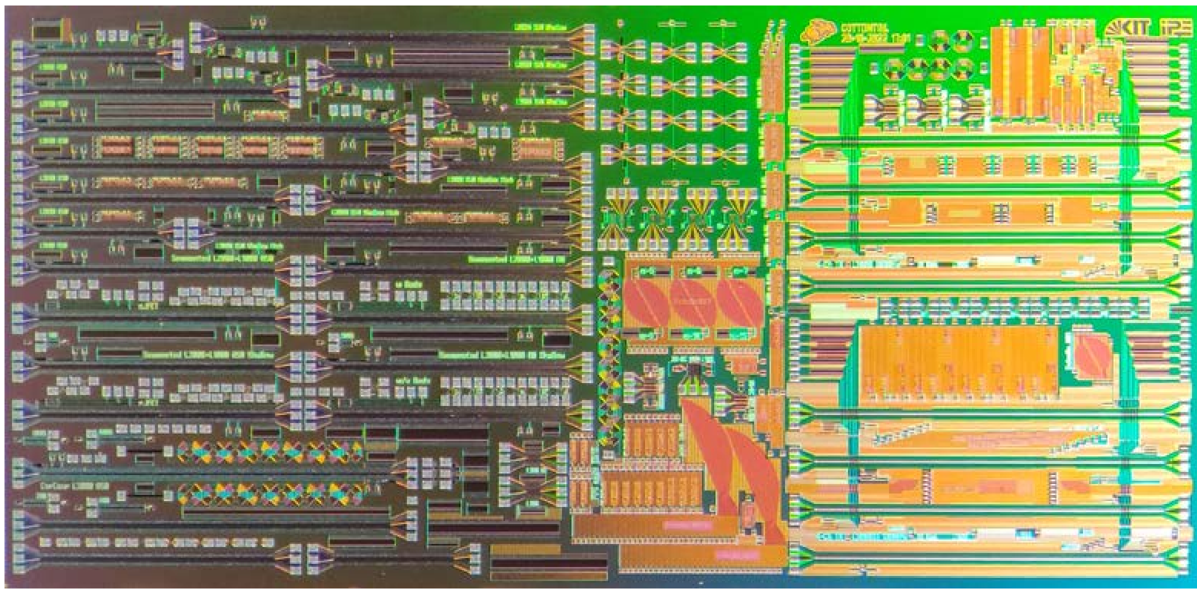

Fig.1: Micrograph of the COTTONTAIL chip.

All photonic components are connected to very efficient grating couplers from the PDK, which allow the coupling to optical glass fibers anywhere on the chip surface with a good mode matching.

Results

Fig.2 shows the frequency characteristics of some of our MZM designs of different lengths. While the shorter ones show a rather high bandwidth, the longest MZM shows a very high efficiency at low frequencies with a steep initial drop to higher frequencies and a plateau, resulting in a rather low cut-off frequency. The reason for the pronounced peak at the beginning of the frequency trace has still to be clarified. The 4-channel PCGs, whose transmission characteristics are shown in Fig.3, exhibit very low losses (1.6 – 2.3 dB) and a crosstalk of less than 25 dB. The wavelength channels are slightly shifted, which transforms into a silicon thickness deviation from the ideal value of 1.1 nm, which is well within the specified fabrication tolerance.

Recently we performed experiments where MZMs and ring modulators were irradiated with X-rays until the modulation efficiency dropped significantly. Fig.4 shows a ring modulator sample for the experiments with a diced part of the COTTONTAIL chip, a breakout board with electrical connector and the fiber-chip coupling using angle-polished glass fibers. First results show that the radiation-hardened versions of our MZMs survive up to 4.5 MGy and can be revived through an annealing procedure. The same applies to the ring modulators from the PDK for doses up to 3 MGy.

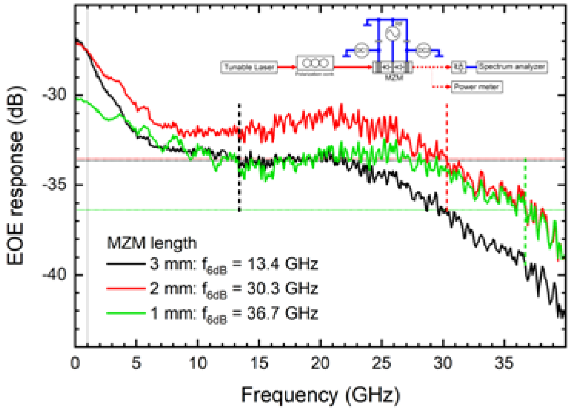

Fig.2: Frequency characteristics of deep etched MZMs of different lengths.

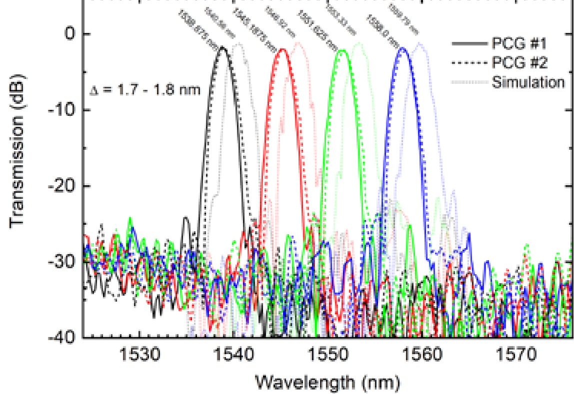

Fig.3: Transmission characteristics of two 4-channel PCGs and their simulation.

Fig.4: Sample for irradiation experiments on ring modulators.

Why Europractice?

Taking part of a multi-project-wafer run through Europractice was an affordable way for us to design high-quality silicon photonic chips and get them fabricated. Without this access to tools and foundry services, it would have been extremely difficult to develop and produce the COTTONTAIL chip or similar silicon photonic components. Additionally, imec's silicon photonics support team was invaluable for finishing the design.

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Demonstration of High-Frequency Self-Pulsing Oscillations in an Active Silicon Microring Cavity

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Technology:	imec Si-Photonics iSiPP50G
Die Size:	2.5mm × 2.5mm
Design Tools:	Synopsys OptoDesigner, KLayout
Application Area:	Datacom / Telecom

Introduction

Silicon photonics is a key technology for integrated optical communication and artificial neural networks, enabling compact, low-power, and CMOS-compatible devices. Silicon microring resonators are especially attractive due to their small footprint, high quality factor, and strong nonlinear effects, making them suitable for neuromorphic and high-speed communication applications. This report presents experimental results from silicon microring resonators fabricated at the imec foundry through Europractice services, designed to study nonlinear dynamics and optical self-pulsing in active and passive PIN- and PN-junction devices. Figure 1 illustrates the principle of self-pulsation and the waveguide cross-section with multiple doping levels.

Description

The prototyped silicon microring resonators study high-frequency self-pulsing and nonlinear dynamics. Fabricated on SOI with single-mode waveguides and optimized ring radii, they resonate in the telecom range. Bus-to-ring gaps enable near-critical coupling, and integrated PIN/PN junctions control free-carrier and thermal effects. Multiple microring variants, including passive and active designs, were implemented on the same chip to facilitate systematic comparisons and detailed time- and frequency-domain measurements.

Results

The fabricated devices demonstrated optical self-pulsing oscillations under continuous-wave excitation. Figure 2(a)

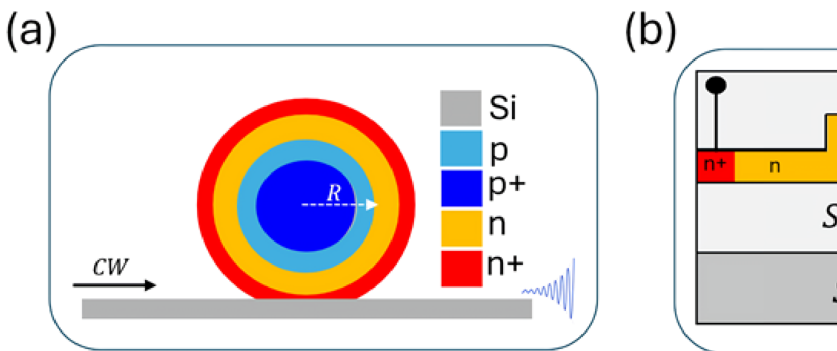

Fig.1: Self-pulsation in a silicon microring resonator (a) and rib waveguide cross-section with four doping levels (b). Adapted from [2].

shows the temporal behavior of normalized transmitted optical power for five oscillations at input powers from 1.57 to 2.08 mW without electrical bias. As input power increases, pulse recovery time grows due to enhanced thermo-optic heating, while stronger free-carrier effects are observed at 2.6 mW under a 100 mV reverse bias (Fig. 3b inset). The output exhibits oscillatory behavior with high extinction ratio and minor intensity fluctuations, producing a semi-random duty cycle (Fig. 3a). FFT spectra (Fig. 3b) reveal dominant frequency components around 15 MHz and 30 MHz, resulting from overlapping thermal and free-carrier oscillations. Noise sources include optical noise from the EDFA and electrical noise from DC probes, but intensity fluctuations remain below 8% of peak amplitude, making the devices suitable for applications such as all-optical spiking in photonic neural networks.

These results confirm that self-pulsing originates from coupled free-carrier dispersion, free-carrier absorption, and thermal nonlinearities. Active and passive devices display distinct oscillation regimes depending on optical power and electrical bias, validating the proposed design and enabling controlled high-frequency self-pulsation in silicon microring resonators.

Why Europractice?

We used Europractice to access imec's silicon photonics fabrication affordably. The service provided precise design kits compatible with standard CAD tools, making it easy to implement complex microring resonators reliably for our academic research.

Acknowledgements

The authors acknowledge IMEC and Europractice for fabrication support, as well as financial support from the German Research Foundation (DFG) and the German Federal Ministry of Research, Technology, and Space (BMFTR).

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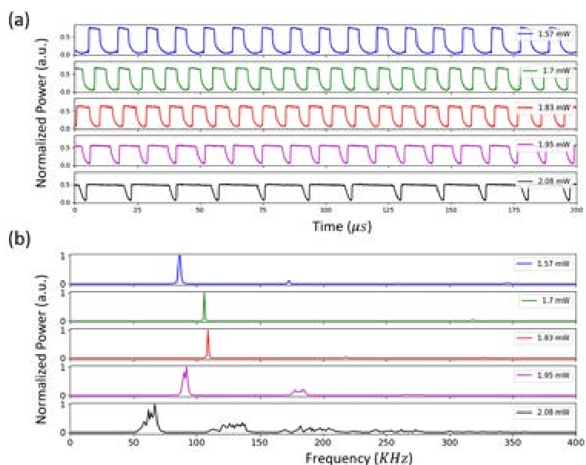

Fig.2: Time-domain output for five input powers (1.57–2.08 mW) at 3 pm detuning (a) and corresponding FFT spectrum (b). Adapted from [3].

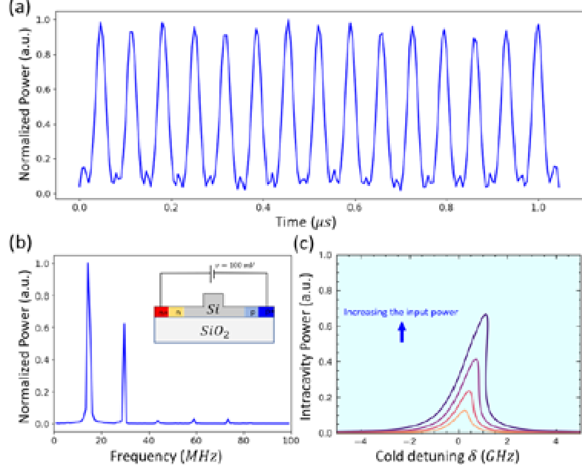

Fig.3: Output for 1.3 mW at 3 pm detuning (a), FFT spectrum with PIN bias inset (b), and normalized circulating power vs. detuning for four input powers (c). Adapted from [3].

DERMIS: A Flexible Fully-Integrated 600μm-Resolution Per-Taxel Slip-to-Spikes Tactile Sensor Readout on a-IGZO TFT for Large-Area High-Density Electronic Skins

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Technology:	Pragmatic FlexIC
Die Size:	3mm x 3mm
Application Area:	Medical / Health

Introduction

Fine grasp-state-dependent force sensing, performed by human hands during dexterous object manipulation, is crucial for e-skin solutions for robotic and neuroprosthetic applications. Depending on the current grasp state, tactile sensors need to sense with high spatial resolution a variety of contact parameters across a large area: a) normal force, b) shear force, c) slip (extracted from the friction coefficient, i.e., the shear force normalized to the normal force). Adaptive event-based signal acquisition is beneficial as both fast slip sensing (< 10 ms for safe grasping) and sparse spatiotemporal sampling (during periods of inactivity) are required.

Sensor-to-readout integration in Si-CMOS [1] addresses the above requirements with dense per-taxel connections but is expensive for large areas. Implementation in a flexible TFT technology offers a scalable alternative. To demonstrate this, a chip, called DERMIS, has been developed in the Pragmatic a-IGZO TFT process [2][3]. It combines capacitive shear sensors with event-based, reconfigurable readout in this large-area TFT technology to enable high-resolution grasp-state-dependent force sensing, including slip (Fig.1).

The Pragmatic a-IGZO TFT technology, optimized for large-area integration, differs from Si-CMOS in that the technology uses devices with lower carrier mobilities, coarser feature sizes, and currently has no PMOS devices yet. These device characteristics lead to a higher static power consumption in the dense digital logic and lower device and metal densities than in advanced Si-CMOS, so implementing the complex on-chip digital processing used in prior slip-extraction algorithms

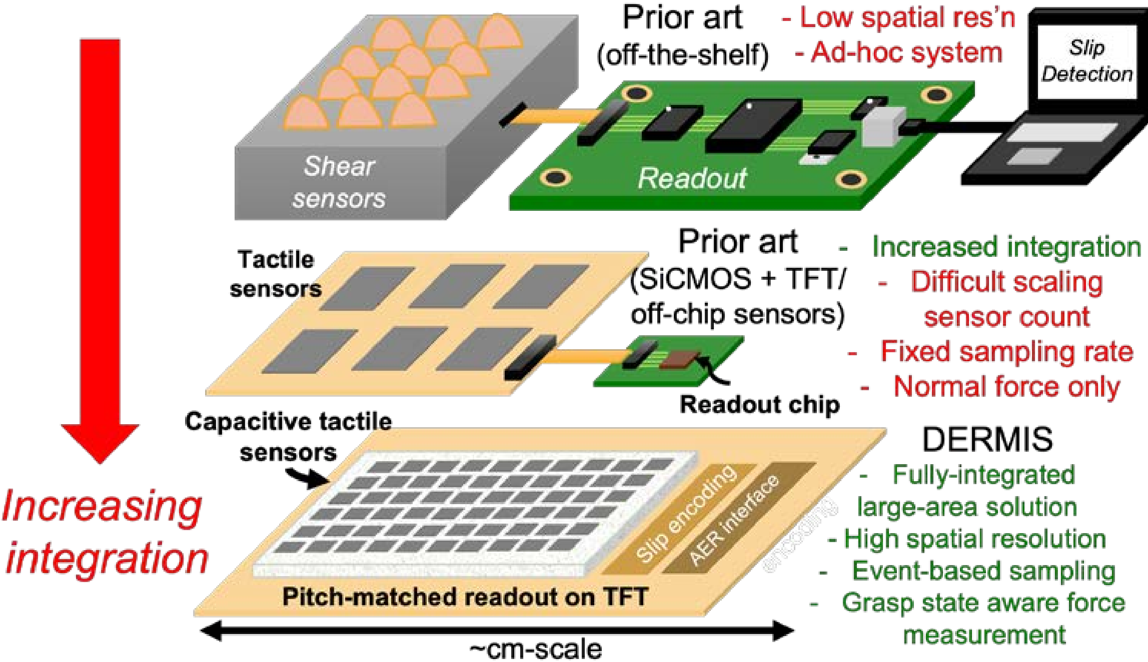
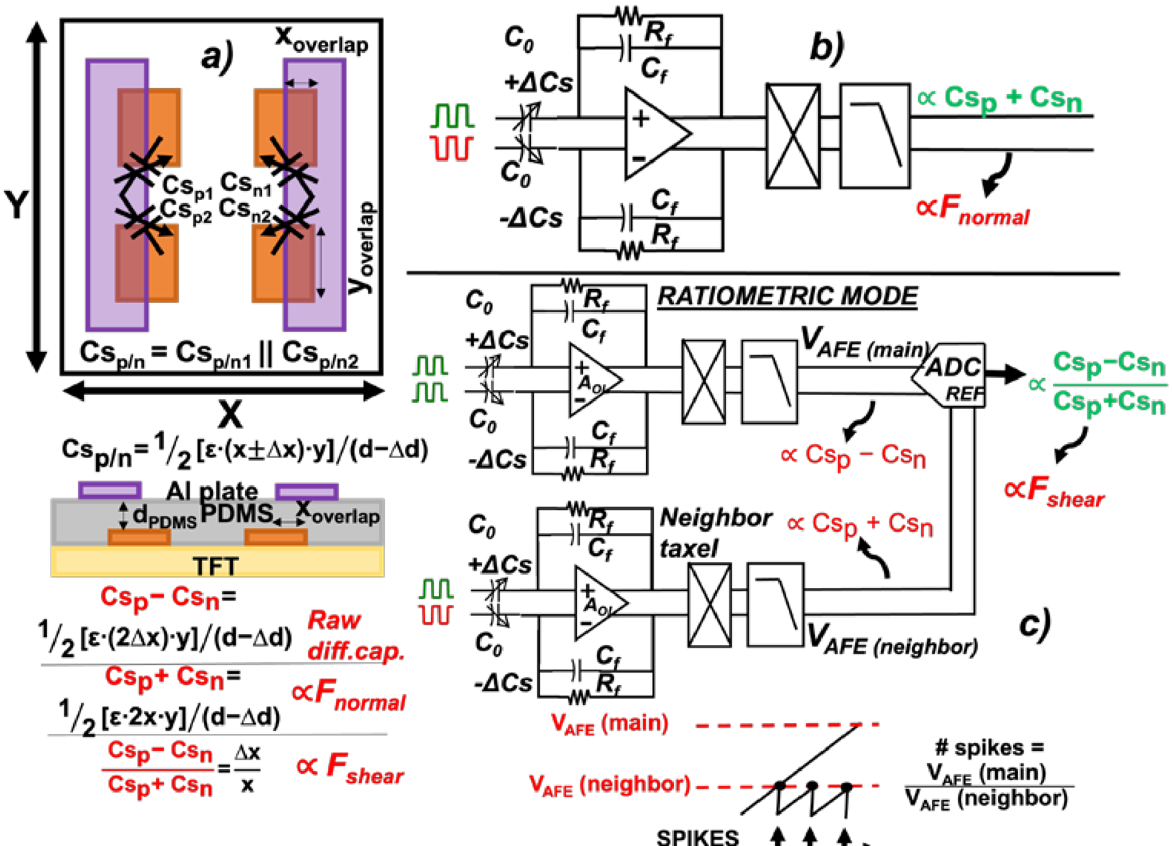


Fig.1:
a) Existing tactile sensing systems lack the level of integration to allow for power-efficient and low-latency slip detection.
b) Hybrid approaches are limited in scalability.
c) To match the high spatial resolution and the fast localized slip detection capability of human hands, next-generation slip detection systems can leverage the integration potential of large-area thin-film transistor (TFT) technology.



is less area- and power-efficient in this technology. Accordingly, our embedded DERMIS slip-sensing method adopts a predominantly analog, event-driven architecture, which is better aligned with the strengths and operating regime of the a-IGZO TFT process, while still enabling low-energy operation.

Fig.2:
a) Novel floating top plate capacitive tactile sensor transduces both shear and normal forces.
b) Readout scheme to directly measure and isolate normal and shear forces, depending on the grasp state.

Description

The DERMIS readout chip prototype includes a 2x2 array of per-taxel readout, pitch-matched to the sensor pitch of 600 µm. The per-taxel readout extracts normal and shear forces directly in the analog frontend, avoiding compute-intensive digital algorithms. This is enabled by differential capacitive sensors (Fig. 2a) whose square-wave drive phases are reconfigured to sense either the raw differential capacitance or normal force (Fig. 2b), while a ratiometric mode derives the shear force by using a neighboring taxel's output (Csp + Csn) as the level-crossing threshold (Fig. 2c). Each taxel's readout combines a fully differential capacitive frontend, which uses the sensor itself as input capacitance and thus removes extra charge amplifiers, with an asynchronous level-crossing converter that detects signal changes via window comparators and that outputs bipolar spikes encoded as addresses by an on-chip AER interface.

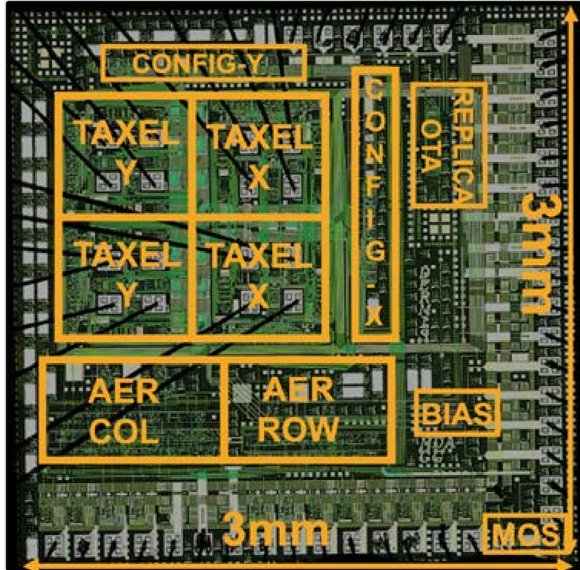


Fig.3: DERMIS chip prototype photo.

Results

The chip is implemented in the NMOS-only 0.6-µm a-IGZO TFT process (Fig.3). This work has presented the first fully-integrated large-area, grasp-state-reconfigurable tactile sensor readout with 600 µm per-taxel shear sensing resolution, paving the way for next-generation slip sensors. The per-taxel a-IGZO TFT readout achieves a peak ENOB of 4.12 bits over a 50-Hz bandwidth, corresponding to a Walden Figure of Merit (FoM) of 4 nJ/c.s. The AFE and ADC occupy only 0.04 and 0.11 mm² per taxel and dissipate 0.0006 and 0.007 mW, respectively, delivering an up to 10× better FoM, a 400× / 250× smaller area, and 60× / 10× less power than prior TFT-based readouts.

Why Europractice?

The integration of our a-IGZO TFT e-skin sensor readout required us to de-risk the design and fabricate a cost-effective prototype for future demonstrations, which was made possible through the Europractice MPW program. Europractice provided valuable technical guidance throughout the entire design and tape-out process. Although there were some delays in the chip delivery, this was understandable given that the TFT MPW offering is new.

Acknowledgements

This work has been supported in parts by the KU Leuven C3 Project DERMIS and by the European Union's Horizon 2020 programme under the Marie Skłodowska-Curie grant agreement No. 861166 (INTUITIVE).

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Exploring IC Design with Pragmatic Flexible Technology: Analog blocks for IoT wireless sensor node

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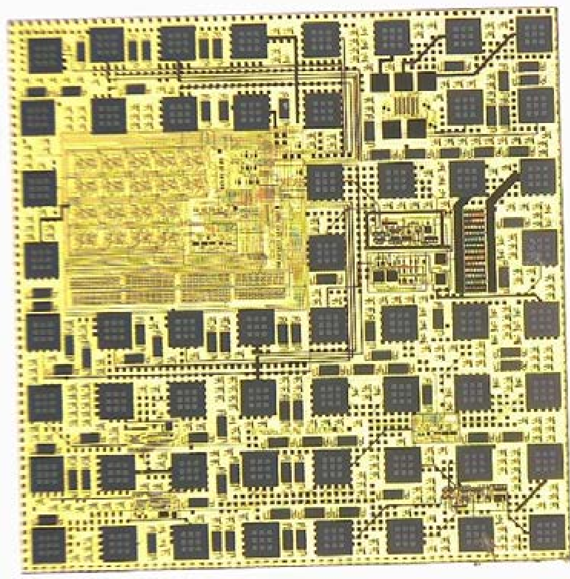
Technology:	Pragmatic FlexIC
Die Size:	3mm x 3mm
Application Area:	IoT

Introduction

At the University of Catania, the Microelectronics Design Laboratory is dedicated to advancing research and innovation in integrated circuits, with primary focus on low-power analog and mixed-signal design. This project marks our first engagement with Pragmatic technology, aimed at assessing its capabilities through the implementation of key building blocks for IoT wireless sensor nodes, including amplifiers, oscillators, analog-to-digital converters, voltage references, and charge pumps. The characterization of these circuits is providing critical insights necessary for the development and integration of more sophisticated systems in future SoC tape-outs. Pragmatic technology was selected due to its innovative approach to flexible IC fabrication, offering a valuable platform for exploring and validating new methodologies in circuit design.

Description

The Microelectronics group from the University of Catania has designed two integrated circuits (ICs) adopting the Pragmatic technology platform – Helvellyn v2.1.0.beta.2 process design kit (PDK). The implemented 3mm x 3mm ICs serve as an educational tool for both design exploration and performance evaluation. Moreover, the combination of some blocks integrated in both chips enables the implementation of a flexible IoT node able to monitor indoor light intensity without the necessity of external sensors. The ICs incorporate three primary functional domains:



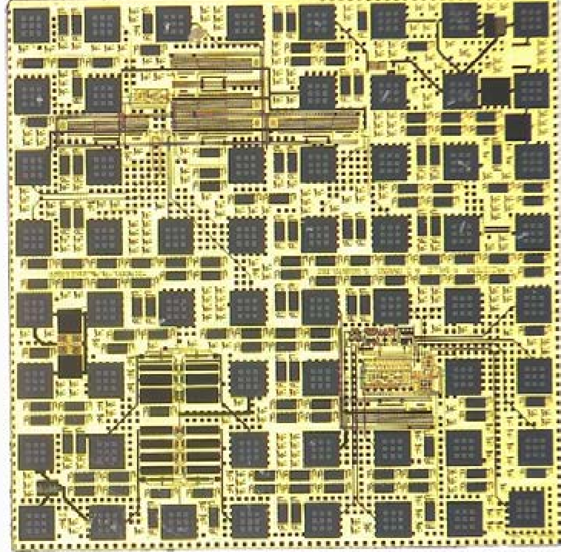


Fig.1: Micro-photographs of the FlexIC devices..

1. On-chip circuit blocks for light sensing: this section includes analog front-end for on-chip light sensing, analog-to-digital converter (ADC) and voltage regulator for internal supply distribution;
2. Circuital blocks for power management and RF-communication: this area features key components such as charge pumps, frequency locked loop (FLL) for both the power management unit and the ADC, and RF switch for backscattering communication;
3. Test-structures and innovative blocks: this section gathers operational amplifiers, digital gates and controlled oscillators with novel topologies on flexible substrates.

Since wire-bonding on Al pads on the chip is a challenging task, often resulting in scarce reliability of the connections, an unconventional and novel approach has been adopted to perform electrical characterization of the FlexICs.

Results

The IoT sensor node was characterized and the measurement results were accepted for being presented at the conference ISSCC 2026. A few other blocks were measured and related papers were submitted for both international journals and conference proceedings. Other devices are currently under testing and validation phase. The main result, as common factor among the various integrated blocks, is a partial agreement of the measurements with the simulations (by using Pragmatic's Helvellyn v2.1.0.beta.2 PDK), while a strong improvement in the model reliability is registered with the latest PDK release (Platform Gen 3).

Why Europractice?

At the University of Catania, we have relied on Europractice services for ASIC fabrication for many years. Their platform has consistently offered access to advanced technologies, dependable support, and an efficient route from design to silicon validation. This long-standing collaboration has significantly enhanced both our research activities and educational programs. In this project, we adopted Pragmatic's technology for the first time through Europractice. The adopted IC fabrication process experienced some reliability issues, and this was expected given the novelty and ongoing development of the FlexIC technology. Throughout the workflow, Europractice team provided valuable assistance, enabling us to address technical challenges and achieve our goals. Overall, our experience with Europractice continues to be highly positive. Their services remain crucial for supporting academic innovation in IC design, and we look forward to future collaborations.

Acknowledgements

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Open-Source IC Design for Classroom Use

ETH Zürich, Switzerland

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Technology:	IHP 0.13µm SG13G2 (open-source PDK)
Die Size:	2.25mm x 2.25mm
Application Area:	IoT

Introduction

At ETH Zürich, we have been teaching practical hands-on IC Design lectures for almost 40 years. Starting in 2025, this lecture has been converted to use a primarily open-source design flow based on the IHP 130 open-source PDK supported through Europractice, open-source EDA tools such as Yosys and OpenROAD, and a SoC template simplified for classroom use, called Croc, based on a compact 32bit RISC-V core (CVE2) and peripherals available through our PULP platform. The lectures and exercises have been openly published on our website (vlsi.ethz.ch).

A total of 65 students, working in groups of two, completed 33 designs as part of the lecture, which modified the example Croc system with various improvements, from peripherals to accelerators. We selected the five best designs from this group and, with the support of IHP, sent them for manufacturing in 2025.

A further four Croc designs were implemented testing various versions of standard cell libraries, bringing the total of designs associated with this course to nine.

Description

From our experience in teaching VLSI design and working on open-source hardware, we have developed Croc (https://github.com/pulp-platform/croc) as a teaching vehicle that can be adapted for many different tasks. Croc is a miniaturized SoC system that closely resembles modern designs. The heart of the system is a compact 32- bit RISC-V core (CVE2), which originates from our own work and was later maintained by LowRISC before being slightly adapted by the OpenHW group. Croc contains a set of peripherals (GPIO, UART), a JTAG programming interface, and provides access to user domain through the OBI interface. The repository for Croc, released under a permissive open-source license (Solderpad-0.51), includes all related modules incorporated in a mono-repo, which makes it easier to use for beginners.

The design has been optimized to run between 50-120 MHz in the IHP130nm process, and the exercise steps can be completed in reasonable time using standard desktop machines.

The students have to complete a project in which they enhance the basic Croc system, either by adding peripherals, attaching accelerators, or by adding instruction set extensions. In the first edition, the following five designs were submitted for fabrication:

- Chiffre (transparent SPI peripheral)
- Crocodillo (sensor data processing extensions with ECC and FFT support)
- Fluffy (integrated DMA support)
- PjonOnCroc (single-wire bus protocol support)
- River (SPI with DMA support)

During the preparation phase, Croc was implemented using different configurations and standard cell libraries, one of which (EZ library) was developed as part of a parallel VLSI lecture by Prof. Christoph Studer and Dr. Oscar Castañeda. The following four designs were taped out as part of this process:

- Mlem (first Croc implementation)
- Koopa (Croc using the initial version of the EZ standard cell library)
- Hati (Croc using an updated IHP standard cell library
- Skoll (Croc using the latest version of the EZ standard cell library)

We will continue developing and refining the lecture further in the upcoming years and build a strong, openly available VLSI lecture.

Results

As an educational activity, we were positively surprised by the results of this first edition of our course. We encountered far fewer problems, and the students enjoyed the project-based lecture a lot. We were able to easily disseminate the exercises to others and hope that our work will find use in many other teaching and training courses. It is important to note that it is not only the opensource EDA tools that made this possible; this activity has also been equally supported by leading commercial EDA companies, and Siemens has graciously given us permission to publish exercises using

their commercial tools (Questasim, Calibre) as well.
At the moment we are still waiting for the ICs to come back from manufacturing and are preparing for the next edition of the lecture where we also hope to have several designs manufactured through Europractice Services.

Why Europractice?

Europractice has been instrumental in our attempt to start such an adventure. While most of the design flow we used is based on open-source EDA tools, we still ended up using commercial EDA tools for a few design steps that relied on academic licenses provided through Europractice. The tape-out procedure was supported through the Europractice partner, Fraunhofer, which helped us through several issues and provided excellent support throughout our adventure in end-to-end open-source design.

Acknowledgements

These design has received generous support from Leibniz Institute for High Performance Microelectronics through the BMBF project FMD-QNC (16ME0831).
https://www.ihp-microelectronics.com/

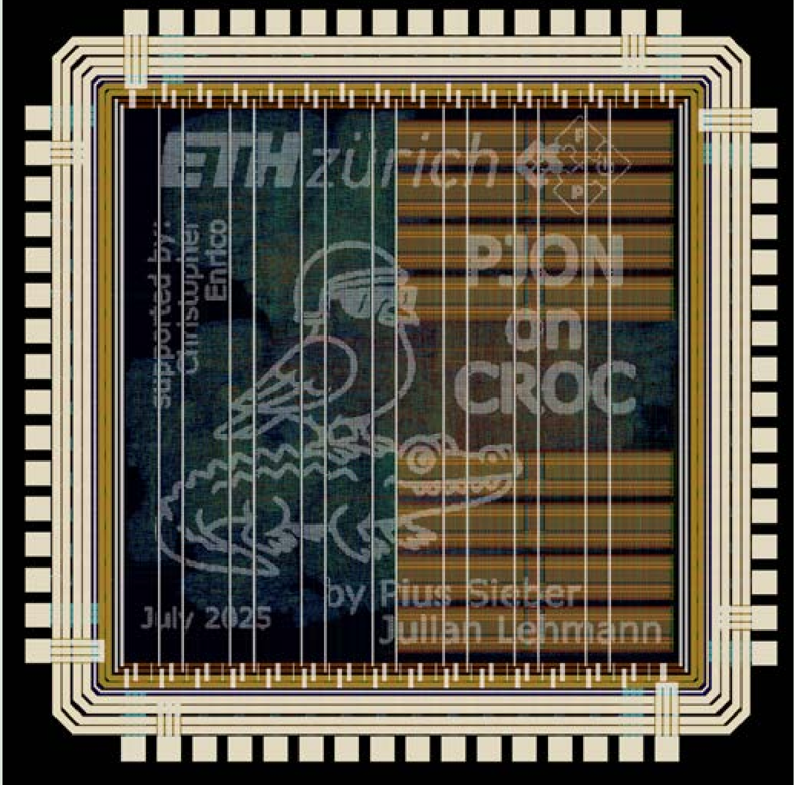

Fig.1: PJOnCroc chip

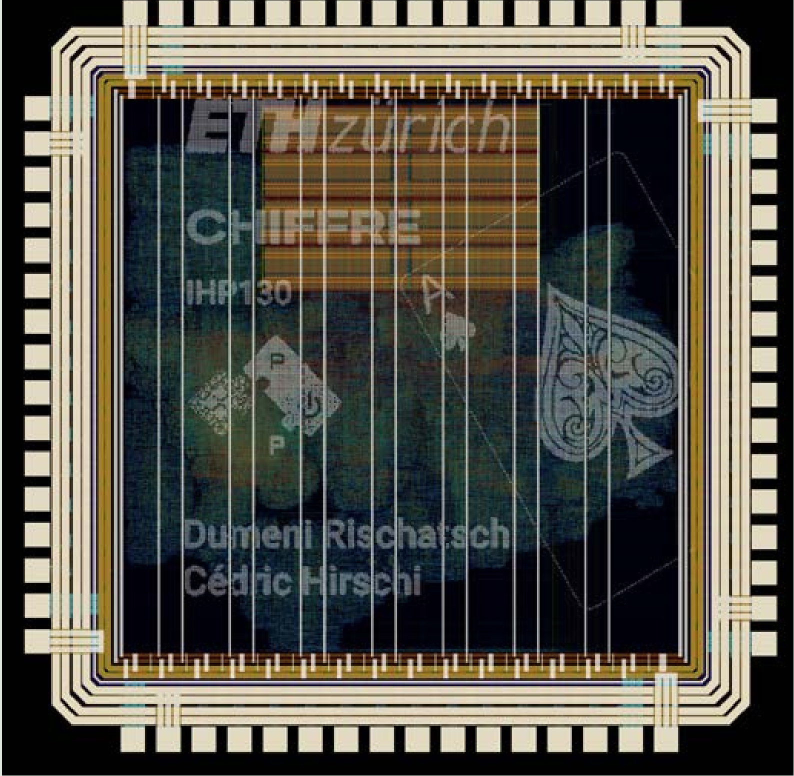

Fig.2: Chiffre chip

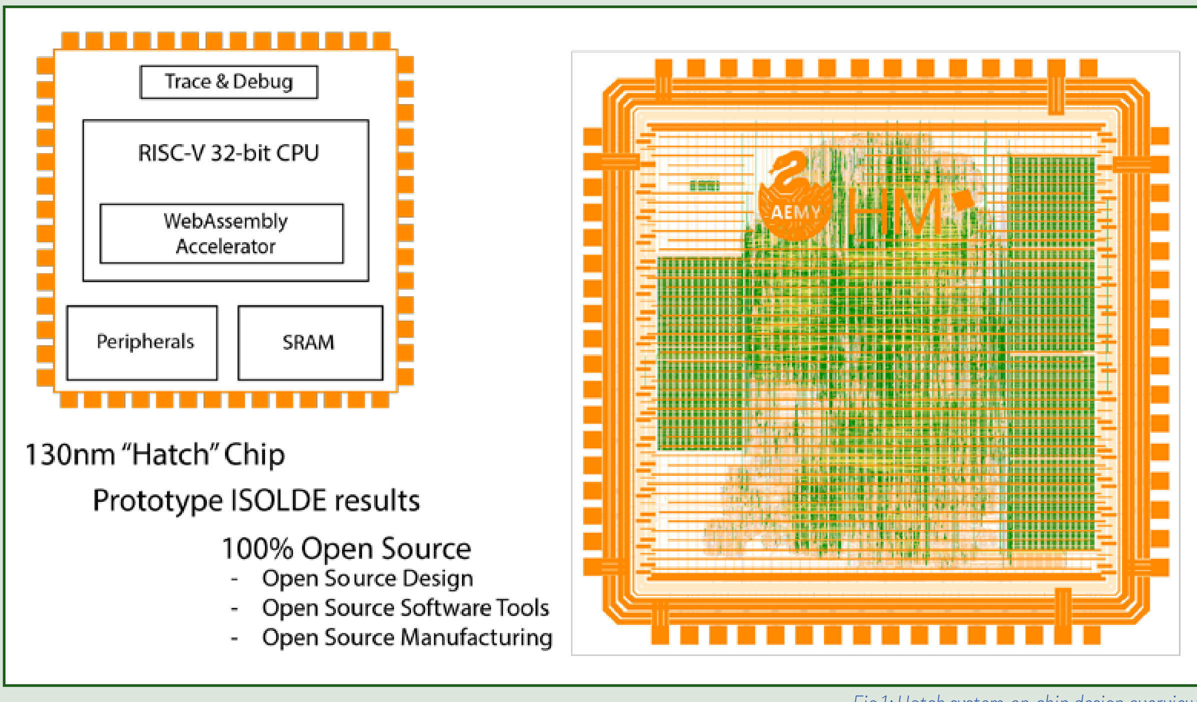

Fig.1: Hatch system-on-chip design overview

All Open Source: RISC-V SoC on IHP 130nm with LibreLane

HM Munich University of Applied Sciences, Germany

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E-mail:	stefan.wallentowitz@hm.edu
Technology:	IHP 0.13µm SG13G2 (open-source PDK)
Die Size:	2.5mm x 2.5mm
Application Area:	Open-Source Hardware

Introduction

We had two different goals with this device. For our teaching and research prototyping we are establishing a baseline system-on-chip, which is entirely built on open-source IP components and extends the great work of the PULP team at ETH Zürich. In the future, we can easily build and explore systems based on this and easily tape out regularly. In this first iteration, we included our own research results from a publicly funded research project on bytecode virtual machine acceleration.

Description

The system-on-chip is a 32-bit RISC-V processor core with custom instruction set extensions to accelerate interpreters of stack-based virtual machines, along with spacious SRAM. Furthermore, we are testing a tracing module that directly traces from software events to SRAM and allows reading it back from software. Finally, an analog block, a true random bit generator, is added for prototyping.

Results

The design is still in production and we are looking forward to receiving MPW samples soon.

Why Europractice?

As a partner of IHP, we used Europractice as MPW service. As this was our first end-to-end manufacturing using the new, exciting LibreLane open-source flow, it was great to have Europractice as a partner.

EUROPRACTICE MEMBERSHIP

Together with the funding provided by the European Commission, Europractice needs additional support to provide high quality service to more than 600 European universities and research institutes. Membership Fees pay for extra staff supporting this requested stimulation activity for academic institutions (not fully paid by the EC). The annual Membership Fee is collected by STFC on behalf of the Europractice project partners.

European universities and research institutes can choose from 4 different levels of membership:

1. **Full-IC annual membership: 1.100€**
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The number of academic members consists of more than 600 institutes in more than 40 countries from the EMEA zone (Europe, Middle East and Africa).

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R21020	Synchrotron SOLEIL
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