

EUROPRACTICE

TSMC RUN SCHEDULE 2027

October, 2026 – v1.0

MPW RUN SCHEDULE 2027

N7, N16, 22nm

28nm & 40nm

55nm & 65 nm

MPW RUN SCHEDULE 2027 – N7, N16, 22nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
7nm CMOS Logic or RF FinFET	January	10251	TM0C77	15	Oct 5 2026	Nov 20 2026	Dec 23 2026	Jan 17	Jan 19	May 17-Jun 21
	The 7nm Cybershuttle deadline(s) for the second half of 2027 will be known in March '27									
16nm CMOS Logic or RF FinFET Compact	April	10210	TM0C81	14	Dec 28 2026	Feb 25	Mar 29	Apr 23 **12PM**	Apr 26	Jul 24-Aug 28
	June	10211	TM0C82	14	Mar 1	Apr 29	May 31	Jun 25 **12PM**	Jun 28	Sep 27-Oct 30
	October	10253	TM0C84	14	Jun 25	Aug 19	Sep 20	Oct 15 **12PM**	Oct 18	Jan 15-Feb 19 2028
	December	10254	TM0C85	14	Aug 25	Oct 14	Nov 15	Dec 10 **12PM**	Dec 13	Mar 11-Apr 15 2028
22nm CMOS Logic or RF ULL (w/ or wo/ ReRam)	January	10214	TM0CA0	15	Oct 05 2026	Nov 13 (2026)	Dec 16 (2026)	Jan 10	Jan 12	Apr 07-May 12
	March	10215	TM0CA1	15	Nov 25 2026	Jan 15	Feb 17	Mar 14	Mar 16	Jun 09-Jul 14
	April	10216	TM0CA2	15	Dec 28 2026	Feb 12	Mar 17	Apr 11	Apr 13	Jul 07-Aug 11
	May	10216	TM0CA3	15	Jan 27	Mar 12	Apr 14	May 9	May 11	Aug 04-Sep 08
	August	10255	TM0CA5	15	Apr 28	Jun 25	Jul 28	Aug 22	Aug 24	Nov 17-Dec 22
	September	10218	TM0CA6	15	May 25	Jul 23	Aug 25	Sep 19	Sep 21	Dec 15-Jan 19 2028
	November	10219	TM0CA7	15	Jul 27	Sep 17	Oct 20	Nov 14	Nov 16	Feb 09-Mar 15 2028
	December	10256	TM0CA8	15	Aug 25	Oct 21	Nov 21	Dec 16	Dec 20	Mar 14-Apr 18 2028

*Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.
For FinFet designs, meeting the 12 PM CET cutoff is essential to ensure sufficient time for validation and feedback before the tape-out.

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MPW RUN SCHEDULE 2027 – 28nm & 40nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
28nm CMOS Logic or RF HPC/HPC+	January	10221	TM0CB0	15	Oct 05 2026	Nov 13 (2026)	Dec 16 2026	Jan 10	Jan 12	Apr 01-May 06
	March	10222	TM0CB2	15	Nov 25 2026	Jan 22	Feb 24	Mar 21	Mar 23	Jun 10-Jul 15
	May	10223	TM0CB3	15	Jan 27	Mar 19	Apr 21	May 16	May 18	Aug 05- Sep 09
	June	10224	TM0CB4	15	Mar 1	Apr 16	May 19	Jun 13	Jun 15	Sep 02-Oct 07
	September	10225	TM0CB6	15	May 25	Jul 23	Aug 25	Sep 19	Sep 21	Dec 09 -Jan 13 2028
	November	10226	TM0CB7	15	Jul 27	Sep 17	Oct 20	Nov 14	Nov 16	Feb 03-Mar 09 2028
	December	10227	TM0CB8	15	Aug 25	Oct 15	Nov 17	Dec 12	Dec 14	Mar 02-Apr 06 2028
40nm CMOS Logic LP (no triple gate oxide)	February	10232	TM0CC1	14	Oct 26 2026	Dec22 2026	Jan 25	Feb 18	Feb 22	May 31-Jul 05
	April	10233	TM0CC2	12	Dec 28 2026	Feb 18	Mar 22	Apr 15	Apr 19	Jul 16- Aug 20
	June	10234	TM0CC3	14	Mar 1	Apr 22	May 24	Jun 17	Jun 21	Sep 01-Oct 06
	August	10257	TM0CC4	14	Apr 28	Jun 17	Jul 19	Aug 12	Aug 16	Oct 27-Dec 01
	October	10235	TM0CC5	12	Jun 25	Aug 19	Sep 20	Oct 14	Oct 18	Dec 29-Feb 02 2028
	December	10258	TM0CC6	14	Aug 25	Oct 21	Nov 22	Dec 16	Dec 20	Mar 01-Apr 05 2028
40nm CMOS MS/RF, GP (no triple gate oxide)	April	10236	TM0CC2	12	Dec 28 (2026)	Feb 18	Mar 22	Apr 15	Apr 19	Jun 30-Aug 04
	October	10237	TM0CC5	12	Jun 25	Aug 19	Sep 20	Oct 14	Oct 18	Dec 29-Feb 02 2028

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.

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MPW RUN SCHEDULE 2027 – 55nm ~ 65nm

Technology	Month	Run	Foundry ref	Fab	Reserve before	Signed quote/PO before	Dry run GDS	Final GDS*	Tape-out	Estimated shipment date
55nm CMOS Logic or MS/RF, GP or LP or ULP	May	10238	TM0CA9	14	Jan 27	Mar 19	Apr 21	May 16	May 18	Jul 26-Aug 30
65nm CMOS Logic or MS/RF, GP or LP**	January	10239	TM0CD1	14	Oct 05 2026	Nov 06	Dec 02	Dec 22 2026	Jan 05	Mar 16-Apr 20
	March	10240	TM0CD2	12	Nov 25 2026	Jan 02	Feb 03	Feb 28	Mar 02	May 11-Jun 15
	April	10241	TM0CD3	14	Dec 28 2026	Feb 19	Mar 24	Apr 18	Apr 20	Jun 29-Aug 03
	June	10242	TM0CD4	14	Mar 01	Apr 23	May 26	Jun 20	Jun 22	Aug 31-Oct 05
	September	10243	TM0CD6	14	May 25	Jul 09	Aug 11	Sep 05	Sep 07	Nov 16-Dec 21
	December	10244	TM0CD8	14	Aug 27	Oct 1	Nov 3	Nov 28	Nov 30	Feb 08-Mar 14 2028

* Provide final GDS two weeks earlier in case of IP merge. In case of LVS or other services are required, please reach out to eptsmc@imec.be at the purchase order stage.
** 65nm eFuse is only supported in Fab12. Please select the correct shuttle.

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GUIDELINES FOR SCHEDULE 2027

Design registration guidelines

- Single reservation for multiple chips
- No backup reservation
- Provide single GDS with all designs,
  - Enclosed with TSMC sealring + 80um scribe (post-shrink if applicable).
  - If designs are not identical, put marker in the scribe line.
  - Add dummies to the scribe line for 12-inch tape-outs.
  - Exception: multiple reservations accepted for different projects with different metal stacks or far backend.

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Shipment guidelines

- The estimated shipment date is applicable for reservations with quantity <200 dies.
- If additional samples are required above 200 dies, additional cycle time of 1~3 weeks might be needed.
- Cycle time estimates are based on typical conditions. Corner wafers or SHDMiM processing requires additional cycle time.
- Optional services adding cycle time
  - Wafer thinning (thinner than 10mils): up to 12 days
  - Additional bumped wafer thinning and die saw (each 200 ea.): 5 working days

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IP Merge Guidelines

- To ensure timely inclusion in the TSMC MPW when an IP merge is required, deliver the final GDS 2 weeks in advance to allow sufficient time for integration and validation.
- Why This Matters:
  - **Complete LVS Setup Required**

    A fully validated LVS setup must be in place before initiating the merge process.
  - **Ip-transfer**

    Third-party IPs have to be transferred from the vendor to the TSMC merge team, which may introduce delays in the process.
  - **Increased Complexity with Multiple IP Instances**

    Merging several IP blocks adds significant complexity and increases the risk of integration issues.
  - **Merge Errors Can Jeopardize the Deadline**

    Errors discovered after merging may delay the process and reduce the likelihood of meeting the MPW schedule. TSMC requests to re-submit the merge even for minor typos or missing files

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Questions?

Contact our teams through a portal support case:

Support Tape-out	For support on the tape-out submission
Support SalesOps	For support on portal, quotations, export documents, purchase orders, and design registration questions
Support EP packaging	For any question related to the Europractice packaging offer.
Support Foundry	For support on foundry libraries, PDK's (installation, flavors, bugs, ...), LVS

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Release notes

- October, 2026
  - Release of v 1.0 2026

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